The First IEEE International Conference on Field-Programmable Technology (FPT' 02)

Monday 16 December 2002

0800-1830 Registration

0830-0845 Welcome

0845-0900 Special Keynote: Paul Y.S. Cheung, Policy Advisor, Innovation and Technology Commission, Hong Kong Government
Title: Technology Research and Development in Hong Kong: Hype or Reality

0900-0940
Keynote: Tsugio Makimoto, Sony Corporation
Title: The Hot Decade of Field Programmable Technologies

Session 1: Networking Applications (0940-1030)
Session Chair: S.J.E. Wilton, University of British Columbia

Paper : Real-time Packet Editing Using Reconfigurable Hardware for Active Networking
Authors : T. Miyazaki, T. Murooka, N. Takahashi and M. Hashimoto

Paper : Implementation of an FPGA Based Accelerator for Virtual Private Networks
Authors : O.Y.H. Cheung and P.H.W. Leong

1030-1110 - Coffee and Poster Session 1

Session 2: Run-time Reconfiguration Technology (1110-1250)
Session Chair: C.C. Cheung, Chinese University of Hong Kong

Paper : Compiling Run-Time Parametrisable Designs
Authors : A. Derbyshire and W. Luk

Paper : Adaptive FIR Filter Architectures for Run-Time Reconfigurable FPGAs
Authors : T. Rissa, R. Uusikartano and J. Niittylahti

Paper : A Methodology for Design of Run-time Reconfigurable Systems
Authors : G. Lee and G. Milne

Paper : Resource-Aware Run-time Elaboration of Behavioural FPGA Specifiations
Authors : U. Malik, K. So and O. Diessel

1250-1415 – Lunch

1415-1455
Keynote: Patrick Lysaght, Xilinx, Inc.
Title: FPGAs as Meta-platforms for Embedded Systems

Session 3: Signal and Matrix Processing (1455-1650)
Session Chair: O. Diessel, University of New South Wales

Paper : High-Speed Programmable Sum-of-Power-of-Two (SOPOT) Finite-Duration Impulses Response (FIR) Filters
Authors : K.S. Yeung and S.C. Chan

Paper : FPGA-based System-level design framework based on the IRIS synthesis tool and System Generator
Authors : Y. Yi and R. Woods

Paper : Area and Time Efficient Implementation of Matrix Multiplication on FPGAs
Authors : J. Jang, S. Choi and V.K. Prasanna

1610-1650 - Tea and Poster Session 2

Session 4: FPGA-based Applications (1650-1830)
Session Chair: T. Rissa, Nokia

Paper : A System Level Implementation of Rijndael on a Memory-slot based FPGA Card
Authors : D.K.Y. Tong, P.S. Lo, K.H. Lee and P.H.W. Leong

Paper : FPGA-Based Cloud Detection for Real-Time Onboard Remote Sensing
Authors : J.A. Williams, A.S. Dawood and S.J. Visser

Paper : An FPGA-Based Processor for Shogi Mating Problems
Authors : Y. Hori, M. Sonoyama and T. Maruyama

Paper : Population based Ant Colony Optimization on FPGA
Authors : M. Guntsch, B. Scheuermann and H. Schmeck

Tuesday 17 December 2002

0800-1830 Registration

0900-0940
Keynote: Michael J. Flynn, Stanford University
Title: Programmed Solutions: The step beyond Programmed Logic

Session 5: Reconfigurable and Memory Architectures (0940-1030)
Session Chair: O. Mencer, Bell Laboratories

Paper : Clustered Programmable-Reconfigurable Processors
Authors : D.B. Gottlieb, J.J. Cook, J.D. Walstrom, S. Ferrera, C.Wang and N.P. Carter

Paper : Implementing Logic in FPGA Embedded Memory Arrays: Heterogeneous Memory Architectures
Authors : S.J.E. Wilton

1030-1110 - Coffee and Poster Session 3

Session 6: High-Level Design Tools (1110-1250)
Session Chair: A. Fong, City University of Hong Kong

Paper : Optimising and Adapting High-Level Hardware Designs
Authors : J.G.F. Coutinho and W. Luk

Paper : Floating-Point Bitwidth Analysis via Automatic Differentiation
Authors : A.A. Gaffar, O. Mencer, W. Luk, P.Y.K. Cheung and N. Shirazi

Paper : DRESC: A Retargetable Compiler for Coarse-Grained Reconfigurable Architectures
Authors : B. Mei, S. Vernalde, D. Verkest, H.D. Man and R. Lauwereins

Paper : A Prolog Based Hardware Description Environment
Authors : K. Benkrid, S. Belkacemi and D. Crookes

1250-1300
Special Session: Masahiro Fujita, The University of Tokyo
Title: Presentation on FPT'03 (Tokyo)

1300-1415 Lunch

1415-1455
Keynote: Paul Master, Quicksilver Technology
Title: The Next Big Leap in Reconfigurable Systems

Session 7: Reconfigurable Circuits and Devices (1455-1610)
Session Chair: H. Lau, University of Hong Kong

Paper : Gigahertz SiGe BiCMOS FPGAs with new architectures and novel power management schemes
Authors : K. Zhou, Channakeshav, J. Guo, S. Liu, R.P. Kraft, C. You and J.F. McDonald
Paper : Evolutionary Analog Circuit Design on a Programmable Analog Multiplexer Array
Authors : C.C. Santini, J.F.M. Amaral, M.A.C. Pacheco and M.M. Vellasco

Paper : An Optically Differential Reconfigurable Gate Array and its Power Consumption Estimation
Authors : M. Watanabe and F. Kobayashi

1610-1650 - Tea and Poster Session 4

Session 8: Technology Mapping and Layout Tools (1650-1830)
Session Chair: T. Kok, Hong Kong University of Science and Engineering

Paper : A Technology Mapping Algorithm for CPLD Architectures
Authors : S. Chen, T.T. Hwang and C.L. Liu

Paper : Power-Aware Technology Mapping for LUT-Based FPGAs
Authors : J.H. Anderson and F.N. Najm

Paper : Synthesizing Datapath Circuits for FPGAs with Emphasis on Area Minimization
Authors : A. Ye, J. Rose and D. Lewis
Paper : The Effect of Cluster Packing and Node Duplication Control in Delay Driven Clustering
Authors : M.E. Dehkordi and S.D. Brown

2000-2330 : Conference Dinner (Hong Kong Harbour Cruise)

1915 : Shuttle bus leaves Esther Lee Building for Ferry Pier
1945 : OR Meet and embark at Hung Hom Ferry Pier

Wednesday 18 December 2002

0800-1250 Registration

0900-0940
Keynote: Erik Cleage, Altera Corporation
Title: The Economics of FPGAs, ASSPs & ASICs

Session 9: Debugging Methods (0940-1030)
Session Chair: Y.L. Wu, Chinese University of Hong Kong

Paper : Debug Methodology for Arithmetic Circuits on FPGAs
Authors : M. Kubo and M. Fujita

Paper : Debug Methods for Hybrid CPU/FPGA Systems
Authors : E. Roesler and B. Nelson

1030-1110 - Coffee and Poster Session

Session 10: Instruction Processors and Systems (1110-1250)
Session Chair: S.C. Chan, University of Hong Kong

Paper : Scalable Acceleration of Inductive Logic Programs
Authors : A. Fidjeland, W. Luk and S. Muggleton

Paper : A Fine-Grained Reconfigurable Logic Array Based on Double Gate Transistors
Authors : P. Beckett

Paper : A Co-simulation Study of Adaptive EPIC Computing
Authors : V.S. Gheorghita, W. Wong, T. Mitra and S. Talla

Paper : System on Programmable Chip for Real-Time Control Implementations
Authors : D.L.S. Pradel, S.R. Jones and R.M. Goodall

1250-1300 - Closing Remarks

1430-1730 – Asia Pacific Technology Forum, LT3, Esther Lee Building

Thursday 19 December 2002

0930-1800 – Technical Tutorials, LT2, Sino Building

Thanks for joining the FPT'02 conference!
We look forward to seeing you in FPT'03 in Japan.