IEEE ICFPT 2003
Final Technical Programme

Monday, 15 December, 2003

0800-1830
Registration

0840-0900
Welcome

0900-0940 *Session Chair: Masahiro Fujita, University of Tokyo*
Keynote:
Title: A Reconfigurable Future
Speaker: Phil Bishop
Celoxica Ltd.

Session 1: Applications 1
Session Chair: Masahiro Fujita, University of Tokyo

0940-1005
Paper: High Resolution ADPLL Frequency Synthesizer for FPGA- and ASIC-based Applications
Authors: Riad Stefo, Jorg Schreiter, Jens-Uwe Schlußler and Rene Schuffny
Dresden University of Technology

1005-1030
Paper: Improved SVD Systolic Array and Implementation on FPGA
Authors: A. Ahmedsaid, A, Amira and A. Bouridane
The Queen's University of Belfast

1030-1050
Coffee Break

Session 2: Cryptography & Computer Security
Session Chair Wayne Luk, Imperial College

1050-1115
Paper: An implementation of the Rijndael on Async-WASMII
Authors: Y. Adachi, K. Ishikawa, S. Tsutsumi, H. Amano
Keio University

1115-1140
Paper: Modular Exponentiation using Parallel Multipliers

Authors: S.H. Tang, K.S. Tsui and P.H.W. Leong
The Chinese University of Hong Kong

1140-1205
Paper: Implementation of Elliptic Curve Cryptosystems on a Reconfigurable Computer
Authors: Nghi Nguyen, Kris Gaj, David Caliga, Tarek El-Ghazawi
George Mason University, SRC computers, The George Washington University

1205-1230
Paper: A Pattern-Matching Co-Processor for Network Instrusion Detection
Authors: Christopher R. Clark and David E. Schimmel
Georgia Institute of Technology

1230-1305
Poster Short Presentation 1 (3min * 11)

1305-1415
Lunch and Poster Session 1&2

1415-1455 *Session Chair Steve Wilton, University of British Columbia*
Invited Paper:
Title: Seamless top-down flow for quick trial of HW/SW co-design
Speaker: Naotoshi Nojiri and Tadatoshi Ishii
Interdesign Technology, Inc.

Session 3: Computer Arithmetic
Session Chair Steve Wilton, University of British Columbia

1455-1520
Paper: A Parallel Look-up Logarithmic Number System Addition/Subtraction Scheme for FPGA
Authors: B.R.Lee and N.Burgess
Cardiff University

1520-1545
Paper: Arbitrary Function Approximation in HDLs
Authors: C.H. Ho, K.H. Tsoi, H.C. Yeung, Y.M. Lam, K.H. Lee, P.H.W. Leong, R. Ludewig, P. Zipf, A.G. Ortiz, M. Glesner
The Chinese University of Hong Kong, Darmstadt University

1545-1610
Paper: Hierarchical Segmentation Schemes for Function Evaluation
Authors: Dong-U Lee, Wayne Luk, John Villasenor and Peter Cheung
Imperial College, University of California, Los Angeles

1610-1645
Poster Short Presentation 2 (3min * 11)

1645-1710
Tea Break and Poster Session 1&2

Session 4: Signal Processing
Session Chair Neil Bergmann, University of Queensland

1710-1735
Paper: FPGA Implementations of Fast Fourier Transforms for Real-Time Signal and Image Processing
Authors: I.S. Uzun, A. Amira and A. Bouridane
The Queen's University of Belfast

1735-1800
Paper: An FPGA-based Re-configurable 24-bit 96kHz Sigma-Delta Audio DAC
Authors: Ray C.C. Cheung, K.P. Pun, Steve C.L. Yuen, K.H. Tsoi and Philip H.W. Leong
The Chinese University of Hong Kong

1800-1825
Paper: Reconfiguration Requirements for High Speed Wireless Communication Systems
Authors: T. Pionteck, L.D. Kabulepa and M. Glesner
Darmstadt University of Technology

1825-1850
Paper: An FPGA Implementation of Kak's Instantaneously-Trained, Fast-Classification Neural Networks
Authors: Jihan Zhu and Peter Sutton
The University of Queensland

1900-2100
Reception Party (Sponsored by Elixent Ltd.)

Tuesday, 16 December, 2003

0800-1830
Registration

0830-0910 *Session Chair Makoto Ikeda, University of Tokyo*
Keynote:
Title: Networking on Chip with Platform FPGAs
Speaker: Delon Levi and Gordon Brebner
Xilinx, Inc.

Session 5: Runtime Reconfiguration
Session Chair Makoto Ikeda, University of Tokyo

0910-0935
Paper: Concept and Implementation of Run-time Resource Management System Operating on Autonomously Reconfigurable Architecture
Authors: Yoshiki Nakane, Kouichi Nagami, Tsunemichi Shiozawa and Akira Nagoya
NTT Corporation

0935-1000
Paper: High-level Language Extensions of Run-time Reconfigurable Systems
Authors: T.K. Lee, A. Derbyshire, W. Luk and P.Y.K. Cheung
Imperial College

1000-1020
Coffee Break

Session 6: FPGA Architectures
Session Chair Oliver Diessel, University of New South Wales

1020-1045
Paper: Placement and Routing for FPGA Architectures Supporting Wide Shallow Memories
Authors: Steven W. Oldridge and Steven J.E. Wilton
University of British Columbia

1045-1110
Paper: Product-term Based Synthesizable Embedded Programmable Logic Cores
Authors: Andy Yan and Steven J.E. Wilton
University of British Columbia

1110-1135
Paper: An Architecture for Asynchronous FPGAs
Authors: Catherine G. Wong, Alain J. Martin and Peter Thomas

California Institute of Technology

1135-1200
Paper: Evaluation of Network Topologies for a Run Time Re-routable Network on a Programmable Chip
Authors: David A. Kearney and Gerard Veldman
The University of South Australia

1200-1235
Poster Short Presentation 3 (3min * 11)

1235-1245
Special Presentation: Prof. Neil Bergman
Title: FPT 2004 – Brisbane Australia

1245-1400
Lunch and Poster Session 3&4

Session 7: Applications 2
Session Chair David Kearney, University of South Australia

1400-1425
Paper: A High-speed Ray Tracing Engine Built on a Field-Programmable System
Authors: Joshua Fender and Jonathan Rose
University of Toronto

1425-1450
Paper: Reconfigurable Real-time Address Trace Compressor for Embedded Microprocessors
Authors: Shyh-Ming Huang, Ing-Jer Huang and Chung-Fu Kao
National Sun Yat-Sen University

1450-1515
Paper: Customising Parallelism and Caching for Machine Learning
Authors: Andreas Fidjeland and Wayne Luk
Imperial College

1515-1545
Poster Short Presentation 4 (3min * 10)

1545-1610
Tea Break and Poster Session 3&4

Session 8: Image Processing
Session Chair Nick Carter, University of Illinios

1610-1635
Paper: A Low Cost FPGA System for High Speed Face Detection and Tracking
Authors: Stavros Paschalakis and Miroslaw Bober
Mitsubishi Electric ITE B.V.

1635-1700
Paper: An Autonomous Flying Object Navigated by Real-time Optical Flow and Visual Target Detection
Authors: Hitoshi Yamada, Takashi Tominaga, and Michinori Ichikawa
RIKEN BSI

1700-1725
Paper: FPGA based EBCOT Architecture for JPEG 2000
Authors: Manjunath Gangadhar and Dinesh Bhatia
University of Texas at Dallas

1725-1750
Paper: FPGA-based Computation of Free-Form Deformations in Medical Image Registration
Authors: Jun Jiang, Wayne Luk and Daniel Rueckert
Imperial College

1830
Buses depart from the conference venue for conference dinner.

1900-2100
Conference Dinner (on Japanese-style houseboat)

Wednesday, 17 December, 2003

0800-1250
Registration

0900-0940 *Session Chair Philip Leong, Chinese University of Hong Kong*
Invited Paper: I2
Title: FPGA-Based High-Speed Emulator of Quantum Computing
Speaker: Minoru Fujishima
The University of Tokyo

Session 9: Platforms for Reconfigurable Computing
Session Chair Philip Leong, Chinese University of Hong Kong

0940-1005
Paper: DIMES: An Iterative Emulation Platform for Multiprocessor-System-On-Chip Designs
Authors: Hirofumi Sakane, Levent Yakay, Vishal Karna, Clement Leung and Guang R. Gao
University of Delaware

1005-1030
Paper: TKDM – A Reconfigurable Co-processor in a PC's Memory Slot
Authors: Christian Plessl and Marco Platzner
Swiss Federal Institute of Technology

1030-1050
Coffee Break

Session 10: Hardware Compilation and CAD
Session Chair Satoshi Komatsu, University of Tokyo

1050-1115
Paper: Performance-Driven Recursive Multi-Level Clustering
Authors: Mehrdad Eslami Dehkordi and Stephen D. Brown
University of Toronto

1115-1140
Paper: Design Space Exploration with A Stream Compiler
Authors: Oskar Mencer, David J. Pearce, Lee W. Howes and Wayne Luk
Imperial College

1140-1205
Paper: Source-directed Transformations for Hardware Compilation
Authors: Jose Gabriel F. Coutinho and Wayne Luk
Imperial College

Poster Session 1

Paper: An FPGA Based Coprocessor for 3D Affine Transformations
Authors: F.Bensaali, A.Amira and A.Bouridane
The Queen's University of Belfast

Paper: An FPGA Based Coprocessor for Large Matrix Product Implementation
Authors: F. Bensaali, A. Amira and A. Bouridane
The Queen's University of Belfast

Paper: Using FPGA to implement a N-channel Arbitrary Waveform Generator with Various Add-On Functions
Authors: Jen-Wei Hsieh, Guo-Ruey Tsai and Min-Chuan Lin
Kun-Shan University of Technology

Paper: Design of FPGA-based Adaptive Remote Calibration Control System
Authors: Yuan-Long Jeang, Liang-Bi Chen, Chia-Pin Huang, Yu-Hsiang Hsu, Ming-Yu Yeh and Kai-Ming Yang
National Kaohsiung University of Applied Sciences

Paper: Performance Optimization of an FPGA-Based Configurable Multiprocessor for Matrix Operations
Authors: Xiaofang Wang and Sotirios G. Ziavras
New Jersey Institute of Technology

Paper: Bayesian Digital Terrain Model Reconstruction on Virtex-II FPGA
Authors: Han Tao, Toh Lik Khoong and Chai Geok Ling Serena
DSO National Laboratories

Paper: A Coarse-Grained Reconfigurable Architecture with Low Cost Configuration Data Compression Mechanism
Authors: Kazuya Tanigawa, Takashi Kawasaki and Tetsuo Hironaka
Hiroshima City University

Paper: An Embedded In-circuit Emulator Generator for SOC Platform
Authors: Yuan-Long Jeang, Liang-Bi Chen, Yi-Ting Chou, and Hsin-Chia Su
National Kaohsiung University of Applied Sciences

Paper: A Crystal-Based Digital Ring Oscillator
Authors: S. R. Abdollahi, B. Bakkaloglu and S. M. Fakhraei
University of Tehran, Texas Instrument

Poster Session 2

Paper: A Parameterized Automatic Cache Generator for FPGAs

Authors:	Peter Yiannacouras and Jonathan Rose University of Toronto
Paper:	A Field-customizable and Runtime-adaptable Microarchitecture
Authors:	Toshinori Sato and Daisuke Morishita Japan Science and Technology Agency, Kyushu Institute of Technology
Paper:	On-chip Communication Architectures for Reconfigurable System-on-Chip
Authors:	Andy S. Lee and Neil W. Bergmann The University of Queensland
Paper:	Three Video Applications using an FPGA based pyramid implementation: Tracking, Mosaics and Stabilization
Authors:	Marco Aurelio Nuño-Maganda, Miguel O. Arias-Estrada and Claudia Feregrino-Uribe Instituto Nacional de Astrofisica
Paper:	The Egret Platform for Reconfigurable System on Chip
Authors:	Neil W. Bergmann and John Williams The University of Queensland
Paper:	A Temporal Partitioning Approach Based on Reconfiguration Granularity Estimation for Dynamically Reconfigurable Systems
Authors:	Xue-jie Zhang and Kam-wing Ng Chinese University of Hong Kong, Yunnan University
Paper:	Beyond Performance: Secure and Fair Memory Management for Multiple Systems on a Chip
Authors:	Carlos Maci´an, Sarang Dharmapurikar and John Lockwood University of Stuttgart
Paper:	Double Precision Floating-Point Arithmetic on FPGAs
Authors:	Stavros Paschalakis and Peter Lee Mitsubishi Electric ITE BV
Paper:	Temporal Task Clustering for Online Placement on Reconfigurable Hardware
Authors:	Ali Ahmadinia, Christophe Bobda and Jürgen Teich University of Erlangen-Nuremberg
Paper:	Reconfigurable Parallel Comparator Architecture and Its Application to IP Packet Filters
Authors:	Noriuki Aibe and Moritoshi Yasunaga University of Tsukuba

Paper: Reconfigurable Architecture for Probabilistic Neural Network System
Authors: Ryosuke Mizuno, Noriyuki Aibe, Moritoshi Yasunaga and Ikuo Yoshihara
University of Tsukuba, Miyazaki University

Poster Session 3

Paper: Parallel Image Processing Field Programmable Gate Array for Real Time Image Processing System
Authors: Takeaki Sugimura, JeoungChill Shim, Hiroyuki Kurino and Mitsumasa Koyanagi
Tohoku University

Paper: Artificial neural networks as building blocks of FPGA
Authors: Manjunath. R and K.S. Gurumurthy
UVCE

Paper: Specification and Integration of Software and Reconfigurable Hardware Components in Hardware Join Java
Authors: John Hopf and David Kearney
University of South Australia

Paper: Architecture Template with Dynamic Buffering for Runtime Reconfiguration of Adaptive Embedded Communication Systems
Authors: Dirk Eilers, Helmut Steckenbiller and Rudi Knorr
Fraunhofer Institute for Communication Systems

Paper: Accelerating Signal Processing Algorithms in Digital Holography Using an FPGA Platform
Authors: Thomas Lenart, Viktor Öwall, Mats Gustafsson, Mikael Sebesta and Peter Egelberg
Lund University

Paper: A New Approach for Reconfigurable Massively Parallel Computers
Authors: Christophe Bobda, Klaus Danne, Ali Ahmadinia and J¨urgen Teich
University of Erlangen

Paper: An FPGA Implementation of a Special Purpose Processor for Steganography
Authors: Hala A. Farouk and Magdy Saeb
Arab Academy for Science

Paper: Comparing the Usage of FPGA Area by Simple Applications Specified in Hardware Join Java and HandelC
Author: John Hopf
University of South Australia

Paper: Abstractions and Primitives Enabling Runtime Resource Allocation for Dynamic IP Cores Using Virtual Platform FPGAs
Authors: David A. Kearney, Gerard Veldman and David Warren
University of South Australia

Paper: Combined Run-time Area Allocation and Long Line Re-routing for Reconfigurable Computing
Author: Mark D. Jasiunas
University of South Australia

Paper: A Concurrent Multi-bankMemory Arbiter for Dynamic IP Cores using Idle Skip Round Robin
Authors: David A. Kearney and Gerard Veldman
The University of South Australia

Poster Session 4

Paper: Augmenting General Purpose Processors for Network Processing
Authors: Hamid Reza Ghasemi, Hossein Mohammadi, Behnam Robatmili and Nasser Yazdani
University of Tehran

Paper: Design of Low Cost FPGA Based PCI Bus Sniffer
Authors: Chee Wei Liang, Noohul Basheer Zain Ali and Ramesh Seth Nair
Universiti Teknologi Petronas

Paper: FPGA implementation of real-time image convolutions with three level of memory hierarchy
Authors: Hongtu Jiang and Viktor Owall
Lund University

Paper: Fault Injection into SRAM-based FPGAs for the Analysis of SEU Effects
Authors: Ghazanfar Asadi, Seyed Ghassem Miremadi, Hamid Reza Zarandi and Alireza Ejlali
Sharif University of Technology

Paper: Compiling to FPGAs via an EPIC Compiler's Intermediate Representation
Authors: Zhiguo Ge, Jirong Liao and Weng-Fai Wong
National University of Singapore

Paper: Mapping Computation Kernels to Clustered Programmable-Reconfigurable Processors
Authors: Jeffrey J. Cook, Lee W. Baugh, Derek B. Gottlieb and Nicholas P. Carter
University of Illinois at Urbana-Champaign

Paper: Multisensor Inversion with High-Performance FPGA Computation

Authors: Yongxiang Hu, Yang Cai and Mark Tomzak
NASA Langley Research Center, Carnegie Melon University

Paper: Exploiting System-Level Parallelism in the Application Development on a Reconfigurable Computer
Authors: Esam El-Araby, Mohamed Taher, Kris Gaj, Tarek El-Ghazawi, David Caliga and Nikitas Alexandridis
The George Washington University, George Mason University, SRC Computers

Paper: The Multiplier Tree FIR Filter Architecture
Authors: A. Carreira and T.W. Fox

Paper: FPGA Implementable Architecture for Geometric Positioning
Authors: Anant Utgikar, Guna Seetharaman and Ha Le
University of Louisiana at Lafayette