The 2010 International Conference on Field-Programmable Technology (FPT'10)

Tsinghua University, Beijing, China

8 - 10 December 2010

ADVANCE PROGRAM

Date	Day	Start Time	EndTime	Title	Authors
8/12/10	**Wed**	**0740**	**0800**	**Bus Line: Jinchunyuan → Jiasuo → Main Building**	**Jinchunyuan (7:40), Jiasuo (7:50)**
	Wed	**0800**	**1100**	**REGISTRATION**	
	Wed	**0800**	**0820**	**Welcome**	
	Wed	**0820**	**0950**	**Keynote Session 1.1**	**Chair: Yajun Ha**
	Wed	0820	0905	**Reconfigurable Computing – Evolution of Von Neumann Architecture**	Prof. Shaojun Wei Tsinghua University
		0905	0950	**FPGA platforms leading the way in the application of 'More than Moore's' technology**	Dr. Ivo Bolsens CTO of Xilinx, Inc.
	Wed	**1000**	**1100**	**Morning Tea, Poster Session 1.2, see details below**	
	Wed	**1100**	**1220**	**Oral Session 1.3 - Architectures**	**Chair: Jimmei Lai**
	Wed	1100	1120	An FPGA Architecture Supporting Dynamically Controlled Power Gating	Assem A. M. Bsoul and Steven J. E. Wilton
	Wed	1120	1140	A Tiled Programmable Fabric using QCA	Rajeswari Devadoss, Kolin Paul and M Balakrishnan
	Wed	1140	1200	Phase-Change-Memory-Based Storage Elements for Configurable Logic	Pierre-Emmanuel Gaillardon, M. Haykel Ben-Jamaa, Marina Reyboz, Giovanni Betti
	Wed	1200	1220	Dynamic Reconfigurable Bit-Parallel Architecture for Large-Scale Regular Expression Matching	Yusaku Kaneta, Shingo Yoshizawa, Shin-ichi Minato, Hiroki Arimura and Yoshikazu Miyanaga
	Wed	**1220**	**1240**	**Bus Line: Main Building → Zhilanyuan**	**Buses will leave at 12:40**
	Wed	**1230**	**1330**	**Lunch**	
	Wed	**1330**	**1345**	**Bus Line: Zhilanyuan → Main Building**	**Buses will leave at 13:45**
	Wed	**1400**	**1540**	**Oral Session 1.4 – Parallel Implementation and CAD**	**Chair: Masahiro Fujita**
	Wed	1400	1420	Impact of Reconfigurable Hardware on Accelerating MPI_Reduce	Shanyuan Gao, Andrew Schmidt and Ron Sass
	Wed	1420	1440	Accelerating HMMER on FPGA using Parallel Prefixes and Reductions	Naeem Abbas, Steven Derrien, Sanjay Rajopadhye and Patrice Quinton
	Wed	1440	1500	Multiple Data Set Reduction on FPGAs	Yi-Gang Tai, Chia-Tien Dan Lo and Kleanthis Psarris
	Wed	1500	1520	Accelerating FPGA Development Through the Automatic Parallel Application of Standard Implementation Tools	Athira Chandrasekharan, Sureshwar Rajagopalan, Guruprasad Subbarayan, Tony Frangieh, Yousef Iskander, Stephen Craven and Cameron Patterson

	Wed	1520	1540	Parallelizing FPGA Placement Using Transactional Memory	Steven Birk, J. Gregory Steffan and Jason Anderson
	Wed	**1540**	**1620**	**Afternoon Tea**	
	Wed	**1620**	**1800**	**Oral Session 1.5 – Multi-Core and Multi-FPGA**	**Chair: Frank Hannig**
	Wed	1620	1640	A Message-Passing Multi-Softcore Architecture on FPGA for Breadth-First Search	Qingbo Wang, Weirong Jiang, Yinglong Xia and Viktor Prasanna
	Wed	1640	1700	Deterministic Multi-Core Parallel Routing for FPGAs	Marcel Gort and Jason Anderson
	Wed	1700	1720	The TransC Process Model and Interprocess Communication	Henning Manteuffel, Cem Bassoy and Friedrich Mayer-Lindenberg
	Wed	1720	1740	Comparing Performance and Energy Efficiency of FPGAs and GPUs for High Productivity Computing	Brahim Betkaoui, David B Thomas, Wayne Luk
	Wed	1740	1800	Local-and-Global Stall Mechanism for systolic Computational-Memory Array on Extensible Multi-FPGA System	Wang Luzhou, Kentaro Sano and Satoru Yamamoto
	Wed	**1800**	**1815**	**Bus Line: Main Building → Jinchunyuan Hotel**	**Bus will leave at 18:15**
		1820	**1900**	**Welcome Function**	
		1900	**2100**	**Demo Session 1.6 - details below**	**Chair: Yu Wang**
9/12/10	**Thurs**				
	Thurs	**0740**	**0800**	**Bus Line: Jinchunyuan → Jiasuo → Main Building**	**Jinchunyuan (7:40), Jiasuo (7:50)**
	Thurs	**0800**	**0810**	**Welcome, Announcements**	
	Thurs	**0810**	**0940**	**Keynote Session 2.1**	**Chair: Peter Athanas**
	Thurs	0810	0855	**Bringing FPGA Design to Application Domain Experts**	Dr. James Truchard CEO of National Instruments
	Thurs	0855	0940	**Technology Issues Facing the World's Largest Integrated Circuits**	Prof. Stephen Brown Altera Corporation; University of Toronto
	Thurs	**1000**	**1100**	**Morning Tea, Poster Session 2.2, see details below**	
	Thurs	**1100**	**1230**	**Oral Session 2.3 – Arithmetic**	**Chair: Philip Leong**
	Thurs	1100	1120	Floating-point exponential functions for DSP-enabled FPGAs	Florent de Dinechin and Bogdan Pasca
	Thurs	1120	1140	Modular Design of Fully Pipelined Accumulators	Miaoqing Huang and David Andrews
	Thurs	1140	1200	Efficient implementation of Parallel BCD Multiplication in LUT-6 FPGAs	Alvaro Vazquez and Florent de Dinechin
	Thurs	1200	1220	High-Performance Implementation of Matrix Multiplication on FPGAs	Guiming Wu, Yong Dou and Miao Wang
	Thurs	1220	1230	FPT2011 Announcement	Tulika Mitra
	Thurs	**1230**	**1245**	**Bus Line: Main Building → Zhilanyuan**	**Buses will leave at 12:45**
	Thurs	**1230**	**1330**	**Lunch**	
	Thurs	**1330**	**1345**	**Bus Line: Zhilanyuan → Main Building**	**Buses will leave at 13:45**
	Thurs	**1350**	**1530**	**Oral Session 2.4 – Robust and Secure Computing**	**Chair: Tulika Mitra**
	Thurs	1350	1410	Fine-Grained Characterization of Process Variation in FPGAs	Haile Yu, Qiang Xu and Philip Leong

	Thurs	1410	1430	A Stochastic Method for Security Evaluation of Cryptographic FPGA Implementations	Michael Kasper, Werner Schindler and Marc Stöttinger
	Thurs	1430	1450	Fine-grain Fault Diagnosis for FPGA Logic Blocks	Stavros Tzilis, Ioannis Sourdis and Georgi N. Gaydadjiev
	Thurs	1450	1510	A Robust Reconfigurable Logic Device Based on Less Configuration Memory Logic Cell	Qian Zhao, Yoshihiro Ichinomiya, Yasuhiro Okamoto, Motoki Amagasaki, Masahiro Iida and Toshinori Sueyoshi
	Thurs	1510	1530	Compact Implementations of BLAKE-32 and BLAKE-64 on FPGA	Jean-Luc Beuchat, Eiji Okamoto and Teppei Yamazaki
	Thurs	**1530**	**1600**	**Afternoon Tea**	
	Thurs	**1600**	**1720**	**Oral Session 2.5 - Applications**	**Chair: Manfred Glesner**
	Thurs	1600	1620	Lightweight DPA Resistant Solution on FPGA to Counteract Power Models	Yingxi Lu, Philip Hodgers, Kean Hong Boey and Maire O'Neill
	Thurs	1620	1640	An FPGA-Based Text Search Engine for Approximate Regular Expression Matching	Yuichiro Utan, Shin'ichi Wakabayashi and Shinobu Nagayama
	Thurs	1640	1700	Real-time Detection of Line Segments on FPGA	Jianyun Zhu and Tsutomu Maruyama
	Thurs	1700	1720	True Random Number Generation in Block Memories of Reconfigurable Devices	Tim Gueneysu
	Thurs	**1730**	**1800**	**WALK TO DINNER**	**About 5 min; Follow the guide**
	Thurs	**1830**	**2130**	**CONFERENCE DINNER (Banquet)**	
10/12/10	**Fri**				
	Fri	**0740**	**0800**	**Bus Line: Jinchunyuan → Jiasuo → Main Building**	**Jinchunyuan (7:40), Jiasuo (7:50)**
	Fri	**0800**	**0810**	**Welcome, Announcements**	
	Fri	**0810**	**0855**	**Keynote Session 3.1**	**Chair: Wayne Luk**
	Fri	0810	0855	**In Search For Better Silicon And Human Efficiency**	Dr. Albert Wang Stretch Company
	Fri	0900	1000	Announcement of Design Competition Winners & Talk by Sponsor	Dr. Qiang Liu
	Fri	**1000**	**1100**	**Morning Tea, Poster Session 3.2, see details below**	
	Fri	**1100**	**1220**	**Oral Session 3.3 – Routing and Scheduling**	**Chair: Lesley Shannon**
	Fri	1100	1120	Obstacle-free Two-dimensional Online-Routing for Run-time Reconfigurable FPGA-based Systems	Dirk Koch, Christian Beckhoff and Jim Torrison
	Fri	1120	1140	The Effect of Multi-bit Based Connections on the Area Efficiency of FPGAs Utilizing Unidirectional Routing Resources	Omesh Mutukuda, Andy Ye and Gul Khan
	Fri	1140	1200	ATB: Area-Time Response Balancing Algorithm for Scheduling Real-Time Hardware Tasks	Xabier Iturbe, Khaled Benkrid, Tughrul Arslan, Imanol Martinez and Mikel Azkarate
	Fri	1200	1220	Dynamic Scheduling Monte-Carlo Framework for Multi-Accelerator Heterogeneous Clusters	Anson H.T. Tse, David B. Thomas, K.H. Tsoi and Wayne Luk
	Fri	**1230**	**1245**	**Bus Line: Main Building → Zhilanyuan**	**Buses will leave at 12:45**
	Fri	**1230**	**1330**	**Lunch**	

	Fri	**1330**	**1345**	**Bus Line: Zhilanyuan → Main Building**	**Buses will leave at 13:45**
	Fri	**1400**	**1530**	**Oral Session 3.4 – Special Session**	**Chair: Yongxin Zhu**
	Fri	1400	1415	Multi-dimensional Packet Classification on FPGA: 100 Gbps and Beyond	Yaxuan Qi, Jeffrey Fong, Weirong Jiang, Bo Xu, Yibo Xue, Jun Li and Viktor Prasanna
	Fri	1415	1430	Automatic Synthesis of Processor Arrays with Local Memories on FPGAs	Guiming Wu, Yong Dou and Miao Wang
	Fri	1430	1445	GVE: Godson-T Verification Engine for Many-core Architecture rapid prototyping and debugging	Zhengmeng Lei, Lunkai Zhang, Fenglong Song, Shibin Tang, Dongrui Fan, Yongbin Zhou and Xiao Xiao
	Fri	1445	1500	Synthesis of a Unified Unit for Evaluating an Application-Specific Set of Elementary Functions	Liangwei Ge, Zhenan Tang, Kaiyu Wang, Ming Chao, Wencong Zou and Dong Liu
	Fri	1500	1515	A Compression Method for Inverted Index and its FPGA-based Decompression Solution	Jing Yan, Ning-Yi Xu, Zeng-Lin Xia, Bo-Jun Huang, Rong Luo and Feng-Hsiung Hsu
	Fri	1515	1530	FPGA Implementation of GZIP Compression and Decompression for IDC Services	Jian Ouyang, Hong Luo, Zilong Wang, Jiazi Tian, Chenghui Liu and Kehua Sheng
	Fri	**1530**	**1545**	**CLOSE**	
				POSTER, DEMO, PhD Session papers	
8/12/10	**Wed**	**1000**	**1100**	**Wednesday Morning Poster Session 1.2**	
				Application-specific hardware accelerator for implementing recursive sorting algorithms	Dmitri Mihhailov, Valery Sklyarov, Iouliia Skliarova and Alexander Sudnitson
				Towards an Embedded Biologically-Inspired Machine Vision Processor	Vinay Sriram, Kuen Tsoi, Wayne Luk and David Cox
				Wireless Sensors Networks Emulator Implemented on a FPGA	Jean Louis Boizard, Nadim Nasreddine, Christophe Escriba and Jean Yves Fourniols
				A Novel FPGA-based Support Vector Machine Classifier	Markos Papadonikolakis and Christos-Savvas Bouganis
				High-Throughput IP-Lookup for Dynamic Routing Tables using FPGA	Hoang Le and Viktor Prasanna
				A Novel Design Flow for Tamper-Resistant Self-Healing Properties of FPGA Devices without Configuration Readback Capability	Andre Seffrin, Sunil Malipatlolla and Sorin A. Huss
				A Novel HDL Coding Style to Reduce Power Consumption for Reconfigurable Devices	Thomas Marconi, Dimitris Theodoropoulos, Koen Bertels and Georgi Gaydadjiev
				Wire Congestion Aware Synthesis for a Dynamically Reconfigurable Processor	Takao Toi, Takumi Okamoto, Toru Awashima, Kazutoshi Wakabayashi and Hideharu Amano

				A FPGA Implementation of the Two-Dimensional Digital Huygens' Model	Tan Yiyu, Yukinori Sato, Eiko Sugawara, Yasushi Inoguchi, Makoto Ohya, Yukio Iwaya, Hiroshi Matsuoka, Takao Tsuchiy
				Reconfigurable Number Theoretic Transform Architectures for Cryptographic Applications	Gavin Xiaoxu Yao, Ray C.C. Cheung, Cetin Kaya Koc and Kim Fung Man
				An FPGA Chip Identification Generator Using Configurable Ring Oscillator	Haile Yu, Philip H. W. Leong and Qiang Xu
				FPGA Implementation of an Interior Point Solver for Linear Model Predictive Control	Juan L Jerez, George A Constantinides and Eric C Kerrigan
				General Switch Box Modeling and Optimization for FPGA Routing Architectures	Kejie Ma, Xuegong Zhou, Lingli Wang and Sheldon Tan
				Efficient Hardware task reuse and interrupt handling for FPGA-based partially reconfigurable systems	Yi Lu, Georgi Gaydadjiev and Koen Bertels
				A debugging method for repairing post-silicon bugs of high performance processors in the fields	Bijan Alizadeh and Masahiro Fujita
8/12/10	**Wed**	**1900**	**2100**	**Wednesday Evening Demo Session 1.6**	
				Integration of PSoC Technology with Educational Robotics	Jingchuan Wang and Weidong Chen
				A Graphical Programming and Design Environment for FPGA-based Hardware	Guoqiang Wang, Trung N. Tran and Hugo A. Andrade
				Using Partial Reconfiguration and High-Level Models to Accelerate FPGA Design Validation	Yousef Iskander, Stephen Craven, Athira Chandrasekharan, Suresh Rajagopalan, Guruprasad Subbarayan, Tannous Frangieh and Cameron Patterson
				FPGA-Based Video Processing for a Vision Prosthesis	Benjamin Kwek, Freddie Sunarso, Melissa Teoh, Arrian van Zal, Philip Preston and Oliver Diessel
				Reducing power consumption for Dynamically Reconfigurable Processor Array with partially fixed configuration mapping	Kazuei Hironaka, Masayuki Kimura, Yoshiki Saito, Toru Sano, Masaru Kato, Vasutan Tunbunheng, Yoshihiro Yasuda and Hideharu Amano
				Hard Macros and Rapid Prototyping for FPGA Designs	Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson and Brad Hutchings
				VMODEX: A Visualization Tool for Multi-Objective Design Space Exploration	Toktam Taghavi and Andy Pimentel
				Advanced Partial Run-time Reconfiguration on Spartan-6 FPGAs	Dirk Koch, Christian Beckhoff and Jim Torresen

				Mapping Real-life Applications on Run-time Reconfigurable NoC-based MPSoC on FPGA	Amit Singh, Akash Kumar, Thambipillai Srikanthan and Yajun Ha
9/12/10	**Thurs**	**1000**	**1100**	**Thursday Morning Poster Session 2.2**	
				Design Space Exploration for Sparse Matrix-Matrix Multiplication on FPGAs	Colin Yu Lin, Zheng Zhang, Ngai Wong and Hayden Kwok-Hay So
				Accelerating FPGA Design Space Exploration Using Circuit Similarity-Based Placement	Xiaoyu Shi, Dahua Zeng, Bryan Hu, Guihui Lin and Osmar Zaiane
				Structured ASIC: Methodology and Comparison	Sam M. H. Ho, Steve C.L. Yuen, Hiu Ching Poon, Thomas C.P. Chau, Yan Qing Ai, Philip H.W. Leong, Oliver C.S. Choy and Kong-Pang Pun
				OpenPipes: making distributed hardware systems easier	Glen Gibb and Nick McKeown
				Design Space Exploration of Instruction Schedulers for Out-of-Order Soft Processors	Kaveh Aasaraai and Andreas Moshovos
				An Area-efficient Dynamically Reconfigurable Spatial Division Multiplexing Network-on-Chip with Static Throughput Guarantee	Zhiyao Joseph Yang, Akash Kumar and Yajun Ha
				A VLIW Softcore Processor with Dynamically Adjustable Issue-slots	Fakhar Anjam and Stephan Wong
				An FPGA implementation of full-search variable block size motion estimation	Shuichi Asano, Zheng Zhi Shun and Tsutomu Maruyama
				A Multiported Register File with Register Renaming for Configurable Softcore VLIW Processors	Fakhar Anjam, Stephan Wong and Faisal Nadeem
				ABACUS: A configurable framework for investigating workload execution on multicore processors	Eric Matthews, Lesley Shannon and Alexandra Fedorova
				Performance Estimation Framework for FPGA-based Processors	Yan Lin Aung, Siew Kei Lam and Thambipillai Srikanthan
				Evaluation of FPGA Design Guardband Caused by Inhomogeneous NBTI Degradation Considering Process Variations	Yabuuchi Michitarou and Kazutoshi Kobayashi
				Efficient Implementation of Greyscale Morphological Filters	Donald Bailey

				A Many Processing Element Framework for the Discrete Fourier Transform	Andrew van der Byl, Michael Inggs and Richardt H. Wilkinson
				Acceleration of Control Flow on CGRA using Advanced Predicated Execution	Kyuseung Han, Jong Kyung Paek and Kiyoung Choi
10/12/10	**Friday**	**1000**	**1100**	**Friday Morning Poster Session 3.2**	
				Efficient FPGA Implementation of CIOQ Switches with Sequential Iterative Matching Algorithms	Xiaojun Yang, Christoforos Kachris and Manolis Katevenis
				On Identifying Instruction Sequences for Dynamic Compilation	João Bispo and João Cardoso
				A datapath classification method for FPGA-based scientific application accelerator systems	Yui Ogawa, Tomonori Ooya, Yasunori Osana, Masato Yoshimi, Yuri Nishikawa, Akira Funahashi, Noriko Hiroi, Hideharu Amano, Yuichiro Shibata and Kiyoshi Oguri
				Efficient Custom Instructions Generation for System-Level Design	Huynh Phung Huynh, Yun Liang and Tulika Mitra
				Histogram Based Probability Density Function Estimation on FPGAs	Suhaib A. Fahmy
				A parallel FPGA design of the Smith-Waterman traceback	Zubair Nawaz, Muhammad Nadeem, Hans van Someren and Koen Bertels
				Routing Optimizations for Component-based System Design and Partial Run-time Reconfiguration on FPGAs	Dirk Koch and Jim Torresen
				An Approach to Solve Exact Cover Problems on FPGA and its Application to Sudoku	Michael Dittrich and Thomas Preußer
				GE3: a single chip client-server architecture for Golomb ruler derivation	Pavlos Malakonakis, Euripides Sotiriades and Apostolos Dollas
				An FPGA-based Scalable Platform for High-Speed Malware Collection in Large IP Networks	Sascha Mühlbach and Andreas Koch
				FPGA Based Soft-core SIMD Processing: A MIMO-OFDM Fixed Sphere Decoder Case Study	Xuezheng Chu and John McAllister
				A Deeply Pipelined and Parallel Architecture for Denoising Medical Images	Frank Hannig, Moritz Schmid, Hritam Dutta, Jürgen Teich and Heinz Hornegger

SEU Tolerant SRAM for FPGA Applications	Sudipta Sarkar, Anubhav Adak, Dr. Virendra Singh, Dr. Kewal Saluja and Dr. Masahiro Fujita
Design Automation for Accelerating Applications on FPGA-Based Clusters	Qiang Liu, Tim Todman, Kuen Hung Tsoi and Wayne Luk
A 64-context MEMS optically reconfigurable gate array	Yuichiro Yamaji and Minoru Watanabe
Minimalistic Architecture for Reconfigurable Audio Beamforming	Dimitris Theodoropoulos, Georgi Kuzmanov and Georgi Gaydadjiev