Fundamentals of Signal and Power Integrity

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… and many others!
Abstract

This presentation will give an introduction to the fundamentals of signal and power integrity engineering for high-speed digital systems with a focus on packaging aspects. The presentation is intended for an audience that has little or no formal training in electromagnetic theory and microwave engineering.

Topics that will be addressed include lumped discontinuities, transmission line effects, crosstalk, bypassing and decoupling, via and power plane effects, return current issues, and measurement techniques for Gbps links.

More information on current research projects at the Institute of Electromagnetic Theory can be found at:

http://www.tet.tuhh.de/
A Bird’s Eye View on SI, PI & EMC
Signal Transmission Issues:
Attenuation, Reflection, Dispersion, Interference, Crosstalk
Signal Transmission Issues:

Attenuation, Reflection, Dispersion, Interference, Crosstalk
A Bird‘s Eye View on SI, PI & EMC

Power Delivery Issues:
Voltage Drop, Switching Noise, Crosstalk
A Bird’s Eye View on SI, PI & EMC

Power Delivery Issues:

Voltage Drop, Switching Noise, Crosstalk
Electromagnetic Compatibility Issues:
Near Field Coupling, Radiated Emissions
Electromagnetic Compatibility Issues:
Near Field Coupling, Radiated Emissions
SI + PI + EMC = “Electrical Integrity”
Outline

(1) Hamburg and TUHH
(2) Signal Integrity
(3) Power Integrity
(4) Vias and Return Currents
(5) Measurement Techniques
(6) Wrapping Up
(1)

Hamburg and TUHH
Hamburg University of Technology

TUHH
Technische Universität Hamburg-Harburg

Founded 1978
Approx. 6000 Students
Approx. 100 Faculty Members
Hamburg University of Technology

Technische Universität Hamburg-Harburg
\[ \nabla \cdot \vec{D} = \rho \]
\[ \nabla \cdot \vec{B} = 0 \]
\[ \nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \]
\[ \nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \]

Maxwell's Equations

Printed circuit board layout
(2)

Signal Integrity
Electrical Integrity of Digital Systems
Packaging of Digital Systems

- Housing / Chassis
  - IC (Transmitter)
  - IC (Receiver)
  - Package / Module
  - Connector
  - Cable
  - Daughtercard
  - Backplane / Motherboard
  - Socket
  - Daughtercard

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Packaging of Digital Systems
The **ideal interconnect** will simply delay the signal:

Any **real interconnect** will additionally change timing and amplitude:
Effect of Interconnects

The deviations in timing and amplitude are in general called:

1. Timing jitter or simply: **JITTER**
2. Amplitude noise or simply: **NOISE**
Signal Bandwidth

\[ f_{\text{max}} \approx \frac{1}{\pi T_R} \approx 0.3 \ldots 0.5 \]

rise time

Maximum Frequency

\[ f_0 = \frac{1}{2T_B} = 0.5 \]

bit period

Fundamental Frequency
Maintaining Signal Integrity

1. Match terminations
2. Manage discontinuities
3. Reduce Coupling
4. Limit attenuation
5. Equalize signals
Effect of Terminations

Let’s use the following interconnect (link) model:
Transmission Lines in Digital Systems

Microstrip Line

\[ Z_0 \approx \frac{87 \Omega}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left( \frac{5.98 \cdot h}{0.8 \cdot w + t} \right) \]

(h = height of dielectric, 
\( w = \) conductor width, 
\( t = \) conductor thickness)

Stripline (symmetric)

\[ Z_0 \approx \frac{60 \Omega}{\sqrt{\varepsilon_r}} \cdot \ln\left( \frac{1.9 \cdot h}{0.8 \cdot w + t} \right) \]

(h = height of dielectric, 
\( w = \) conductor width, 
\( t = \) conductor thickness)
Transmission Lines in Digital Systems

Typical trace length
$\approx 5 - 75 \text{ cm}$

Velocity of propagation
$\approx 150 \, 000 \text{ km/s}$

Operating frequency
$\approx 5 \text{ GHz}$

Corresponding wavelength
$\approx 3 \text{ cm}$

... up to 25 wavelengths on a trace!
Effect of Terminations

Let’s use the following interconnect (link) model:

\[ \frac{u_2}{u_0} = \text{const. and max.}! \]
Effect of Terminations

\[ a = \frac{Z_0}{Z_S + Z_0} \]

input acceptance
Effect of Terminations

\[ H = \exp(-\gamma \cdot l) \]

\[ Z_{S}, Z_{0}, \gamma, l \]

input acceptance  TL transfer function
Effect of Terminations

\[ r_L = \frac{Z_L - Z_0}{Z_L + Z_0} \]

\[ t_L = 1 + r_L \]

input acceptance

TL transfer function

load transmission

load reflection
Effect of Terminations

\[
\begin{align*}
  r_S &= \frac{Z_S - Z_0}{Z_S + Z_0} \\
  t_S &= 1 + r_S
\end{align*}
\]

- **Source transmission**
- **Load transmission**
- **Input acceptance**
- **TL transfer function**
- **Source reflection**
- **Load reflection**
Effect of Terminations

\[ \frac{u_2}{u_0} = \frac{a \cdot H \cdot t_L}{1 - H^2 \cdot r_L \cdot r_S} = ?? \]
Effect of Terminations

\[ Z_L = Z_0 \quad \Rightarrow \quad \frac{u_2}{u_0} = a \cdot H \]

\[ Z_S = Z_L = Z_0 \quad \Rightarrow \quad \frac{u_2}{u_0} = \frac{1}{2} \cdot H \]
Effect of Terminations

Matched interconnect:

Mismatched Interconnect:

- Lossless transmission line
- Lossy transmission line
- Low source impedance
- High source impedance

Time
Voltage

$T_D$

$2 \cdot T_D$
Effect of Terminations

1. $Z_s = 10\Omega$, $Z_0 = 50\Omega$, $Z_L = 1k\Omega$
   zero losses

2. $Z_s = 50\Omega$, $Z_0 = 50\Omega$, $Z_L = 100\Omega$
   zero losses

3. $Z_s = 50\Omega$, $Z_0 = 50\Omega$, $Z_L = 50\Omega$
   zero losses

4. $Z_s = 100\Omega$, $Z_0 = 50\Omega$, $Z_L = 100\Omega$
   zero losses

5. $Z_s = 10\Omega$, $Z_0 = 50\Omega$, $Z_L = 1k\Omega$
   non-zero losses

6. $Z_s = 50\Omega$, $Z_0 = 50\Omega$, $Z_L = 50\Omega$
   non-zero losses

(all lines have a delay of 0.1 ns)
Matching Terminations

- Check your interconnect length \((2 \cdot T_D > T_R)\)!
- Check your interconnect impedance!
- Match receiver input impedance!
- Match transmitter output impedance!
The technology is typically CMOS with the links being voltage mode, unidirectional, serial, point-to-point, and source-synchronous. For improved bandwidth equalization is typically used in the Tx, Rx, or both.
Packaging of Digital Systems

Interconnect (Link)
Effect of Lumped Discontinuities

\[ u_1 \text{ Source Voltage} \rightarrow 50 \Omega \rightarrow 2.5 \text{ nH} \rightarrow 50 \Omega \rightarrow u_2 \text{ Received Voltage} \]

Signal In \hspace{1cm} Signal Out

Tx-Output \hspace{1cm} Bond Wire \hspace{1cm} Rx-Input
Effect of Lumped Discontinuities

Source Voltage \( u_1 \) → 50 Ω → 1 pF → 50 Ω → Received Voltage \( u_2 \)

Signal In → Via → Signal Out

Tx-Output → Via → Rx-Input
Effect of Lumped Discontinuities

- Attenuation of high frequency signal components
- „Slowing down" of the edges of a digital signal

\[ \frac{u_2(t)}{u_1(t)} \]

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>Time [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_0 \approx 6.37 \text{ GHz} )</td>
<td>( \tau = \frac{1}{\omega_0} = 25 \text{ ps} )</td>
</tr>
</tbody>
</table>
Effect of Distributed Discontinuities

\[ Z_0 \rightarrow Z, \gamma, l \rightarrow Z_0 \]

1 inch, 45 Ohm mismatched transmission line at \( c_0 /2 \)

\[ f = \frac{c}{4 \cdot l} = 2.952 \text{GHz} \]

Frequency Response
(Scattering Parameters)
Overall Effect of Discontinuities

Magnitude of S-Parameters [dB]

Frequency [GHz]

Step Response [Volt]

Time [ps]

2nH

Z=49
P=1cm

300fF

2nH

Z=48
P=15cm

300fF

2nH

Z=52
P=5cm

300fF

2nH

Z=48
P=1cm

300fF

0 0 0 0

Port1 Port2

Z=49
P=1cm

300fF

2nH

Z=48
P=15cm

300fF

Z=52
P=5cm

300fF

Z=48
P=1cm

2nH
Managing Discontinuities

- Avoid them!
- Check their impact!
- Minimize them ($\pm 10$ Ohm around 50 Ohm)!
- Compensate them (difficult)!
- Concentrate on the “bottleneck!”
Packaging of Digital Systems

Interconnect (Link)
Effect of Coupling

Consider two transmission lines in close proximity:

1. Input
2. Output
3. Near End
4. Far End

Aggressor Line (Active Line)
Victim Line (Quiet Line)
Effect of Coupling

Consider two transmission lines in close proximity:

(1) Input

(2) Output

(3) Near End

(4) Far End

**NEXT** = Near End Crosstalk
(sum of ind. and cap. crosstalk)

**FEXT** = Far End Crosstalk
(difference of ind. and cap. crosstalk)
Effect of Coupling

For weak coupling \((k_{L,C} \leq 0.25)\) it is found approximatively:

(1) Input

\[
U_{\text{INPUT}}^{\text{max}}
\]

(2) Output

Effect of crosstalk is usually small.

(3) Near End

Polarity is equal to input polarity.

(4) Far End

Polarity also depends on coupling coefficients.
Effect of Coupling

For weak coupling \((k_{L,C} \leq 0.25)\) it is found approximatively:

\[
U_{\text{NEXT}}^{\text{max}} = \begin{cases} 
\frac{k_C + k_L}{2} \cdot \frac{T_D}{T_R} \cdot U_{\text{INPUT}}^{\text{max}} & (T_D < 0.5 \cdot T_R) \\
\frac{k_C + k_L}{4} \cdot U_{\text{INPUT}}^{\text{max}} & (T_D > 0.5 \cdot T_R) 
\end{cases}
\]

\[
U_{\text{FEXT}}^{\text{max}} = \frac{k_C - k_L}{2} \cdot \frac{T_D}{T_R} \cdot U_{\text{INPUT}}^{\text{max}}
\]

It should be noted that these formulas do not take into account losses on the lines or reflections from load mismatches.
Example for Coupling Coefficients

For two thin wires above infinite ground one can find:

\[ k_C = \frac{C'_{12}}{C'_{11} + C'_{12}} \approx \frac{\ln(1 + (2h/a)^2)}{2 \cdot \ln(4h/d)} \]
Reducing Coupling

- Increase line separation!
- Decrease distance to ground!
- Balance capacitive and inductive coupling!
- Increase rise time!
- Reduce coupling length!
- Use differential signaling!
In a **SINGLE-ENDED** link there is a common (global) reference against which the signal is measured ("ground").

In a **DIFFERENTIAL** link the reference is the negative of the signal itself (which has to be transmitted as well).
(3)

Power Integrity
Electrical Integrity of Digital Systems
Effect of Common Power Delivery

$U_0 \rightarrow Z_{PDN} \rightarrow IC \#1 \rightarrow IC \#2$

$PDN = \text{Power Delivery Network}$
Effect of Common Power Delivery

\[ \Delta u(t) = R \cdot \left[ i_{\text{Gate1}}(t) + i_{\text{Gate1}}(t) + \ldots \right] + L \cdot \frac{d}{dt} \left[ i_{\text{Gate1}}(t) + i_{\text{Gate1}}(t) + \ldots \right] \]

"DC-drop or IR-drop"

"\(\Delta l\)-drop or \(\Delta l\)-noise"

\[ u_{\text{IC}} = U_0 - \Delta u \]
Maintaining Power Integrity

1. Decrease PDN impedance
2. Add decoupling
3. Add even more decoupling
4. Use several power supplies
5. Use on-chip VRMs
PDN Elements

High Power DC Supply

Discrete Decoupling Capacitors (various sizes)

IC incl. Power/Ground Grid & Integrated Decaps

Package incl. Power/Ground Planes

Voltage Regulator Module

Printed Circuit Board incl. Power/Ground Planes
PDN Impedance

In frequency domain the standard PDN model looks like this:

\[ Z_{PDN}(f) \]

\[ u_0 \]

\[ \Delta u(f) \]

\[ Z_{IC}(f) \]

\[ |\Delta u(f)| \leq \Delta u_{max} \]

\[ \left| Z_{PDN}(f) \right| \leq Z_{Target} \]

\[ f \in \text{"operating frequency range"} \]
A typical maximum ripple for digital systems is:

\[
\frac{\Delta u_{\text{max}}}{u_0} = \text{maximum ripple } \leq 5\% \text{ to } 10\%
\]

With a 10% value the following numbers can be obtained for applications … of the early 1990’ies: … of 2000 and on:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>(u_0)</td>
<td>5.0 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>(i_{\text{avg}})</td>
<td>1 A</td>
<td>120 A</td>
</tr>
<tr>
<td>(u_0 / i_{\text{avg}})</td>
<td>5.0 Ω</td>
<td>0.01 Ω</td>
</tr>
<tr>
<td>(P_{\text{avg}})</td>
<td>5 W</td>
<td>144 W</td>
</tr>
<tr>
<td>(Z_{\text{Target}})</td>
<td>0.5 Ω</td>
<td>0.001 Ω</td>
</tr>
</tbody>
</table>

\[Z_{\text{Target}} = 0.001\Omega = 1\ m\Omega!\]
Is 1 mΩ hard to achieve? How about 10 mΩ? Let’s see …

Example:

The PDN consists of a simple copper wire of 2 mm radius in the form of a flat rectangle with side lengths of 5 cm and 1 cm, respectively.

\[ |Z_{PDN}| = \sqrt{R^2 + (\omega L)^2} \]

with \( R \approx 0.7 \) mΩ \( L \approx 40 \) nH

It turns out that 10 mΩ cannot be maintained beyond 40 kHz!
Decreasing PDN Impedance

- Use adequate copper cross sections!
- Avoid big current loops!
- Use power/ground planes!
- Provide enough power/ground pins!
- Decouple!
Decoupling

Based on the simple example from before:

\[ Z_{PDN} = R + j\omega L \]
\[ \approx j\omega L \]
(for large \( \omega \))

\( R = 0.7 \) m\( \Omega \),
\( L = 40 \) nH

\[ Z_{IC}(f) \]
Decoupling

... we ask what a so called "decoupling" or "bypass" capacitor does:

\[
\begin{align*}
Z_{PDN} &= \frac{R + j\omega L}{1 + j\omega RC - \omega^2 LC} \\
&\approx \frac{1}{j\omega C} \quad \text{(for large } \omega) \\
\end{align*}
\]

\[R = 0.7 \text{ m}\Omega\]
\[L = 40 \text{ nH}\]
\[C = 1 \text{ mF}\]
Decoupling

Heuristic explanation:

**Frequency domain:** Beyond the resonance frequency the capacitor decouples the part of the PDN that lies "left" of him, i.e. the IC sees only the impedance of the capacitor.

**Time domain:** The capacitor stores charges close to the IC that can become currents needed for fast switching. It is like a "small battery".
Decoupling

While being beneficial at higher frequencies decoupling increases the PDN impedance in the vicinity of the resonance frequency:

\[ \omega_0 = \frac{1}{L} \sqrt{\frac{L}{C} - R^2} \quad (L/C \geq R^2) \]

\[ \rightarrow \quad Z_{PDN}(\omega_0) = \frac{1}{R} \cdot \frac{L}{C} \geq R \]

Hence, increasing the "damping" (by increasing \( R \) and/or reducing \( L/C \)) can be helpful:

\[ (\text{with} \quad Q = \frac{1}{R \cdot \sqrt{L/C}} \quad \text{the condition becomes} \quad Q \geq 1) \]
Real Word Decoupling Capacitors

Unfortunately, there is no ideal capacitor available in the real world!

Ideal world:                        … and real world:

R is also called the **EQUIVALENT SERIES RESISTANCE (ESR)** and L the **EQUIVALENT SERIES INDUCTANCE (ESL)**.

As a consequence any real world capacitor behaves approximately like an inductor beyond its resonance frequency:

\[ \omega_0 = 1/\sqrt{LC} \]
More Decoupling

- Speed of charge delivery, effective frequency
- Amount of charge, size of decoupling capacitance

board-level  package-level  chip-level
Power/Ground Planes

Power/ground planes serve multiple purposes at the same time:

➔ easy access to power and ground domains for mounted components
➔ a "natural" decoupling capacitor for PDN improvement
➔ return current paths, i.e. they serve as reference conductors
➔ shielding between different signal layers, i.e. they reduce crosstalk
➔ containment for internal EM fields, i.e. reduce EM emission

... HOWEVER ...

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Power/Ground Planes

... they do show a resonant behavior:

Dielectric Filling ($\varepsilon_r = 4$)

$$C_{pp} = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d} \approx 11 \text{ nF}$$

(1 inch = 2.54 cm, 1 mil = 0.001 inch)
Power/Ground Planes

The resonance frequencies are given by:

\[ f_{mn} = \frac{c_0}{\sqrt{\mu_r \varepsilon_r}} \sqrt{\left( \frac{m}{2a} \right)^2 + \left( \frac{n}{2b} \right)^2} \quad (m, n = 0, 1, 2, \ldots) \]

Examples of standing wave patterns on a rectangular power/ground plane pair.
Adding Decoupling

- Determine your target impedance!
- Determine your operating frequency range!
- Provide decoupling at all levels/frequencies!
- Use parallel decoupling to reduce ESR/ESL!
- Be wary of resonances!
Vias and Return Currents
The Problem With Vias

Signal Current

Signal Via

Load

Return Current

Ground Via

Load
A “Physcis-Based” Model for Vias

**Equations:**

\[
\begin{bmatrix}
 v'_{i_u} \\
 i'_{i_u}
\end{bmatrix} = \begin{bmatrix} 1 & 0 \\
1/Z_{p_u} & 1
\end{bmatrix} \cdot \begin{bmatrix}
 v_{i_u} \\
 i_{i_u}
\end{bmatrix}
\]

\[
\begin{bmatrix}
 v_{i} \\
 i_{i}
\end{bmatrix} = \begin{bmatrix} 1 & Z_{pp} \\
0 & 1
\end{bmatrix} \cdot \begin{bmatrix}
 v_{i} \\
 i_{i}
\end{bmatrix}
\]

\[
\begin{bmatrix}
 v'_{i} \\
 i'_{i}
\end{bmatrix} = \begin{bmatrix} 1 & 0 \\
1/Z_{p} & 1
\end{bmatrix} \cdot \begin{bmatrix}
 v_{i} \\
 i_{i}
\end{bmatrix}
\]

**Diagram:**

- **Current Flow:**
  - Plane to Plane
  - Plane to Via
  - Via to Plane

- **Impedance:**
  - \(Z_{pp}\): (Parallel Plate Impedance)
  - \(Z_{p}\)

- **Symbols:**
  - \(v_{i}\), \(v'_{i}\)
  - \(i_{i}\), \(i'_{i}\)
  - \(C_p\)

**Image:**

- Via Cross Section
- Plane to Plane
- Plane to Via
- Via to Plane
Where Do We Zpp Get From?

\[ Z_{ij}(\omega) = \frac{j \omega \mu d}{ab} \cdot \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \left[ C_m^2 C_n^2 \cdot \frac{\cos(k_{xm} x_i) \cdot \cos(k_{yn} y_i) \cdot \cos(k_{xm} x_j) \cdot \cos(k_{yn} y_j)}{k_{xm}^2 + k_{yn}^2 - k^2} \right] \]

\[ k_{xm} = \frac{m \pi}{a}, \quad k_{yn} = \frac{n \pi}{b}, \quad k = \omega \sqrt{\mu \varepsilon} \]

\[ C_m, C_n = 1 \text{ for } m, n = 0 \text{ and } \sqrt{2} \text{ otherwise} \]
Including Striplines

Trace between planes:

2 Modes: Stripline + Parallel Plate

Modal decomposition: find suitable transformation matrices to diagonalize MTL equations
Including Striplines

\[ k \approx - \frac{h_1}{h_1 + h_2} \]

Stacking the Deck

Decoupling capacitor model

Cavity representation

Cavity representation

S-Parameter Matrix

Cavities joined by segmentation techniques

Comparison with Full-Wave Results

6 Vias, 4 traces case
Centered striplines at two levels, and thru vias in a 6 cavity stackup

Port 1,3

Port 2,4

Full-wave model

Magnitude of $S_{12}$ [dB]

Frequency [GHz]

Model
FEM simulation
FIT simulation

Comparison with Full-Wave Results
Comparison with Measurements

Assumption of infinite plates

- 119 vias (76 signal, 43 ground)
- 14 differential striplines (2D)
- 6 cavities
- Terminations

Comp. time: < 3 min
Models capture the salient features of the hardware response despite the drastic model simplification.
Investigation of Via Return Currents

Effect of number of ground vias:

1 GND via

2 GND vias

4 GND vias

6 GND vias
Investigation of Via Return Currents

Effect of number of ground vias:

<table>
<thead>
<tr>
<th>Number of GND vias</th>
<th>Magnitude of $S_{12}$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 GND vias</td>
<td></td>
</tr>
<tr>
<td>2 GND vias</td>
<td></td>
</tr>
<tr>
<td>4 GND vias</td>
<td></td>
</tr>
<tr>
<td>6 GND vias</td>
<td></td>
</tr>
</tbody>
</table>

Frequency [GHz]
(5)

Measurement Techniques
Multiport Vector Network Analysis

Agilent Vector Network Analyzer 8364C with 12-port extension at Institute of Electromagnetic Theory (TUHH)

12 ports
Bandwidth 10 MHz – 50 GHz
Electronic calibration module
Advanced calibration software
Common Surface Launches

\[ \text{Surface Connectors} \quad \text{Access Vias} \quad \text{MICRO-PROBE} \]

\[ \text{STRUCTURE UNDER TEST} \quad 5 \text{ mm} \quad \text{STRUCTURE UNDER TEST} \quad 5 \text{ mm} \]

... but vias are usually a high frequency bottleneck!
The Recessed Probe Launch (RPL)

No access vias

→ less distortion
→ probes closer to the structure under test
RPL Error Box Extraction

Error boxes of RPLs from TRL calibration

(thru = 90 mil long, line = 220 mil long)
Problems with Via Arrays

... many vias at tight pitch!
The Interposer Concept

SMA or SMP Connectors

~ 1 cm

~ 1 mm

~ 1 cm

Signal pitch conversion from ~1 cm to ~1 mm

& easy multiport access
Typical Measurement Set-up

Multiport VNA

Interposer 1

Interposer 2

High speed serial links
Interposer Prototype

Hardware courtesy of IBM YKT (Y. Kwark)
Application to Link Measurement

Hardware courtesy of IBM YKT (Y. Kwark)

1st interposer connected to the via array

2nd interposer connected to the via array

Stripline connecting vias from both via arrays
(6)
Wrapping Up
Electrical Integrity of Digital Systems
Electrical Integrity of Digital Systems

The basic goals of EMC, SI, and PI for an electrical system are complementary to each other.

→ **SIGNAL INTEGRITY**: insure acceptable quality of signals within

→ **POWER INTEGRITY**: insure acceptable quality of power delivery within

→ **EMC**: insure acceptable level of interference with the outside
Contact Information

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