

# Oversampling Analog/Digital Converters with Finite Zeros in Noise Shaping Functions<sup>1</sup>

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## ABSTRACT

A double-input oversampling modulator (DIOM) is proposed for analog/digital converter design. The main property of the novel method is that it allows arbitrary noise shaping functions, provided that stability is assumed. Finite zeros can be introduced. For bandpass type input signal a DIOM can be designed with a much lower sampling rate than a sigma-delta modulator. The requirement on opamp settling time can thus be greatly reduced. Sensitivity behaviour of DIOMs is discussed and a multistage design example is provided.

## 1. INTRODUCTION

Sigma-delta modulators (SDMs) have attracted much attention recently for high precision analog/digital converter (ADC) design [1-12]. In an SDM the quantisation noise is processed by a feedback network. Most of the noise is pushed outside the signal band and out-band noise can be filtered out by a digital network. This greatly eases the tolerance requirement on the analog circuit part.

For an SDM the signal and the noise transfer functions are dependent on each other and they can not be chosen arbitrarily [1-7]. As a result, SDMs are normally designed to minimise the quantisation noise around DC. Although the advantage of introducing finite zeros in noise shaping functions has been considered [6,7], it can only be achieved with very a high oversampling ratio so that the influence on the signal transfer function can be ignored.

This paper proposes a novel double input oversampled modulator (DIOM) with independent noise shaping and signal transfer functions. It is particularly useful for realising finite zeros in noise shaping functions with a low oversampling ratio to ease the requirement on opamp settling time. It can also be used to improve dynamic range for multi-bit design. Sensitivity properties are discussed and a multistage design example is provided.

## 2. DOUBLE INPUT OVERSAMPLING MODULATOR (DIOM)

Consider a z-domain DIOM system shown in Fig.1a, where the comparator can be described by a linear model with an additional quantisation noise source,  $n(z)$ , Fig.1b. The signal input,  $x(z)$ , is coupled into the network through two paths and hence the name. The output,  $y(z)$  can be derived in term of  $x(z)$  and  $n(z)$  as

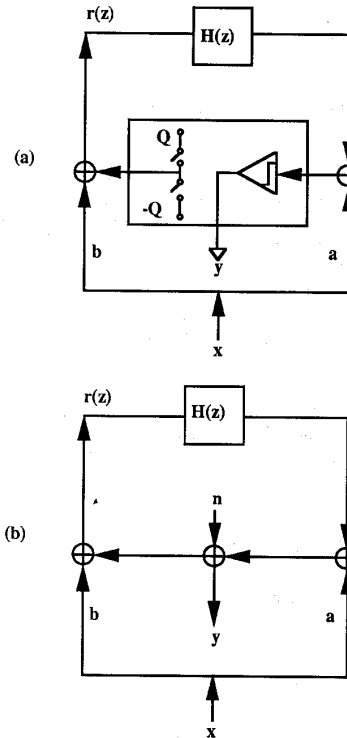


Fig. 1 (a) A double input oversampling modulator (DIOM)  
(b) The linearised model of a DIOM

<sup>1</sup> This work was partly carried out during the author's stay with Wolfson Microelectronics, Edinburgh, U.K.

$$y(z) = \frac{a + bH(z)}{1 - H(z)} x(z) + \frac{1}{1 - H(z)} n(z) \quad (1)$$

Let  $a=-1$  and  $b=1$ , then

$$y(z) = -x(z) + \frac{1}{1 - H(z)} n(z) \quad (2)$$

It can be seen that the input signal is directly fed through while the noise is weighted by  $w(z)$ , the noise shaping function, defined by

$$w(z) = \frac{1}{1 - H(z)} \quad (3)$$

Let  $H(z)$  be represented by the ratio of two polynomials as

$$H(z) = m(z)/d(z) \quad (4)$$

Denote  $\Delta(z) = d(z) - m(z) \quad (5a)$

then  $w(z) = d(z)/\Delta(z) \quad (5b)$

For a band limited signal the noise interference can be eliminated by properly selecting  $w(z)$ , such as by placing all the zeros of  $w(z)$  in the signal band. Signal and noise can then be separated in later stages of digital circuits, where lowpass and bandpass comb filters can be used.

### 3. REALISATION CONSIDERATIONS

If all the zeros of  $w(z)$  are placed at DC and one bit quantisers are used, the behavior of a DIOM is very much the same as an SDM.

If multi-bit quantisers are used [8,9], there is a significant advantage in adopting the DIOM scheme. It can be verified that the level of the feedback signal,  $r(z)$ , is very close to the level of the quantisation residual. Actually the input signal through branch b would exactly cancel the output of the quantiser were there no quantisation error and  $b=-a=1$ . For a multi-bit realisation the level of  $r(z)$  is small. It can be amplified to fully utilise the dynamic range of the subnetwork realising  $H(z)$ . After  $H(z)$  the signal is scaled back down by the same factor before it is added to the input through branch a. The noise produced in  $H(z)$  is thus reduced by the scaling factor, which can be set to  $2^{n-1}$  for an  $n$ -bit design.

Another notable feature of DIOM design is that the zeros of  $w(z)$  (the roots of  $d(z)$ ) can take finite values. For a second order design, these roots can be placed on the unit circle, so that,

$$\begin{aligned} d(z) &= (z - e^{+j\omega_0 T})(z - e^{-j\omega_0 T}) \\ &= 1 - 2\cos(\omega_0 T)z^{-1} + z^{-2} \end{aligned} \quad (6)$$

For realisation convenience, let

$$\alpha = 2(1 - \cos(\omega_0 T)) \quad 0 < \alpha < 4 \quad (7a)$$

so  $d(z) = 1 - (\alpha/2)z^{-1} + z^{-2} \quad (7b)$

The selection of  $m(z)$  has less impact on system behaviour and this provides freedom for efficient circuit realisation. For  $1 < \alpha < 3$ , simply let

$$m(z) = z^{-2} \quad (8)$$

From (5a), (7) and (8)

$$\Delta(z) = 1 - (2 - \alpha)z^{-1} \quad (9)$$

$\Delta(z)$  represents the denominator of a stable system. Other schemes are possible but will not be discussed.

Notice from (4) and (6) that  $H(z)$  is realised as a resonator with its resonant frequency centred at  $\omega_0$ . This is the fundamental principle of a DIOM: using a resonant network to perform negative feedback for attenuating the quantisation noise.

### 4. MULTISTAGE DESIGN

It has been found that in first and second order cases a DIOM is stable provided that  $w(z)$  represents a stable system. For higher order DIOMs instability may occur even if  $w(z)$  is a stable function.

Stable higher order DIOM systems can also be designed by a multistage approach [3]. Consider cascading two second order DIOMs (Fig.2). The input of the second modulator comes from the first stage, is given by

$$x_2(z) = \frac{H_1(z)}{1 - H_1(z)} n_1(z) = w_1(z)H_1(z)n_1(z) \quad (10)$$

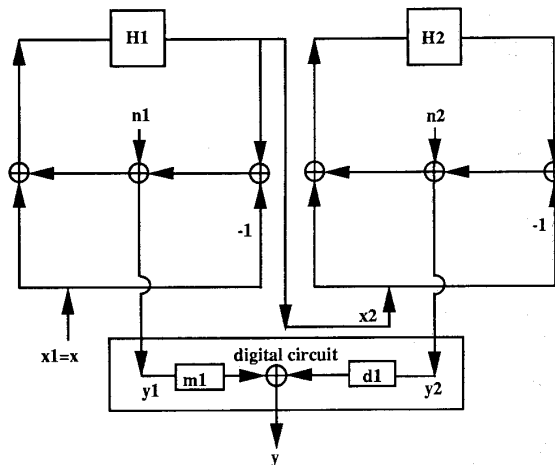


Fig.2 A two-stage DIOM

so that  $y_2(z) = -w_1(z)H_1(z)n_1(z) + w_2(z)n_2(z) \quad (11)$

$$\begin{aligned} y(z) &= m_1(z)y_1(z) + d_1(z)y_2(z) \\ &= -m_1(z)x(z) + d_1(z)w_2(z)n_2(z) \end{aligned} \quad (12)$$

A high order noise shaping function

$$w(z) = d_1(z)w_2(z) = \frac{d_1(z)d_2(z)}{\Delta_2(z)} \quad (13)$$

is obtained. Notice that if the first biquad is designed according to (8) then  $m_1(z) = z^{-2}$  is just a delay function. The same principle applies to DIOMs with more stages.

### 5. SENSITIVITY

It is seen from (1) (if  $b=-a=1$ ) that the signal transfer function is completely insensitive to most of the parameters of the network except  $a$  and  $b$ . The derivatives of the signal transfer function against  $a$  and  $b$  are,

$$\frac{d(y/x)}{da} = -w(z) \tag{14a}$$

$$\frac{d(y/x)}{db} = -1 + w(z) \tag{14b}$$

where  $w(z)$  is normally designed to be very small in the signal band. The unity term in (14b) represents only a scaling factor. The input branch of an SDM has the same effect. Therefore the signal transfer function is very tolerant to component deviations.

The finite zeros of the noise shaping function may shift due to errors in the element values. This problem does not exist if all the zeros are placed at DC as they result directly from the integration. From (7) the sensitivity of  $\omega_0$  can be derived against the deviation of  $\alpha$ ,

$$S^{\omega_0}_{\alpha} = \frac{\alpha}{\omega_0} \frac{d\omega_0}{d\alpha} = \frac{1 - \cos(\omega_0 T)}{\omega_0 T \sin(\omega_0 T)} = \frac{\tan(\omega_0 T/2)}{\omega_0 T} = \frac{\tan(\pi f_0/f_s)}{2\pi f_0/f_s} \tag{15}$$

where  $\omega_0 = 2\pi f_0$  and  $f_s$  is the sampling frequency.  $S^{\omega_0}_{\alpha}$  is monotonously increasing for  $0 < f_0/f_s < 1/2$ . For  $0 < f_0/f_s < 1/4$   $S^{\omega_0}_{\alpha}$  is small ( $< 2/\pi$ ).

### 6. DESIGN EXAMPLE

In Fig.3 an example of a two stage DIOM is shown. In each stage  $H(z)$  is realised as a second order SC resonator. The design data is as follows,

|                            |  |
|----------------------------|--|
| sampling frequency         | 66 kHz                                 |
| signal band                | 15.5 kHz to 16.5 kHz                   |
| in-band quantisation noise | < -70dB                                |
| for the first stage        | $\alpha_1 = 2.0, f_{01} = 16.5$ kHz    |
| for the second stage       | $\alpha_2 = 1.855, f_{02} = 15.75$ kHz |

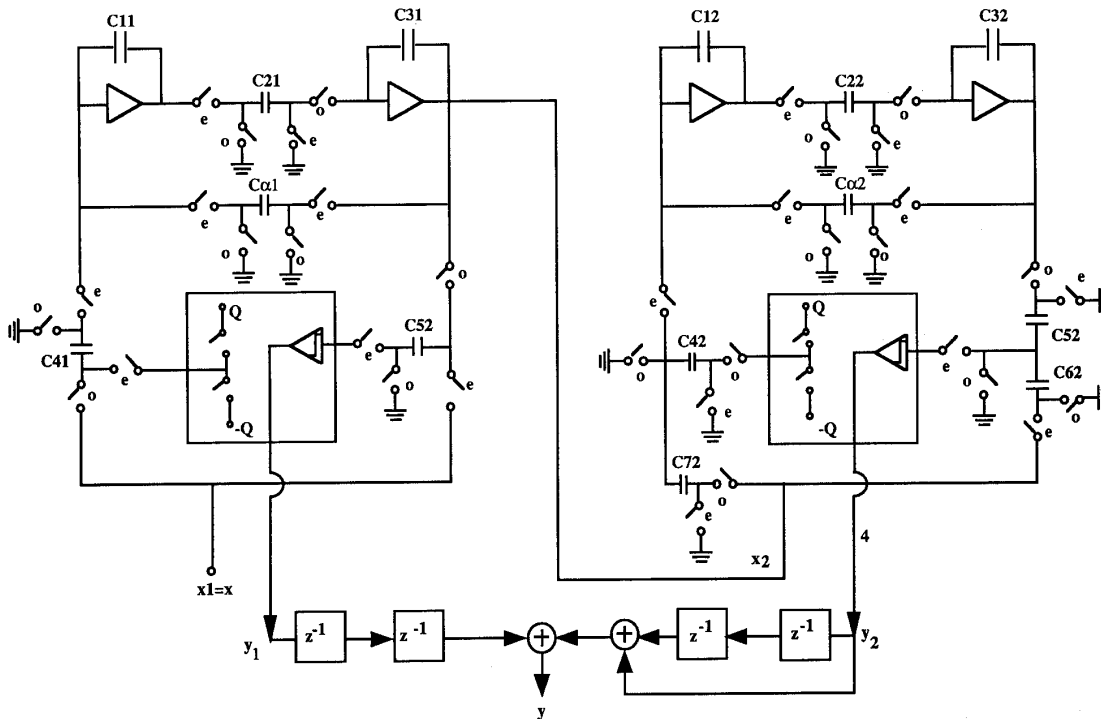


Fig.3 Switched capacitor realisation of a fourth order DIOM.  $C11=C21=C31=C41=C51=C12=C22=C32=C42=C52=1$   
 $C62=C72=0.25$   $C\alpha_1=2$   $C\alpha_2=1.855$

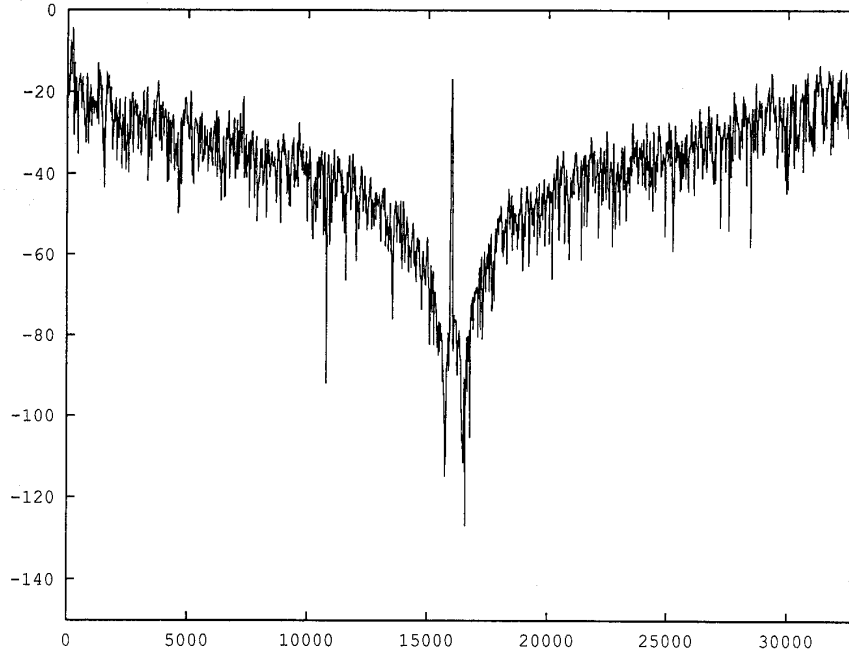


Fig.4 Simulated response of a fourth order DIOM

The input signal of the second stage is scaled by a factor of 4 to avoid overloading. A typical simulation spectrum is shown in Fig.4 with a sinusoidal input at 16 kHz. If the accuracy of the capacitor ratios can be fabricated within 0.5%, then from (15) and (16) and the relation,

$$\alpha_i = (C_{\alpha i} C_{2i}) / C_{1i} C_{3i} \quad (16)$$

for each biquadratic section the variance of  $\omega_0$  will be within 1%. It is found that this variance has only minor effect on the system behavior.

For the same application a fourth order SDM design would use a sampling rate at about 600 kHz and this would require much higher opamp settling time.

## 7. CONCLUSIONS

It has been shown that DIOMs provide a flexible means for high resolution ADC design. The principle applies similarly to DAC design.

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