SWITCHED CAPACITOR AND ACTIVE-RC ALLPASS LADDER FILTERS

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ABSTRACT

Ladder based allpass filters are derived for active-RC, SC and digital realisations. The resulting circuits have the attractive properties of parallel structures and very low amplitude sensitivities. The implementations are canonical with respect to the number of opamps or delays and multipliers. Examples are given and these are critically assessed for component spread and sensitivities.

INTRODUCTION

Allpass filters are primarily designed to provide phase characteristics and any interference with an existing magnitude response should be avoided. However in practical realisations the amplitude response will inevitably be influenced by component variations. A novel low sensitivity method for allpass digital ladder design has been recently proposed [1,2]. This paper presents a further investigation of a family of canonical active-RLC, active-RC and SC allpass ladders. An improved allpass digital structure is also described which is canonical with respect to both multipliers and delays. It is demonstrated that sensitivities of the amplitude responses of ladder systems are much lower than those of the cascade biquad structures. Low capacitance spreads are also observed for ladder based methods.

CONTINUED FRACTIONS OF ALLPASS FUNCTIONS

For convenience only even order designs will be considered.

The s-domain formulae

An allpass function in the s-domain has the form,

$$H_a(s) = \pm P(-s)/P(s) \tag{1}$$

where P(s) is a Hurwitz polynomial. Separate P(s) into even and odd parts

$$P(s) = EvP(s) + OdP(s) \tag{2}$$

Substitute (2) into (1) and rearrange [1]

$$H_a(s) = 1 - \frac{2}{1+EvP(s)/OdP(s)} = 1 - \frac{2}{1+Y(s)} \tag{3}$$

It is well known that if P(s) = EvP(s) + OdP(s) is Hurwitz then Y(s) = EvP(s)/OdP(s) can be expanded as continued fractions [3]

$$Y(s) = sC_1 + \cfrac{1}{sL_1 + \cfrac{1}{\ddots \; sC_m + \cfrac{1}{sL_m}}} \tag{4}$$

The z-domain formulae

An allpass function in the z-domain has the form

$$H_a(z) = - z^n P(z^{-1})/P(z) \tag{5}$$

Rearrange (5) to get

$$H_a(z) = 1 - \cfrac{1+z}{1 + \cfrac{zP(z) + z^n P(z^{-1})}{P(z) - z^n P(z^{-1})}} = 1 - \frac{1+z}{1+Y(z)} \tag{6}$$

$$\text{Define } \Psi = z^{-1}/(1-z^{-1}) \quad \Phi = 1/(1-z^{-1}) \tag{7}$$

The continued fraction expansion of Y(z) can be achieved in terms of Ψ^{-1} and Φ^{-1} alternately [4]

$$Y(z) = \Psi^{-1}C_1 + \cfrac{1}{\Phi^{-1}L_1 + \cfrac{1}{\ddots \; \Psi^{-1}C_m + \cfrac{1}{\Phi^{-1}L_m}}} \tag{8}$$

Notice a different form of (8) has been given in [1].

Eqs.(3) and (7) can be realised by the scheme shown in Fig.1, where the transfer function 1+Y(s) or 1+Y(z) can be synthesised by a singly terminated LC ladder, shown in Fig.2. In the z-domain the admittance $y_i = \Psi^{-1}C_1$ and impedance $z_i = \Phi^{-1}L_i$ are physically unrealisable, but they can be used as prototypes for SC and digital simulations.

ALLPASS LADDER DESIGN

Active RLC and RC allpass ladder synthesis

For the active-RLC scheme shown in Fig.2 the amplitude response has very low sensitivity and only a canonical number of reactance elements are required. The summing amplifier and several resistors are an extra cost.

Let the ladder section of Fig.2 be described by nodal equations

$$(sC + s^{-1}\Gamma + G) V = -gv_{in} \tag{9}$$

The matrix decomposition method for active-RC network design described in [5,6] can be readily applied here. Eq.(9) can be written in the LUD form

$$W = - (s^{-1}\Gamma + G)V - gv_{in} \tag{10a}$$

$$V = s^{-1}C^{-1} W \tag{10b}$$

Eqs.(10) are linearised with respect to s^{-1} so that they can be realised directly by active-RC circuits. For a 6^{th} order circuit, the signal flow graph (SFG) of Fig.3 (Case A) and the simulation circuit, Fig.4 (incorporating the summation stages) can be obtained.

SC and digital allpass ladder synthesis

A nodal description can also be set up for the ladder section of Fig.2 in terms of Ψ and Φ. The nodal equation has the form

$$(\Psi C + \Phi\Gamma + G) V = -(1+z)gv_{in} \tag{11}$$

Left-LUD SC and digital circuits are obtained by rewriting (11)

$$W = - (\Phi\Gamma + G)V - \alpha g v_{in} \tag{12a}$$

$$V = C^{-1} (\Psi W - \beta g v_{in}) \tag{12b}$$

where α=2, β=1. This can be again represented by a SFG, Fig.3 (Case B), including the output stage. Notice the corresponding digital implementation is canonical with respect to both multiplier coefficients and delays. The SC realisation is straightforward but this method results in a large capacitance spread. There is another realisation of (11), by choosing α=1+z and β=0, Fig.3 (Case C) results. Note the (1+z) term is non-causal and can be avoided by multiplying (7) through by z^{-1} to give $z^{-1}+(1+z^{-1})/(1+Y)$. Also note that α and b can be exchanged without affecting the overall transfer function. The corresponding SC circuit is shown in Fig.5. The single z^{-1} of the above sheme has been realised by a rearrangement of switching in the sample-and-hold and other input/output circuitry. The sampled input from an even phase is transferred to the output summing amplifier in the subsequent odd phase. The unit delay is realised when the output is sampled in the even phase of the next clock period. This scheme usually results in lower capacitance spread.

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The summing amplifier employed in the output stage in Figs.4, 5 need not be realised explicitly in delay equalised filter systems. Provided that the allpass filter is succeeded by an amplitude filter stage, the virtual ground of the input integrator of the amplitude stage can be directly connected to P_v to realise the summation function. Thus realisations with a canonical number of opamps are possible.

Other realisations, such as leapfrog, can be derived by employing different matrix decompositions [5].

SENSITIVITY ESTIMATES

It can be shown that coefficient truncation does not influence the allpass property of the digital ladder [1]. For analogue cases, inaccuracies in the values of $\{C_i\}$, $\{L_i\}$ and all the unity valued elements Figs.2-5 will affect the sensitivity, so these are more complicated cases. It will be proved that the amplitude response of the circuit of Fig.4 is completely insensitive with respect to deviation in most element values. Similar arguments can be established for other circuits (e.g., Figs.2,5).

Remark: ***For the circuit in Fig.4 provided that a, b, α and d are fixed then $|H_a|=1$ regardless of all the other parameters, even the unity valued elements.***

Proof: The transfer functions of Fig.4 have the form

$$\left| \frac{v_{out}}{v_{in}} \right| = \left| \frac{a+(b\alpha-ad)v_1/J_1}{1 - dv_1/J_1} \right| \tag{13}$$

with a=b=1, d=-1, α=-2 it is easily seen that $|H_a|=1$ if v_1/J_1 is imaginary. For the SFG in Fig.3, apply Mason's formula [7] to derive v_1/J_1,

$$v_1/J_1 = g_k/\Delta \sum_{\text{all forward paths}} (g_k\Delta_k) \tag{14}$$

$$\text{with } \Delta=1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \dots \tag{15}$$

where g_k is the product of edge weights for kth forward path;P_{mr} is the product of loop transmissions for the mth set of vertex-disjoint feedback loops; Δ_k is the value of Δ for the part of the graph having no vertices in common with the kth forward path.

Every loop in the subnetwork of the reactive two port in Fig.3 (also Fig.4) involves exactly one Ψ term and one Φ term. In the s-domain, $\Psi\Phi = (j\omega)^{-2} = -\omega^{-2}$ and therefore $P_{mr} = \Pi(\Psi/C_i)(-\Phi/L_j)$ will be real , so will Δ and all $\{\Delta_k\}$. There is only one forward path from J_1 to v_1, $g_1 = \Psi/C_1 = j\omega/C_1$, hence from (14) v_1/J_1 is imaginary and $|H_a|=1$. Notice this imaginary property of v_1/J_1 is solely structural and not affected by deviation of any parameter.

EXAMPLES AND COMPARISONS

A 6th order allpass SC filter is designed to achieve an equi-ripple correction of the delay distortion caused by a 6th order SC bandpass filter using the PANDDA software package [8]. The design data given in Table 6.1 relates to an LUD equaliser structure, Fig.5. It can be followed by the amplitude stage with the delay response shown in Fig.6. The circuits have been scaled for maximum dynamic range. The following formula is used to measure the overall system sensitivity

$$S = \{ \Sigma [(c_i/|H|)(\partial|H|/\partial c_i)]^2 \}^{1/2} \tag{16}$$

The system delay sensitivity can be defined in the same way. A leapfrog circuit and two cascade biquad allpass SC circuits using biquad Topologies 1 and 2 of [9] respectively were also designed. A comparison is provided in Fig.7 and Table 2. It is seen that ladder based structures demonstrate the significant advantages of very low sensitivity and moderate capacitance spread.

CONCLUSIONS

Novel ladder circuits have been proposed for active-RC, SC and digital allpass filter design. They have direct application in delay equalisation and also in the realisation of general amplitude functions by a sum of allpass functions [10].

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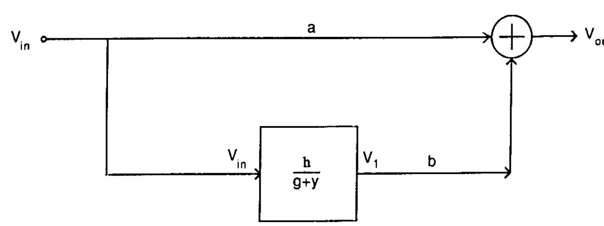
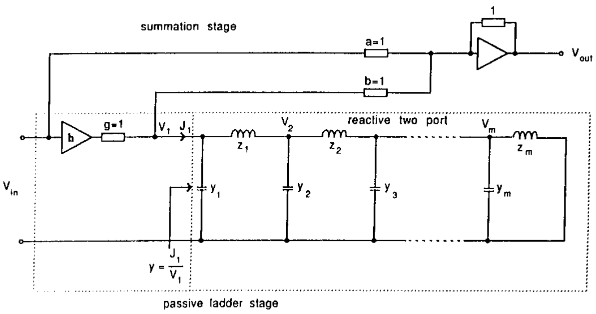


For s-domain a = b = g = 1 h = - 2

For z-domain a = b = g = 1 h =-(1 + z)

Fig. 1. Realisation of allpass function

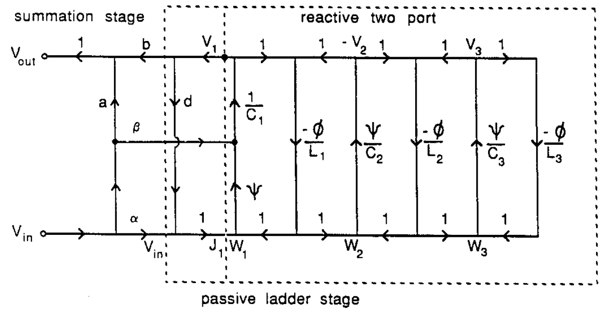


$z_i = \Phi^{-1} L_i \qquad y_i = \Psi^{-1} C_i$

For s-domain $\quad \Psi = s^{-1} \quad \Phi = s^{-1} \quad h = -2$

For z-domain $\quad \Psi = z^{-1}/(1-z^{-1}) \quad \Phi = 1/(1-z^{-1}) \quad h = -(1+z)$

Fig. 2. Active-RLC allpass circuit



Case A: in s-domain,

$\Psi = s^{-1} \quad \Phi = s^{-1} \quad a = b = d = g = 1 \quad \alpha = -2g \quad \beta = 0$

Case B: in z-domain

$\Psi = z^{-1}/(1-z^{-1}) \quad \Phi = 1/(1-z^{-1}) \quad a = b = d = g = 1 \quad \alpha = -2 \quad \beta = -1$

Case C: in z-domain

$\Psi = z^{-1}/(1-z^{-1}) \quad \Phi = 1/(1-z^{-1}) \quad a = \alpha = d = g = 1 \quad b = -(1+z) \quad \beta = 0$

Fig. 3. An LUD type SFG for allpass realisation

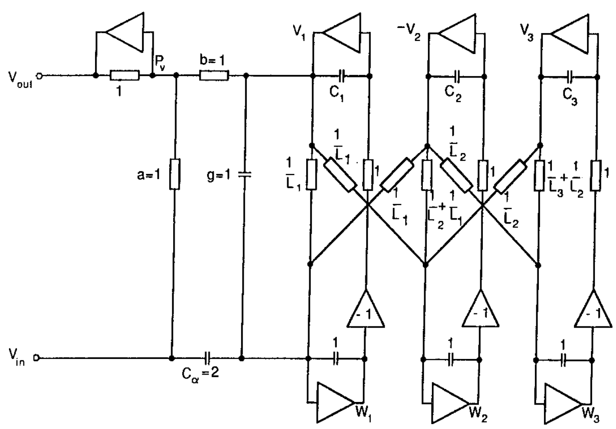


Fig. 4 An LUD type active-RC allpass filter (elements in μF and μS)

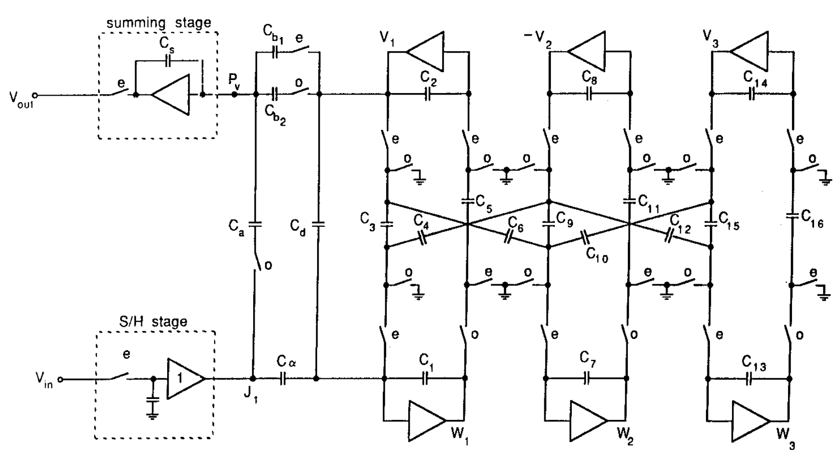


Fig. 5. An LUD type SC allpass filter

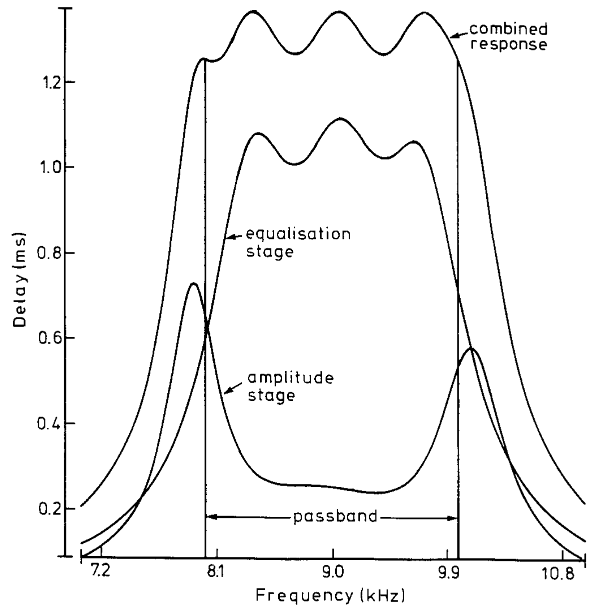


Fig. 6. Delay response of the equalised SC filter system

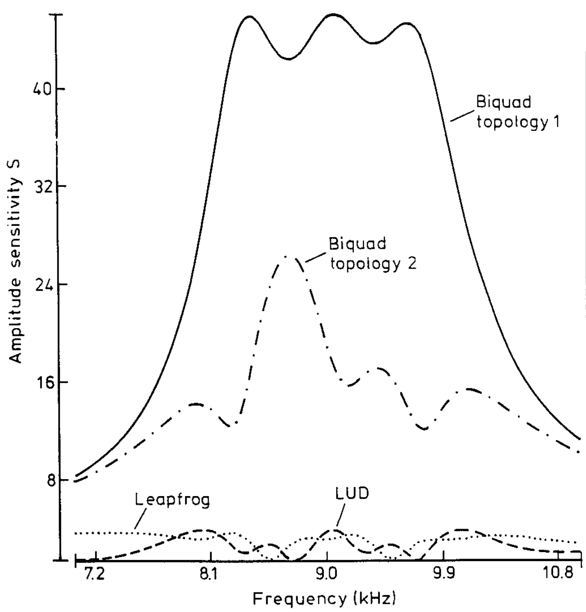


Fig. 7a. Amplitude sensitivities of equalisers

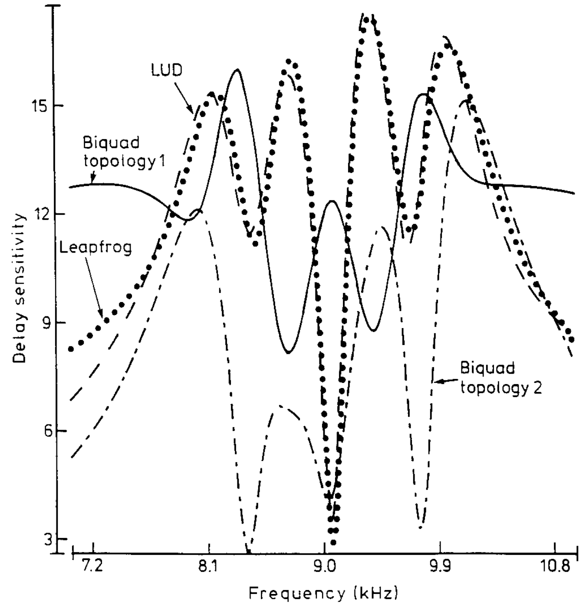


Fig. 7b. Delay sensitivities of equalisers

Specification for delay equaliser

lower equalisation edge	8000Hz	upper equalisation edge	10000Hz
approximation type	equi-ripple	in-band ripple	< 0.00014sec
filter order	6	sample frequency	150000Hz

Poles of normalised allpass transfer function in s-domain

$-0.0518242 + j1.01293$	$-0.0518242 - j1.01293$
$-0.0482866 + j1.08983$	$-0.0482866 - j1.08983$
$-0.0458278 + j0.93370$	$-0.0458278 - j0.93370$

Component values for the LUD SC ladder

Ca	1.000	Cb1	1.023	Cb2	1.023	Cc	2.333	Cd	2.386		
C1	9.903	C2	2.380	C3	3.273	C4	1.000	C5	1.000	C6	1.011
C7	24.22	C8	2.478	C9	8.660	C10	1.000	C11	1.000	C12	1.000
C13	29.29	C14	2.651	C15	10.99						

total capacitance	109 units	capacitance spread	29 units
number of switches	27	number of capacitors	21
number of opamps	6		

Table 1. Design data for SC delay equalisers

	LUD	Leapfrog	Biquad top. 1	Biquad top. 2
total capacitance	109 units	138 units	102 units	311 units
capacitance spread	29 units	29 units	26 units	62 units
number of opamps	6	6	6	6
number of switches	27	28	32	32
number of capacitors	21	21	24	24

The S/H and summation stages are excluded

Table 2. Comparison of various SC delay equalisers