Iterative Decoding of Multi-Dimensional Concatenated Single Parity Check Codes[1]

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Abstract

This paper is concerned with the decoding technique and performance of multi-dimensional concatenated single-parity-check (SPC) code. A very efficient sub-optimal soft-in-soft-out decoding rule is presented for the SPC code, costing only 3 addition-equivalent-operations per information bit. Multi-dimensional concatenated coding and decoding principles are investigated. Simulation results of rate 5/6 and 4/5 3-dimensional concatenated SPC codes are provided. Performance of BER=10^{-4}~10^{-5} can be achieved by the MAP and Max-Log-MAP decoders, respectively, with E_b/N_0 only 1 and 1.5 dB away from the theoretical limits.

I. Introduction

Recently it has been shown that concatenated coding schemes using relatively simple constituent convolutional or block codes can achieve performances close to the theoretical limits [1-4]. The MAP (maximum *a posteriori*) soft-in-soft-out decoding algorithm [5] together with the iterative decoding strategy are essential for such schemes. The trellis based MAP algorithm has been adopted in most related work so far [1-4]. Although the trellis approach is also applicable to block codes [5,6], more efficient alternative soft-in-soft-out algorithms can be developed in many cases, as shown in this paper and in some related work [7-9].

The single parity check (SPC) code [10] is one of the simplest codes. The concatenated SPC codes have been considered by many authors [11,12] and it has been shown that high performance coding schemes can be devised using the multi-dimensional concatenation technique. In this paper we will introduce a very efficient sub-optimal soft-in-soft-out decoding rule for the SPC code, which costs only 3 addition-equivalent-operations per information bit (AEO/IB). This is compared with 20 AEO/IB required by the equivalent trellis based sub-optimal approach [13]. We will also propose a modular multidimensional turbo-type decoder structure which has demonstrated very good convergence property. The decoder structure is also applicable to other concatenated codes [9].

Simulation results of rate 5/6 and 4/5 3-dimensional concatenated SPC codes will be provided. Performance of BER=10^{-4}~10^{-5} can be achieved by the MAP and the proposed sub-optimal decoders with E_b/N_0 1 and 1.5 dB, respectively, away from the theoretical limits.

II. MAP and Max-Log-MAP rules

Consider a binary code C with values in {-1,1}. The transmitted codeword is denoted by $\mathbf{u}=\{u[j]\}$ and the distorted signal by $\mathbf{x}=\{x[j]\}=\mathbf{u}+\mathbf{n}$, where $\mathbf{n}=\{n[j]\}$ is a vector of independent random Gaussian variables with zero mean and variance σ^2. Construct a vector $\tilde{\mathbf{L}}$ of the *a priori* probability ratios conditioned on individual received symbols [3,4],

$$\tilde{L}[j] = \log\left(\frac{\Pr\{u[j]=+1\}}{\Pr\{u[j]=-1\}}\right) = \log\left(\frac{\exp\left(\frac{-(x[j]-1)^2}{2\sigma^2}\right)}{\exp\left(\frac{-(x[j]+1)^2}{2\sigma^2}\right)}\right) = \frac{2x[j]}{\sigma^2} \quad (1)$$

Assume that all the codewords in C have independent and equal probability of occurrence. The output of an MAP soft-in-soft-output decoder can be described by [3-5],

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$$L[j] = \log \frac{\sum_{c[j]=+1} \exp(\frac{< \mathbf{c}, \tilde{\mathbf{L}} >}{2})}{\sum_{c[j]=-1} \exp(\frac{< \mathbf{c}, \tilde{\mathbf{L}} >}{2})} \quad (2)$$

where $< \mathbf{c}, \tilde{\mathbf{L}} >$ is the inner product of **c** and $\tilde{\mathbf{L}}$ and the summations are over all the codewords with c[j]=+1 and -1, respectively. To reduce the computational cost, we can approximate each of the summations in (2) by the dominant term, resulting in the so-called Max-Log-MAP decoder [4,13],

$$L[j] \approx \frac{1}{2}\left(\max_{c[j]=+1} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} - \max_{c[j]=-1} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} \right) \quad (3)$$

The maximizations are over all the codewords with c[j]=+1 and -1, respectively. The trellis approach [6,13] can be used to evaluate (3) for the SPC code which costs about 20 AEO/IB. In the following we will introduce a faster and simpler method requiring only 3 AEO/IB.

III. Efficient Max-Log-MAP soft-in-soft-out decoding rule for the SPC code

Every codeword in a SPC code considered below has an even number of -1 bits [10]. Define a vector **s**={s[j]} by $s[j]=\mathrm{sign}(|\tilde{L}[j]|)$. Clearly,

$$< \mathbf{s}, \tilde{\mathbf{L}} > = \sum_j |\tilde{L}[j]| \quad (4)$$

Denote by j_m and j_s the indices such that $|\tilde{L}[j_m]| = \min\{|\tilde{L}[j]|\}$ and $|\tilde{L}[j_s]| = \min\{|\tilde{L}[j]| : j \neq j_m\}$, i.e., $\tilde{L}[j_m]$ and $\tilde{L}[j_s]$, respectively, have the minimum and the second minimum amplitudes among the entries of $\tilde{\mathbf{L}}$. Let p be the number of -1 bits in **s**. It is easy to verify that for p even,

$$\max_{c[j]=s[j]} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} = < \mathbf{s}, \tilde{\mathbf{L}} > \quad \text{for all } j \quad (5a)$$

$$\max_{c[j]=-s[j]} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} = \begin{cases} < \mathbf{s}, \tilde{\mathbf{L}} > - 2(|L[j]| + |L[j_m]|) & \text{if } j \neq j_m \\ < \mathbf{s}, \tilde{\mathbf{L}} > - 2(|L[j]| + |L[j_s]|) & \text{if } j = j_m \end{cases} \quad (5b)$$

and for p odd,

$$\max_{c[j]=s[j]} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} = \begin{cases} < \mathbf{s}, \tilde{\mathbf{L}} > - 2|L[j_m]| & \text{if } j \neq j_m \\ < \mathbf{s}, \tilde{\mathbf{L}} > - 2|L[j_s]| & \text{if } j = j_m \end{cases} \quad (5c)$$

$$\max_{c[j]=-s[j]} \{< \mathbf{c}, \tilde{\mathbf{L}} >\} = < \mathbf{s}, \tilde{\mathbf{L}} > - 2|\tilde{L}[j]| \quad \text{for all } j \quad (5d)$$

From (5) we have the following rule for evaluating (3),

$$L[j] \approx \begin{cases} s[j](|\tilde{L}[j]| + |\tilde{L}[j_m]|) & \text{if p even and } j \neq j_m \\ s[j](|\tilde{L}[j]| + |\tilde{L}[j_s]|) & \text{if p even and } j = j_m \\ s[j](|\tilde{L}[j]| - |\tilde{L}[j_m]|) & \text{if p odd and } j \neq j_m \\ s[j](|\tilde{L}[j]| - |\tilde{L}[j_s]|) & \text{if p odd and } j = j_m \end{cases} \quad (6)$$

Ignoring the operations for taking the absolute value and negation, the complexity of the above decoding rule is 3 AEO/IB, (For a length-n SPC code with n-1 information bits, finding j_s and j_m requires 2n-3 comparisons and (6) involves n additions.)

Eqn.(5) can be compared with the Wagner rule [14] for finding $\hat{\mathbf{c}}$ that maximizes $< \mathbf{c}, \tilde{\mathbf{L}} >$ in a SPC code, i.e., $\hat{\mathbf{c}} = \mathbf{s}$ for p even and $\hat{\mathbf{c}} = \mathbf{s}'$ for p odd, with $s'[j] = s[j]$ except for $s'[j_m] = -s[j_m]$. The Wagner rule is the most efficient soft-in-hard-out decoding method for the SPC code. It costs only 1 AEO/IB while a trellis based algorithm [6] costs about 6 AEO/IB.

IV. Multi-dimensional concatenation SPC codes

High rate, high gain codes can be constructed using multi-dimensional concatenated SPC codes. We adopted the following concatenation scheme. Let **D** be an I×J array of information bits. Let $\mathbf{D}_n = \pi_n(\mathbf{D})$ be an I×J array obtained from **D** using interleaving π_n, n=1,2,..., N. The interleaver length is denoted by N_d=I×J. Apply a length J+1 SPC code row-wise to every $\mathbf{D}_n$, n=1,2...N, producing N parity check vectors {$\mathbf{P}_n$ | n=1,2...N}, Fig.1(a). The overall codeword is formed by **D** and $\mathbf{P}_1$, $\mathbf{P}_2$, ... $\mathbf{P}_N$, Fig.1(b). We call $\mathbf{D}_n\mathbf{P}_n$ the n-th dimension. The overall coding rate is R=J/(J+N).

The product codes without checks on checks [4] are special cases of the above scheme, e.g., when N=2, I=J, D_1[i,j]=D[i,j] and D_2[i,j]=D[j,i], the above scheme is equivalent to a 2-dimensional product code. However the above scheme has the advantage of allowing flexible interleaver length. The above scheme can also be regarded as an instance of the codes considered in [12]. The regular structure above facilities the design of the interleavers. Notice that the dimension in this paper is equivalent to the degree of systematic nodes used in [12].

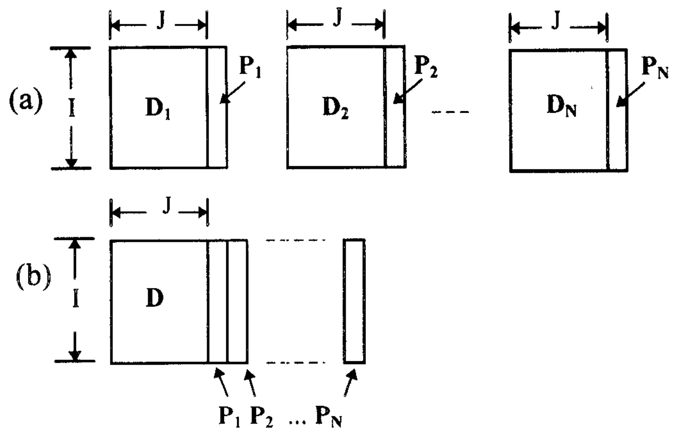

Fig.1 An N-dimensional concatenation scheme. (a) The encoding process. (b) The overall codeword.

V. Iterative decoder for multi-dimensional concatenated codes

An iterative decoding strategy for the multidimensional concatenated code is illustrated in Fig.2. The global decoder, Fig.2(a), consists of N decoding modules detailed in Fig.2(b). The block labeled by $\mathbf{F_n}$ consists of the interleaver π_n, the MAP or Max-Log-MAP decoder and the de-interleaver π_n^{-1}. Its input vector of *a priori* probability ratios in the m-th iteration can be decomposed into two parts, denoted by $\tilde{\mathbf{L}}_{\mathbf{P_n}}$ and $\tilde{\mathbf{L}}^{(m)}_{\mathbf{D_n}}$ respectively. $\tilde{\mathbf{L}}_{\mathbf{P_n}}$ is for the parity check bits in the n-th dimension and it remains unchanged throughout the decoding process. $\tilde{\mathbf{L}}^{(m)}_{\mathbf{D_n}}$ is for the information bits which is updated iteratively. The *a posteriori* ratio vector $\mathbf{L}^{(m)}_{\mathbf{D_n}}$ is generated by $\mathbf{F_n}$ for the information bits and is delivered to the next decoding module as its input. Following the turbo decoding technique [1], the extrinsic information vector is defined by

$$\mathbf{W}^{(m)}_{\mathbf{D_n}} = \mathbf{L}^{(m)}_{\mathbf{D_n}} - \tilde{\mathbf{L}}^{(m)}_{\mathbf{D_n}} \tag{7}$$

As suggested in [1], the extrinsic information should be prevented from circulating back to its generator. In the decoder in Fig.2, this is realized by subtracting the delayed values of $\mathbf{W}^{(m)}_{\mathbf{D_n}}$ in front of the MAP decoding block $\mathbf{F_n}$ as,

$$\tilde{\mathbf{L}}^{(m)}_{\mathbf{D_n}} = \mathbf{L}^{(m)}_{\mathbf{D_{n-1}}} - \mathbf{W}^{(m-1)}_{\mathbf{D_n}} \tag{8}$$

Combining (7) and (8) we have a basic relationship for the decoding module DEC-n,

$$\mathbf{L}^{(m)}_{\mathbf{D_n}} - \mathbf{L}^{(m)}_{\mathbf{D_{n-1}}} = \mathbf{W}^{(m)}_{\mathbf{D_n}} - \mathbf{W}^{(m-1)}_{\mathbf{D_n}} \tag{9a}$$

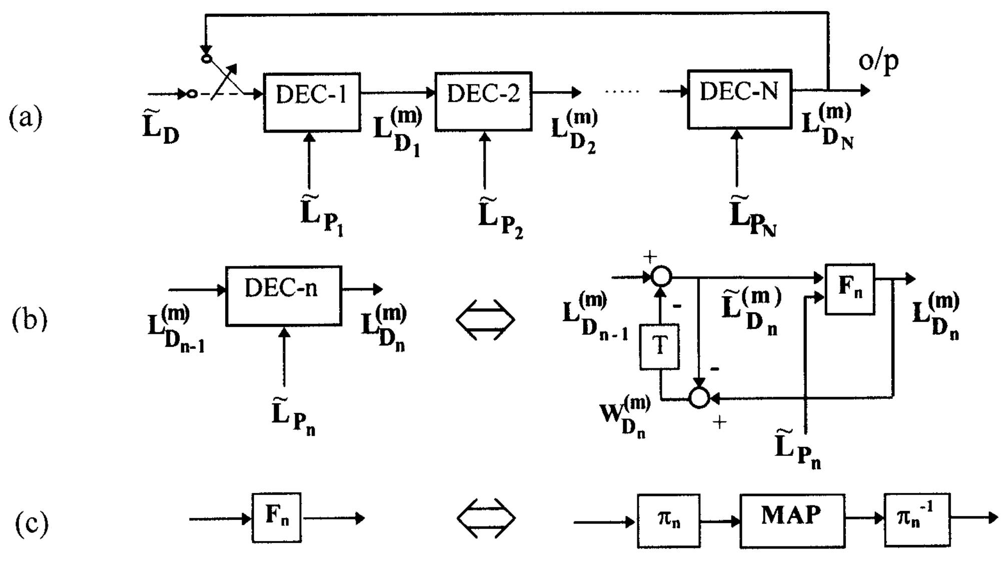

Fig.2 An N-dimensional decoder. (a) The global decoder. (b) The detailed structure of DEC-n. (c) The block labeled by $\mathbf{F_n}$ in (b) consists of a MAP decoder and an interleaver/de-interleaver pair. The MAP decoder can be approximated by a Max-Log-MAP one. T represents delay of one iteration.

with the understandings that

$$L_{D_1}^{(m)} = \begin{cases} \tilde{L}_D & \text{for } m=0 \text{ (the switch at the input position)} \\ L_{D_N}^{(m-1)} & \text{for } m>0 \text{ (the switch at the feed back position)} \end{cases} \quad (9b)$$

and

$$W_{D_n}^{(-1)}=0 \qquad n=1,2,\ldots,N \qquad (9c)$$

Eqn. (9) can be treated as a difference equation. Its solution below characterizes the decoder in Fig. 2(a),

$$L_{D_n}^{(m)} = \tilde{L}_D + \sum_{n'\le n} W_{D_{n'}}^{(m)} + \sum_{n'>n} W_{D_{n'}}^{(m-1)} \qquad (10)$$

Fig.2 represents a serial up-dating process, i.e., the N decoding modules $\{\mathbf{F}_n \mid n=1,2,\ldots N\}$ are activated in a serial manner. This is somewhat different from the multi-dimensional decoder in [3], whose characteristic function can be described by,

$$L_{D_n}^{(m)} = \tilde{L}_D + \sum_{n'\ne n} W_{D_{n'}}^{(m-1)} \qquad (11)$$

Eqn. (11) can be regarded as a parallel process in which all N decoding modules can be activated concurrently during the m-th iteration, since the left hand side of (11) depends only on the results of the (m-1)-th iteration. As indicated in [3], a damping factor is required in the iterative process based on (11). We have observed that this is not necessary for the iterative process based on (10). The good convergence property of the latter is due to the factor that the up-dating of the information ratios in (10) is carried out in a gradual, successive way. The decoder structure of Fig.2 thus represents a relatively simpler and more robust solution when a serial processor is used. The decoder structure based on (11) can be advantageous when parallel processors are available.

The decoding principle discussed above is very general and can be applied to other concatenated codes [9].

VI. Simulation results

The parameters used in our simulation are J=20 and I=500. Thus N_d=10,000. The dimensions are chosen as N=4 and 5. The equivalent full size product codes would require a huge information size of 20^4=160,000 bits and 20^5=3,200,000 bits respectively, that can be undesirable for some practical systems.

The interleavers used are described by $D_n[i,j]=D[\alpha_n(i,j), j]$ with $\alpha_n(i,j)= (i + j\times J_n) \bmod 500$. We have empirically chosen $\{J_n\}=\{0, 1, 25, 127\}$ for N=4 and $\{J_n\}=\{0, 1, 20, 480, 499\}$ for N=5. The simulation results are shown in Fig.3 and Fig.4, where the performances of the MAP decoding with 20 iterations are also included. The following can be observed for the curves with 20 iterations.

- BER of about 10^{-4}~10^{-5} can be achieved by the MAP and Max-Log-MAP decoders, respectively, at about 1 dB and 1.5 dB from the theoretical limits of SNR.
- All curves appear to converge at high E_b/N_0.
- The maximum difference between the performances of the MAP and Max-Log-MAP methods is about 0.6dB for N=5 and about 0.4 dB for N=4, respectively .
- The curves have corner points at around BER$\approx 10^{-5}$ and $E_b/N_o\approx$3dB (flattening effect). Such phenomenon has also been reported for turbo codes [2].
- For the Max-Log-MAP method most coding gain is achieved with three iterations. This has also been observed for the MAP method.

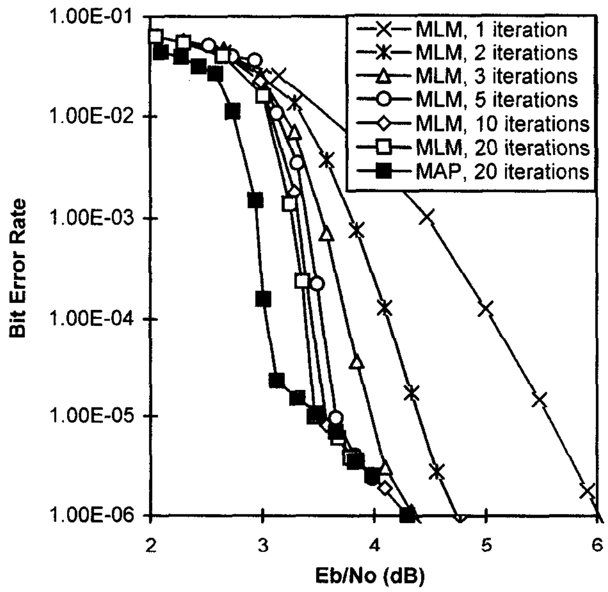

Fig.3 Simulation results for a four-dimensional parallel concatenated [21,20,2] SPC coding scheme. N=4, I=500, N_d=10,000 and rate=5/6. Theoretical limit, $E_b/N_0\approx$2.3dB. MLM stands for Max-Log-MAP.

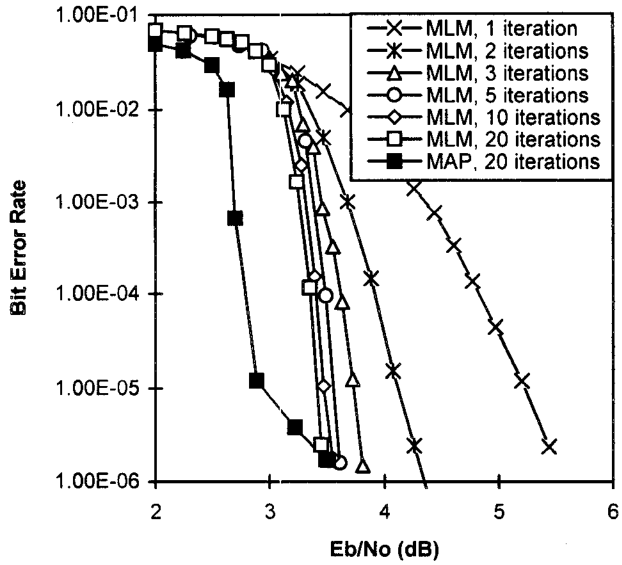

Fig.4 Simulation results for a five-dimensional parallel concatenated [21,20,2] SPC coding scheme. N=5, I=500, N_d=10,000 and rate=4/5. Theoretical limit, $E_b/N_0 \approx 2$dB. MLM stands for Max-Log-MAP.

V. Conclusion

A very low cost, sub-optimal, soft-in-soft-out decoding rule for the single parity check (SPC) codes has been presented. Multi-dimensional concatenated coding and decoding principles have been discussed. Simulation results show that the performance of BER=10^{-5} can be achieved with E_b/N_0 only 1~1.5dB away from the theoretical limits.

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References

[1] C. Berrou, A. Glavieux and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo-codes", Proc. IEEE ICC-93, pp. 1064-1070, 1993.

[2] S. Benedetto, and G. Montorsi, "Unveiling turbo codes: some results on parallel concatenated decoding schemes", IEEE Trans. Inform. Theory, IT-42, pp.409-428, March 1996.

[3] D. Divsalar and F. Pollara, "Multiple turbo codes", Proc IEEE Milcom-95, pp.279-285, 1995.

[4] J. Hagenauer, E. Offer, and L. Papke, "Iterative decoding of binary block and convolutional codes", IEEE Trans. Inform. Theory, IT-42, pp.429-445, March 1996.

[5] L. Bahl, J. Cocke, F. Jelinek and J. Raviv, "Optimal decoding of linear codes for minimizing symbol error rate", IEEE Trans. Inform. Theory, IT-20, pp.284-287, March 1974.

[6] J. Wolf, "Efficient maximum likelihood decoding of linear block codes using a trellis", IEEE Trans. Inform. Theory, IT-24, pp. 76-81, Jan. 1978.

[7] Li Ping, S. Chan and K.L. Yeung "Max-Log-MAP filtering algorithm for decoding product F_{24} code", Proc. IEEE ICC-97, pp. 1366-1370, June 1997.

[8] Li Ping, S. Chan and K.L. Yeung, "Efficient soft-in-soft-out sub-optimal decoding rule for single parity check codes", Electronic Letters, vol., 33, no. 19, pp. 1614-1616, September 1997.

[9] Li Ping and S. Chan, "Iterative decoding of concatenated Hadamard codes", in this Proceedings.

[10] B. Sklar, *Digital Communications*, Prentice Hall, 1988.

[11] J. Lodge, R. Young, P. Hoeher and J. Hagenaur, "Separable MAP "filter" for decoding of product and concatenated codes", Proc. IEEE ICC-93, pp.1740-1745, Geneva, May 1993.

[12] J.F. Cheng and R.J. McEliece, " Some high-rate near capacity codes for the Gaussian Channel", Proc. 34th Annual Allerton Conference on Communication, Control and computing, Monticello IL, Oct. 1996.

[13] P. Robertson, E. Villebrun and P. Hoeher, "A comparison of optimal and sub-optimal MAP decoding algorithms operating in the log domain", Proc. IEEE ICC-95, pp. 1009-1013, June 1995.

[14] R.A. Silverman and M. Balser, "Coding for a constant data rate source", IRE Trans. Inform. Theory, IT-4. pp.50-63, Jan. 1954.