

Active and digital ladder-based allpass filters

Li Ping, MS, PhD
 Prof. J.I. Sewell, BSc, PhD, CEng, FIEE

Indexing terms: Filters and filtering, Circuit theory and designs

Abstract: Ladder-based allpass filters are extended for active *RLC*, active *RC*, *SC* and digital realisations. The resulting circuits have the attractive properties of parallel structure and very low amplitude sensitivity to component changes. The analogue implementations are canonical with respect to the number of op amps and the digital ones are multiplier canonic. Detailed examples are given for *SC* designs and these are critically assessed for capacitance spread and sensitivity.

1 Introduction

Allpass filters are primarily designed to provide phase characteristics and any interference with an existing magnitude response should be avoided. However, in practical realisations, the amplitude response will inevitably be influenced by component variations. It is important therefore to use circuits with low amplitude sensitivity characteristics. Because allpass functions are non-minimum phase by definition, low-sensitivity ladder-based design remains an open problem. Instead, cascaded biquad sections are typical in active and digital realisations, and such topologies are highly sensitive to component deviations, especially in high-Q cases [1–3].

A novel method for allpass digital filter design has recently been proposed [4, 6]. The allpass transfer function is decomposed into two terms: a constant and a function realisable as the driving point impedance of a passive network, which is, in turn, simulated by a digital circuit. The resulting system is structurally allpass, that is, wordlength truncation will not introduce any distortion into the amplitude response. Switched capacitor (SC) simulations of the Foster II structure used in Reference 4 are also known [5].

In this paper, a ladder-based approach is presented for the design of prototypes. The op amps can be made canonical in number for SC implementations, if the allpass equaliser and amplitude filter are considered together (this can also be insured in fully differential active-*RC* circuits). The new configurations are also very suitable for parallel digital circuit implementations and lead to circuits canonical in the number of delays.

Major emphasis will be placed on SC circuit realisations. Design examples are given and comparisons made

between the different ladder-based structures and with cascade biquads. It will be demonstrated that the sensitivities of the amplitude responses of ladder systems are much lower than those of cascade biquad structures and that the sensitivities of the delay responses are similar for all realisations. Low capacitance spreads are also observed for ladder-based methods.

2 Continuous domain allpass ladders

It can be shown [6] that an allpass function in the *s*-domain

$$H_a(s) = \pm \frac{P(-s)}{P(s)} \quad (1)$$

can be rearranged as

$$H_a(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \quad (2)$$

where

$$Y(s) = \begin{cases} \frac{EvP(s)}{OdP(s)} & \text{if } n \text{ is even} \\ \frac{OdP(s)}{EvP(s)} & \text{if } n \text{ is odd} \end{cases} \quad (3)$$

for the Hurwitz polynomial

$$P(s) = EvP(s) + OdP(s) \quad (5)$$

A signal flow graph (SFG) is given in Fig. 1 for the realisation of eqn. 2, where the transfer function $1 + Y(s)$ can be synthesised by a singly terminated *LC* ladder. It is well-known that, if $P(s)$ is Hurwitz, then $Y(s) = EvP(s)/OdP(s)$ can be expanded in continued fraction form and realised according to the ladder circuit of Fig. 2.

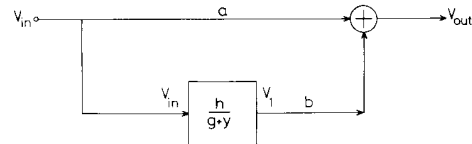


Fig. 1 Realisation of allpass function

For *s*-domain, $a = b = g = 1$, $h = -2$
 For *z*-domain, $a = b = g = 1$, $h = -(1 + z)$

Traditionally, passive allpass filters are realised as cascaded lattice-derived bridged-T structures. Two major disadvantages are associated with this method. First, the amplitude response is sensitive to all components, and, secondly, the circuits are not canonical, requiring approximately $2.5n$ reactance elements in their implementation. For the scheme shown in Fig. 2, the amplitude response is completely insensitive to the deviation in the reactance elements (Section 4) and only n reactance elements are

Paper 7531G (E10), first received 14th December 1989 and in revised form 29th May 1990

Prof. Sewell is, and Li Ping was formerly, with the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow G12 8QQ, United Kingdom

Li Ping is now with the Department of Electrical and Electronics Engineering, University of Melbourne, Parkville, Victoria 3052, Australia

required. The summing amplifier and several resistors are an extra cost.

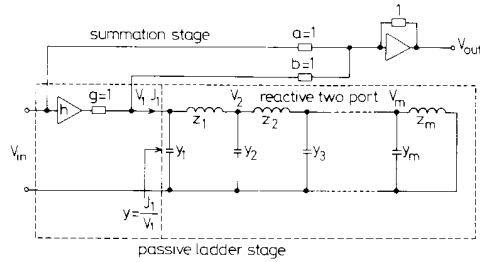


Fig. 2 Active-RLC allpass circuit
 $z_i = \Phi^{-1}L_i, y_i = \Psi^{-1}C_i$
 For s -domain, $\psi = s^{-1}, \Phi = s^{-1}, h = -2$
 For z -domain, $\psi = z^{-1}/(1 - z^{-1}), \Phi = 1/(1 - z^{-1}), h = -(1 + z)$

2.1 Active RC ladder design

The passive ladder network part of the circuit of Fig. 2 can be simulated by active RC circuits. The nodal admittance matrix equation for the passive ladder subnetwork is

$$\left(sC + \frac{1}{s} \Gamma + G\right)V = J \quad (6)$$

where $J = [-ghv_{in}, 0, \dots, 0]$ and C, Γ and G are admittance matrices formed by the contributions of capacitors, inductors and resistors, respectively. V is defined as $V = [v_1, -v_2, v_3, -v_4, \dots]$, where alternate signs are introduced to insure that all entries in eqn. 6 are positive.

The matrix decomposition method for active RC network design described in References 9-11 can be readily applied here. Eqn. 6 can be written in the LUD form, (because all of the capacitors in Fig. 2 are connected to earth, C is simply diagonal and no real decomposition of C is necessary)

$$\begin{cases} W = -(s^{-1} \Gamma + G)V + J & (7a) \\ V = s^{-1} C^{-1} W & (7b) \end{cases}$$

or, from the topological decomposition of $\Gamma = A_L D_L A_L^T$, the leapfrog form results:

$$\begin{cases} (C + s^{-1} G)V = s^{-1} (-A_L W + J) & (8a) \\ W = s^{-1} D_L A_L^T V & (8b) \end{cases}$$

Both eqns. 7 and 8 are linearised with respect to s^{-1} so that they can be realised directly with active-RC circuits. For a sixth order circuit, the signal flow graphs (SFGs) of Figs. 3a and b (case A) and the simulation circuits of Figs. 4a and b (incorporating the summation stages) can be obtained. Inversion in the output stage is incorporated in the simulation part. Notice the different termination stages in LUD and leapfrog realisations.

The summing amplifier employed in the output stage in Fig. 4 need not be realised explicitly in delay equalised filter systems. Provided the allpass filter is succeeded by an amplitude filter stage, the virtual earth of the input integrator of the amplitude stage can be directly connected to P_v to realise the summation function. In a fully differential implementation, separate inverters are not required and thus realisations with a canonical number of op amps are possible.

3 Discrete domain allpass ladders

There are several approaches to the derivation of allpass ladders in the z -domain. In particular, it has been found

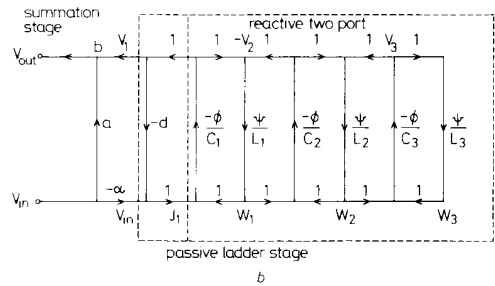
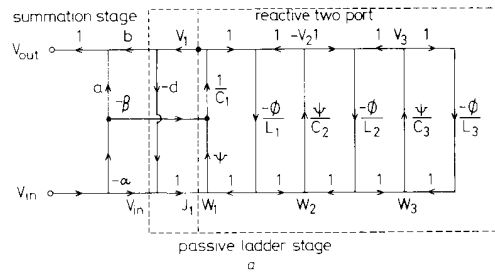


Fig. 3 SFGs for allpass realisation

- a LUD type
- Case A: s -domain
 $\Phi = \psi = s^{-1}, a = b = d = g = 1, \alpha = 2, \beta = 0$
- Case B: s -domain
 $\Phi = 1/(1 - z^{-1}), \psi = z^{-1}/(1 - z^{-1}), a = b = d = g = 1, \alpha = 2, \beta = 1$
- Case C: z -domain
 $\Phi = 1/(1 - z^{-1}), \psi = z^{-1}/(1 - z^{-1}), a = \alpha = d = g = 1, b = 1 + z, \beta = 0$
- b Leapfrog type
- Case A: s -domain
 $\Phi = \psi = s^{-1}, a = b = d = g = 1, \alpha = 2$
- Case B: z -domain
 $\Phi = 1/(1 - z^{-1}), \psi = z^{-1}/(1 - z^{-1}), b = 1 + z^{-1}, a = \alpha = d = g = 1$

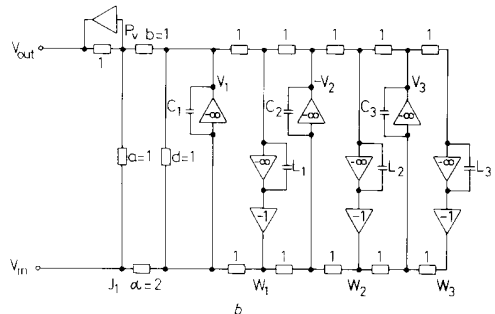
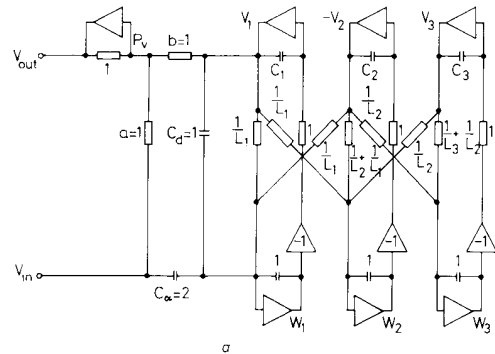


Fig. 4 Active-RLC allpass filters (elements in μF and μS)

- a LUD type
- b Leapfrog type

most efficient to use the so-called bilinear-LDI method, as it is both exact in frequency response and efficient in terms of implementation cost. Such a structure could be derived by the technique of Reference 11, which places real zeros in the ladder prototype to introduce the cancellation of capacitors after bilinear transformation. However, a more straightforward derivation is presented here, which uses a continued fraction expansion for z -domain transfer functions [6–8, 12].

3.1 LUD method for SC and digital ladder design

For an allpass function in z -domain

$$H_a(z) = \mp \frac{z^n P(z^{-1})}{P(z)} = 1 - \frac{1+z}{1 + \frac{zP(z) \pm z^n P(z^{-1})}{P(z) \mp z^n P(z^{-1})}}$$

$$= 1 - \frac{1+z}{1+Y(z)} \quad (9)$$

(– sign for $n = 2m$, + sign for $n = 2m + 1$)

To avoid the noncausal term z in eqn. 9, the transfer function is modified to

$$z^{-1}H_a(z) = z^{-1} - \frac{1+z^{-1}}{1+Y(z)} \quad (10)$$

which introduces only a single extra delay. Define

$$\Phi = \frac{1}{1-z^{-1}} \quad \Psi = \frac{z^{-1}}{1-z^{-1}} \quad (11)$$

The digital realisations of Ψ and Φ are shown in Fig. 5. The continued fraction expansion of $Y(z)$ can be achieved in terms of Ψ^{-1} and Φ^{-1} alternately [12]:

$$Y(z) = \Psi^{-1}C_1 + \frac{1}{\Phi^{-1}L_1 + \frac{1}{\Psi^{-1}C_2 + \frac{1}{\Phi^{-1}L_2 + \dots \Psi^{-1}C_m + \frac{1}{\Phi^{-1}L_m}}}} \quad (12)$$

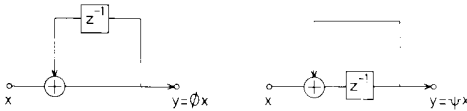


Fig. 5 Digital realisations of Φ and Ψ

For n odd, eqn. 12 will terminate with a $\Psi^{-1}C_{m+1}$ term. Positive values of $\{C_i\}$ and $\{L_i\}$ are guaranteed [12]. By analogy with eqn. 2, it can be seen that a ladder simulation is appropriate. The passive ladder part in Fig. 2 can again be used to realise eqn. 12 by means of a 'passive network', with admittance $y_i = \Psi^{-1}C_i$ and impedance $z_i = \Phi^{-1}L_i$. Although physically unrealisable, it can be used as prototype for SC and digital simulations. A nodal description can be set up for the ladder section of Fig. 2 in terms of Ψ and Φ :

$$\left(\frac{1}{\Psi}C + \Phi\Gamma + G\right)V = (1+z)J \quad (13)$$

LUD SC and digital circuits can be obtained [9–11] by rewriting eqn. 13:

$$\begin{cases} W = -(\Phi\Gamma + G)V + \alpha J & (14a) \\ V = C^{-1}(\Psi W + \beta J) & (14b) \end{cases}$$

where $\alpha = 2$, $\beta = 1$. This can be again represented by an SFG, Fig. 3a (case B), including the output stage. Notice that the corresponding digital implementation is canonical with respect to both multiplier coefficients and delays. The SC realisation is straightforward, but this method results in a large capacitance spread. There is another realisation of eqn. 13, by choosing $\alpha = 1+z$ and $\beta = 0$, Fig. 3a (case C) results. Note that α and β can be exchanged without affecting the overall transfer function. The corresponding SC circuit can be obtained by replacing the branches in the SFG by SC elements, see Fig. 6a. The single z^{-1} of eqn. 10 is realised by a rearrangement of switching in the sample-and-hold and other input/output circuitry. The sampled input from an even phase is transferred to the output summing amplifier during the subsequent odd phase. The unit delay is realised when the output is sampled in the even phase of the next clock period. This scheme usually results in a lower capacitance spread than for case B.

LUD type SC circuits will always require an even number of op amps, which is canonical for even order cases, but not for odd cases.

3.2 Leapfrog method for SC and digital ladder design

Use of 13 to derive directly the leapfrog type circuit causes difficulty in realisation of the termination terms. Instead, it is easy to verify the equivalence between eqn. 13 and the following system:

$$\left(\frac{1}{\Phi}C + \Psi\Gamma + G\right)V = z^{-1}J \quad (15)$$

where

$$C' = C - G \quad (16)$$

The right matrix decomposition structure can be derived [9–11] by rewriting eqn. 15. as

$$\begin{cases} (C' + \Phi G)V = \Phi(-A_L W + z^{-1}J) & (17a) \\ W = \Psi D_L A_L^T V & (17b) \end{cases}$$

The SFG of Fig. 3b (case B) can be used to represent eqn. 17 and an illustration of SC replacement is given in Fig. 6b, which is comparable to an independently reported realisation [7]. Notice that the z^{-1} factor in eqn. 17a cancels the noncausal factor of $1+z$ in eqn. 10.

Leapfrog SC simulation can always realise a circuit with a canonical number of op amps, provided the amplitude and allpass stages are considered together. However, for narrow band SC design, it will result in a larger total capacitance than the LUD method.

From Fig. 3b (case B), it is seen that there is a delay-free loop at the termination stage: $v_1 \rightarrow -g \rightarrow J_1 \rightarrow \Phi/c_1 \rightarrow v_1$. For a digital realisation this can be eliminated by the equivalent circuit transformation shown in Fig. 7. The resulting circuit is highly parallel

and requires only a canonical number of multipliers for digital implementation. The number of additions

varies in the values of $\{C_i\}$, $\{L_i\}$ and all unity-valued elements of Figs. 4 and 6 would affect the sensitivity.

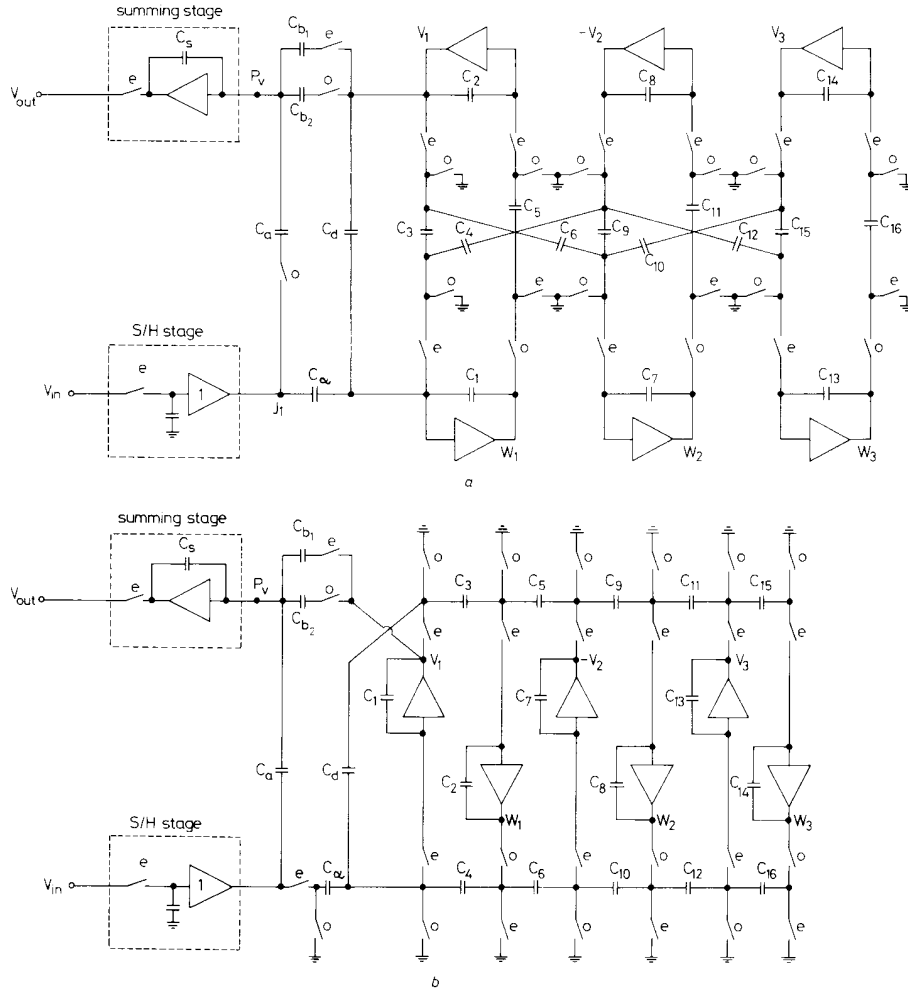


Fig. 6 SC allpass filters
a LUD type b Leapfrog type

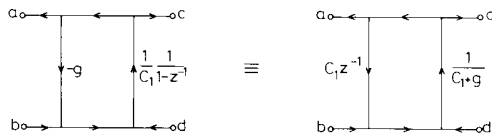


Fig. 7 Network transformation to eliminate delay-free loop

required is also relatively small (roughly $2n$). The digital leapfrog realisation requires one more delay than the equivalent canonical LUD realisation (case B).

4 Sensitivity estimations

In the fabrication process, nonideal factors will inevitably lead to deviation in the system parameters. In the digital case, the nonideal factor would be the truncation of multiplier coefficients to finite wordlength, which will affect only $\{C_i\}$ and $\{L_i\}$. For analogue cases, inaccur-

It will be proved that the amplitude response of the structures introduced in this paper, unlike their biquad counterparts, are completely insensitive with respect to deviation of most of the element values and are bounded for a few terminating elements. The transfer functions of Figs. 2, 4 and 6 have the form

$$\frac{v_{out}}{v_{in}} = H_a = \pm \left(a - \frac{b\alpha v_1/J_1}{1 + dv_1/J_1} \right) \quad (18)$$

For Figs. 2 and 4, $a = b = d = g = 1$, and $\alpha = 2$, and, for Fig. 6, $b = b_1 + b_2 z^{-1}$ and $a = b_1 = b_2 = \alpha = d = g = 1$.

Remark: For the circuits in Figs. 2, 4, and 6, if a , b (or b_1 , b_2) and α are fixed, then $|H_a| = 1$, regardless of all other parameters, even the unity valued elements.

Proof: In the s -domain (Figs. 2 and 4), eqn. 18 becomes

$$|H_a| = \left| \frac{1 - v_1/J_1}{1 + v_1/J_1} \right| \quad (19)$$

It is easily seen that $|H_a| = 1$ if v_1/J_1 is imaginary.

For the circuit in Fig. 2, v_1/J_1 is certainly imaginary, being the admittance of a reactive network.

For the circuit in Fig. 4a, we can apply the Mason formula [13] to derive v_1/J_1 :

$$\frac{v_1}{J_1} = \frac{1}{\Delta} \sum_{\text{all forward paths}} (g_k \Delta_k) \quad (20)$$

with

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \dots \quad (21)$$

where g_k is the product of edge weights for k th forward path, P_{mr} is the product of loop transmissions for the m th set of vertex-disjoint feedback loops and Δ_k is the value of Δ for the part of the graph with no vertices in common with the k th forward path.

Every loop in the subnetwork of the reactive two port in Fig. 3a (case A) involves exactly one Ψ term and one Φ term. In the s -domain, $\Psi\Phi = (j\omega)^{-2} = -\omega^{-2}$ and, therefore, $P_{mr} = \Pi(\Psi/C_i)(-\Phi/L_j)$ will be real, and so will all Δ and $\{\Delta_k\}$. There is only one forward path from J_1 to v_1 , $g_1 = \Psi/C_1 = j\omega/C_1$, hence, from eqn. 20, v_1/J_1 is imaginary and $|H_a| = 1$. A similar proof can be applied to Fig. 4b.

For the z -domain circuit of Fig. 6a, note that all Δ and $\{\Delta_k\}$ are, again, real. Referring to Fig. 3a (case C),

$$\Psi\Phi = \frac{z^{-1}}{(1-z^{-1})^2} = -\sin^2\left(\frac{\omega T}{2}\right) \quad \text{for } z = e^{j\omega T} \quad (22)$$

Since the only forward path is $g_1 = \Psi/C_1$, from eqn. 20, v_1/J_1 will have the form $v_1/J_1 = \epsilon\Psi$, with ϵ real. Hence, the following identities are derived:

$$|H_a| = \left| 1 - \frac{1+z}{1+J_1/v_1} \right| = \left| \frac{-1 + \frac{1-z}{1+z} + 2\frac{J_1/v_1}{1+z}}{1 + \frac{1-z}{1+z} + 2\frac{J_1/v_1}{1+z}} \right| = \left| \frac{-1 + \left(1 + \frac{2}{\epsilon}\right)\frac{1-z}{1+z}}{1 + \left(1 + \frac{2}{\epsilon}\right)\frac{1-z}{1+z}} \right| \quad (23)$$

As $(1-z)/(1+z) = j \tan(\omega T/2)$ is imaginary for $z = e^{j\omega T}$, one can see that $|H_a| = 1$. A similar result can be proved for the circuit in Fig. 6b.

The sensitivity formulas for the remaining elements in the circuits of Fig. 4 can be derived (since $Y(j\omega) = J_1/v_1$ is a pure imaginary number) as

$$-1 \leq \frac{a}{|H_a|} \frac{\partial |H_a|}{\partial a} = \pm \frac{1 - |Y(j\omega)|^2}{1 + |Y(j\omega)|^2} \leq 1 \quad (24a)$$

$$-2 \leq \frac{b}{|H_a|} \frac{\partial |H_a|}{\partial b} = \frac{\alpha}{|H_a|} \frac{\partial |H_a|}{\partial \alpha} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leq 2 \quad (24b)$$

$$-2 \leq \frac{d}{|H_a|} \frac{\partial |H_a|}{\partial d} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leq 2 \quad (24c)$$

Similar formulas can be derived for the circuits of Fig. 6.

5 Examples and Comparisons

The design procedure presented above has been incorporated into the filter design software package PANDDA, where cascade biquad structures are also available [14]. As an example, a sixth order allpass SC filter (case C) is designed to achieve an equiripple correction of the delay distortion caused by a sixth order SC bandpass filter, see Table 1. The design data given in Table 2 relate to the two ladder-based equaliser structures, LUD and leapfrog of Fig. 6. Each of these circuits can be followed by the amplitude stage in Fig. 8, designed as a sixth order elliptic

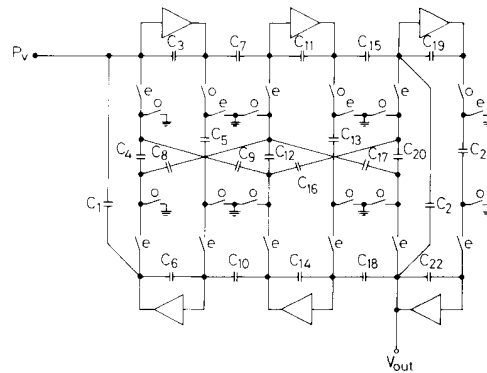


Fig. 8 Sixth order bandpass SC elliptic LUD filter

tic LUD-type SC circuit, see Table 1. All of the circuits have been scaled for maximum dynamic range. The P_i point of either circuit of Fig. 6 can be directly connected to the input of the circuit of Fig. 8. The amplitude and delay responses are shown in Figs. 9a and b.

The following formula is used to measure the overall system sensitivity:

$$S = \left\{ \sum_i \left(\frac{c_i}{|H_{ci}|} \frac{\partial |H_{ci}|}{\partial c_i} \right)^2 \right\}^{1/2} \quad (26)$$

Table 1: Design data for sixth order bandpass SC elliptic filter

Specification for amplitude filter					
Lower passband edge	8000 Hz	Upper passband edge	10000 Hz		
Lower stopband edge	7200 Hz	Upper stopband edge	10800 Hz		
Passband ripple	<0.3 dB	Stopband attenuation	>25 dB		
Approximation type	elliptic	Filter order	6		
Sampling frequency	150 000 Hz				
Component values for LUD SC ladder					
C_1	1.000	C_2	1.000	C_3	10.83
C_4	2.769	C_5	1.000	C_6	2.182
C_7	5.041	C_8	1.000	C_9	1.335
C_{10}	1.356	C_{11}	10.76	C_{12}	4.055
C_{13}	1.794	C_{14}	3.733	C_{15}	5.873
C_{16}	2.573	C_{17}	1.263	C_{18}	1.000
C_{19}	7.265	C_{20}	3.285	C_{21}	1.000
C_{22}	2.430				
Total capacitance	74 units		Capacitance spread	10 units	
Number of switches	25		Number of capacitors	22	
Number of op amps	6				

The system delay sensitivity can be defined in the same way. For comparison, two cascade biquad SC circuits are designed for the delay equalisation stage, using biquad topologies 1 and 2 of Reference 3. The resulting design

parameters are listed in Table 3. As in Reference 3, topology 1 has quite a small spread, but very high sensitivity, whereas topology 2 has an improved sensitivity at the cost of high spread, see Fig. 10. Other biquad topologies

Table 2: Design data for SC delay equalisers

Specification for delay equaliser					
Lower equalisation edge 8000 Hz			Upper equalisation edge 10000 Hz		
Approximation type equiripple			In-band ripple <0.00014 s		
Filter order 6			Sample frequency 150000 Hz		
Poles of normalised allpass transfer function in s-domain					
-0.0518242 + j1.01293		-0.0518242 - j1.01293			
-0.0482866 + j1.08983		-0.0482866 - j1.08983			
-0.0458278 + j0.93370		-0.0458278 - j0.93370			
Component values for the LUD SC ladder					
C_a	1.000	C_{b1}	1.023	C_{b2}	1.023
C_1	9.903	C_2	2.380	C_3	3.273
C_7	24.22	C_8	2.478	C_9	8.660
C_{13}	29.29	C_{14}	2.651	C_{15}	10.99
C_x	2.333	C_y	2.386	C_4	1.000
C_5	1.000	C_6	1.011	C_{10}	1.000
C_{11}	1.000	C_{12}	1.000		
Total capacitance		109 units		Capacitance spread	
Number of switches		27		29 units	
Number of op amps		6		Number of capacitors	
				21	
Component values for the leapfrog SC ladder					
C_a	1.015	C_{b1}	1.000	C_{b2}	1.000
C_1	8.878	C_2	9.546	C_3	3.289
C_7	20.34	C_8	22.19	C_9	8.305
C_{13}	29.21	C_{14}	2.660	C_{15}	1.000
C_x	1.015	C_y	1.000	C_4	3.982
C_5	1.000	C_6	1.000	C_{10}	7.565
C_{11}	1.000	C_{12}	1.000		
Total capacitance		138 units		Capacitance spread	
Number of switches		28		29 units	
Number of op amps		6		Number of capacitors	
				21	

Table 3: Comparison of various SC delay equalisers

	LUD	Leapfrog	Biquad topology 1	Biquad topology 2
Total capacitance	109 units	138 units	102 units	311 units
Capacitance spread	29 units	29 units	26 units	62 units
Number of op amps	6	6	6	6
Number of switches	27	28	32	32
Number of capacitors	21	21	24	24
S/H and summation stages excluded				

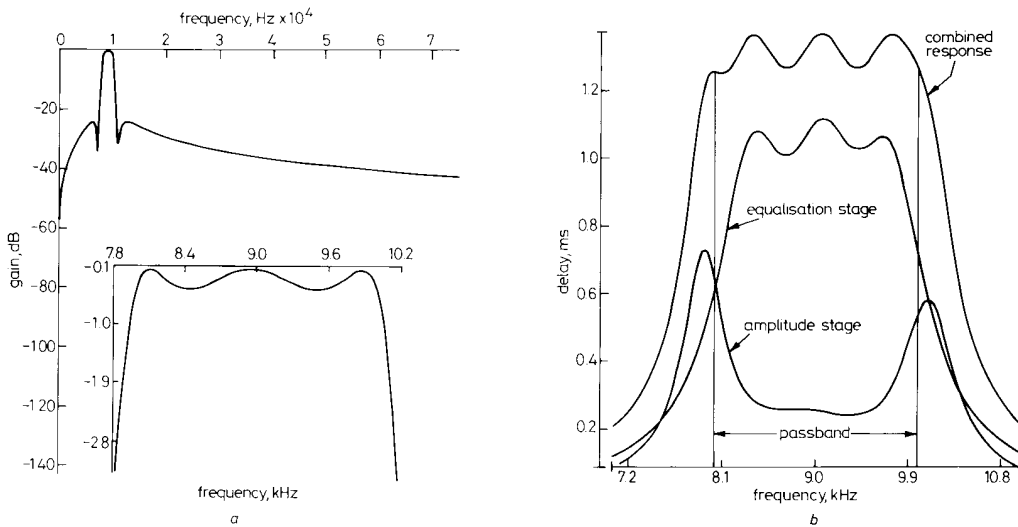


Fig. 9 SC circuit responses

a Amplitude response of sixth order SC LUD filter

b Delay response of equalised SC filter system

[3] show some tradeoff of sensitivity and spread between these two extremes. However, it is seen that ladder-based structures demonstrate the significant advantage of both low sensitivity and low capacitance spread.

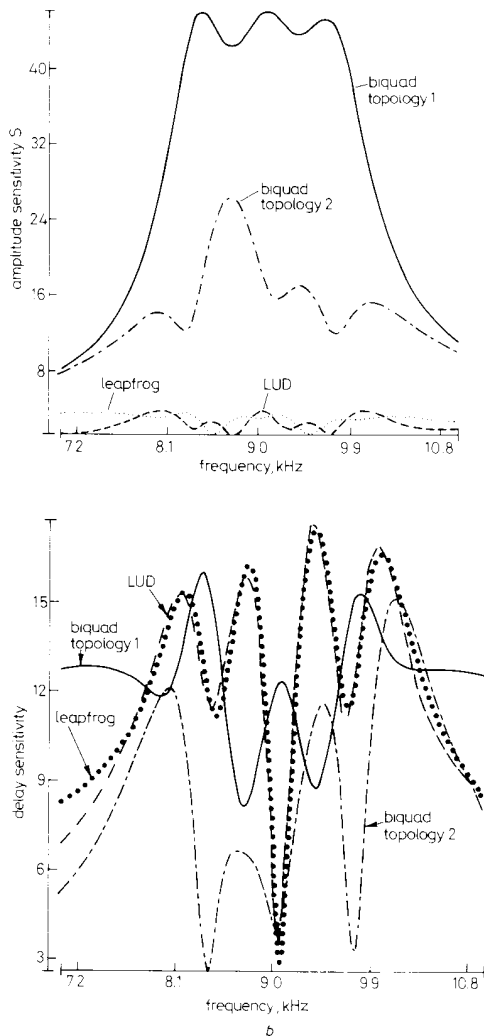


Fig. 10 Equaliser sensitivities
a Amplitude b Delay

The amplitude sensitivities for ladder-based circuits, of the type shown in Fig. 6, are mainly determined by five parameters, i.e. $a = C_a/C_s$, $b_1 = C_{b1}/C_s$, $b_2 = C_{b2}/C_s$, $\alpha = C_c/C_1$ and $d = C_d/C_1$. Provided these ratios are carefully controlled, good allpass properties can be expected.

6 Conclusions

A systematic approach has been proposed for active and digital allpass ladder-based design and novel LUD structures have been developed that demonstrate very low

amplitude sensitivity, as well as other advantages, such as high parallelism for digital realisation and low total capacitance for SC realisation. It is shown that LUD ladder-based structures can be implemented with a canonical number of multipliers and delays for digital circuits or with a canonical number of op amps for analogue circuits.

A formal sensitivity analysis of the ladder-based all pass structures has indicated that amplitude sensitivities are strictly bounded, and this is confirmed by detailed examination of example circuits.

The allpass ladder-based networks have direct application in delay equalisation and also in the realisation of general amplitude functions by a sum of allpass functions [15] to achieve low-sensitivity and low-noise properties.

7 Acknowledgements

The authors wish to thank R.K. Henderson for his invaluable help and suggestions. Helpful discussions with B. Nowrouzian are also gratefully acknowledged.

8 References

- 1 SEDRA, A.S., and BRACKETT, P.Q.: 'Filter theory and design: active and passive'. Matrix, Portland OR, USA, 1978
- 2 GHAUSI, M.S., and LAKER, K.R.: 'Modern filter design: active RC and switched-capacitor' (Prentice-Hall, Englewood Cliffs, New Jersey, USA, 1981)
- 3 LAKER, R.K., GANESAN, A., and FLEISCHER, P.E.: 'Design and implementation of cascaded switched-capacitor delay equalizers', *IEEE Trans.*, 1985, **CAS-32**, (7), pp. 700-711
- 4 NOWROUZIAN, B., and LEE, L.S.: 'Minimal multiplier realisation of bilinear-LDI digital allpass networks', *IEE Proc. G. Circuits, Devices and Systems*, 1989, pp. 114-117
- 5 SVIHURA, M.J., and NOWROUZIAN, B.: 'A new approach to the design of bilinear-LDI switched-capacitor filters having low pass-band sensitivities'. Proceedings of IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, Canada, June 1989, pp. 193-197
- 6 NOWROUZIAN, B., and BRUTON, L.T.: 'Novel approach to the exact design of digital LDI allpass networks', *Electron. Lett.*, 1989, **25**, (22), pp. 1482-1483
- 7 NOWROUZIAN, B.: 'A new synthesis technique for the exact design of switched-capacitor LDI allpass networks'. Proceedings of IEEE International Symposium on Circuits and Systems, New Orleans, USA, May 1990, pp. 2185-2188
- 8 PING, L., and SEWELL, J.I.: 'Switched capacitor and active-RC allpass ladder filters'. Proceedings of IEEE International Symposium on Circuits and Systems, New Orleans, USA, May 1990, pp. 2833-2836
- 9 PING, L., and SEWELL, J.I.: 'The LUD approach to switched-capacitor filter design', *IEEE Trans.* 1987, **CAS-34**, (12), pp. 1611-1614
- 10 PING, L., HENDERSON, R.K., and SEWELL, J.I.: 'Matrix methods for switched capacitor filter design'. Proceedings of IEEE International Symposium on Circuits and Systems, Helsinki, Finland, June 1988, pp. 1021-1024
- 11 PING, L., and SEWELL, J.I.: 'High performance circuit structures and symmetric matrix systems', *IEE Proc. G. Circuits, Devices and Systems*, 1989, **136**, (6), pp. 327-336
- 12 DAVIS, A.M.: 'A new z domain continued fraction expansion', *IEEE Trans.* 1982, **CAS-29**, (10), pp. 658-662
- 13 SESHU, S., and REED, M.B.: 'Linear graphs and electrical networks' (Addison-Wesley Publishing Company Inc., Reading, Massachusetts, USA, 1961)
- 14 HENDERSON, R.K., PING, L., and SEWELL, J.I.: 'A design program for digital and analogue filters: PANDDA'. Proceedings of the European conference on Circuit Theory and Design, Brighton, UK, Sept. 1989, pp. 289-293
- 15 GAZSI, L.: 'Explicit formulas for lattice wave digital filters', *IEEE Trans.*, 1985, **CAS-32**, (1), pp. 68-88