

MATRIX METHODS FOR SWITCHED CAPACITOR FILTER DESIGN

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ABSTRACT

Matrix form description of switched-capacitor (SC) filter networks is introduced. It offers a unified approach to the design of many different categories of filter specification and structure. By the application of matrix transformations, most notably LU factorisation, new filter structures simulating passive networks are derived. One such design eliminates the unswitched capacitive loops of leapfrog filters. Matrix design methods have been implemented in a software package for SC, active-RC and digital filters.

INTRODUCTION

Filter structures which simulate passive RLC ladders are often employed where low sensitivity to element value deviation is important. Of the many possible designs [1], most popular is the leapfrog filter [2], owing to its stray-insensitive property for switched-capacitor implementation.

Present design techniques for leapfrog filters involve the derivation of systematic sets of equations relating the internal variables (voltages and currents) of the ladder prototype. After s - z domain transformation each equation is implemented by a stray-insensitive switched-capacitor building block. For efficient realisation, the equation set must be derived in a different way depending on the form of the passive prototype. Complicated techniques must therefore be adopted to design different classes of filter.

It is shown in this paper that the same design process can be achieved through manipulation of a matrix equation, describing the passive network. The form of the SC network is concisely described by the positions of non-zero entries in a system of matrix equations, arranged to be directly realisable by integrating branches. Lowpass and bandpass filters may now be designed with similar ease, since the matrix operations performed are independent of the form of the passive network.

Various transformations drawn from matrix theory are employed, most notably lower-upper triangular (LU) factorisation. By this abstraction, several new ladder simulation topologies have been developed. One of these has the advantage over traditional leapfrog circuits, of having no delay-free loops, making digital realisation possible [3,4]. Improved performance to non-ideal circuit parameters and low capacitance spread have been obtained for certain SC circuits.

Finally, matrix form is used to demonstrate the equivalence between LDI and bilinearly transformed ladder simulations. The distortion function introduced by approximate LDI simulation is found and it is observed that by compensating the passive ladder frequency response, with a filter optimisation program, that exact LDI switched capacitor filters may be conveniently designed. The same compensation technique is shown to be applicable to the bilinear filter structures, allowing them to utilise the LDI input branch,

which dispenses with the need for sample-and-hold input circuits.

The extension of these techniques to active-RC filters is elementary. Direct transfer function simulation methods, such as cascade biquads, can also be expressed in matrix form.

NETWORK MATRIX DESCRIPTION

According to principles put forward by Hasler [5], only certain stray-insensitive branches which have efficient realisations are possible (see table 1).

For later reference the following definitions are introduced:

$$\Phi = \frac{-1}{1 - z^{-1}} \quad \Psi = \frac{z^{-1}}{1 - z^{-1}} \quad (1a, b)$$

Direct simulation network

The cascade of biquadratic filter sections is the most popular direct transfer function simulation method to find application in active filter design, and will be used as an illustration of matrix form. The principle applies equally to other methods.

The general biquadratic section may be seen to be composed of the stray-insensitive branches of Table 1. The following matrix equations describe a system of biquads.

$$AX = \Psi BY + CY + f(z)J \quad (2a)$$

$$DY = \Phi EX + FX + g(z)J \quad (2b)$$

where X represents the intermediate output voltages of inverting integrators,

Y represents the output voltages of noninverting integrators, $f(z)$, $g(z)$ are input functions and J is a vector of inputs.

Matrices B and C of (2a) represent inverting delaying switched-capacitors and capacitors respectively, connected from op-amp output voltages Y to op-amp inputs X. For example, a non zero entry at position (i,j) of C represents a capacitor connected from voltage y_j to the input of an op-amp producing voltage x_i . Similar rules apply to matrices E and F of (2b) for non-inverting switched-capacitors.

Since op-amp outputs are only connected to either the previous or next op-amp input in a biquad cascade, the non-zero entries in the matrices may only lie on the main sub-diagonals, and so the matrices are at most tridiagonal. The same observation is true for passive network simulation methods.

Matrix description of passive network

The passive RLC ladder may be described in the continuous-time domain by the following nodal admittance matrix equation:

$$(sC + \frac{1}{s}\Gamma + G)V = J \quad (3)$$

where C, Γ and G are admittance matrices formed by the contributions of capacitors, inductors and resistors respectively,

V is a vector of node voltages, J is a vector of input currents (for a single input ladder $J = (J_{in}, 0, \dots, 0)^T$).

Note that it may be more efficient, if there are fewer loops than nodes in the ladder, to use a loop equation $QI = V$. Take $T=2$ secs, for simplicity, and after bilinear transformation this becomes:

$$\left[\frac{1-z^{-1}}{1+z^{-1}} C + \frac{1+z^{-1}}{1-z^{-1}} \Gamma + G \right] V = J \quad (4)$$

Multiply equation (4) through by $(1+z^{-1})/(1-z^{-1})$ to get:

$$\left[C + \left[\frac{1+z^{-1}}{1-z^{-1}} \right]^2 \Gamma + \frac{1+z^{-1}}{1-z^{-1}} G \right] V = \frac{1+z^{-1}}{1-z^{-1}} J \quad (5)$$

Rearranging gives:

$$\left(\frac{1}{\Psi} A - \Phi B + D \right) V = (1+z) J \quad (6)$$

$$A = C + \Gamma + G, \quad B = 4\Gamma, \quad D = 2G.$$

Equation (4) has now been expressed in terms of realisable functions of the discrete time variable z .

Matrix form simulation

New sets of internal variables must be created to fully simulate the operation of the ladder prototype. These new intermediate variables are related to the node voltages of (6) by some additional matrix equations. Three ways are proposed to form these equations:

(a) *factorise matrix* $A = A_L A_R$ (Type-L)

$$A_R X = (\Phi B - D) V + (1+z) J \quad (7a)$$

$$A_L V = \Psi X \quad (7b)$$

where X is the new vector of intermediate variables,

A_L and A_R are the left and right factors of A .

These equations describe a signal flow graph in which a link is present for each non-zero entry in the matrices. Thus, in order to keep the number of coupling branches low, a factorisation method which preserves the sparsity of the original admittance matrix is desirable.

Two possibilities are apparent:

- i. lower-upper triangular factorisation ($A = LU$),
- ii. direct factorisation ($A = AI$).

LU factorisation yields a new stray-insensitive, ladder-simulation structure, known as the LUD filter [4], which possesses *no* delay-free loops. These unswitched, capacitive loops have various detrimental effects on filter performance [1]. Delay-free loops may be seen from (7) to be dependent on the presence of non-zero, off-diagonal entries in matrix A . A loop is formed where these entries occupy positions above and below the main diagonal, causing cross-coupling of op-amp inputs and outputs. By the separation of below-diagonal and above-diagonal elements to matrices L and U , respectively, all loops are effectively removed. Direct factorisation also yields new structures, however they possess delay-free loops and appear to offer no obvious advantages over existing leapfrog structures.

(b) *factorise matrix* $B = B_L B_R$ (Type-R)

$$(A + \Psi D) V = \Psi B_L X + \frac{1+z^{-1}}{1-z^{-1}} J \quad (8a)$$

$$X = \Phi B_R V \quad (8b)$$

where X is the new vector of intermediate variables, B_L and B_R are the left and right factors of B .

LU factorisation of matrix B yields structures related to well-known leapfrog circuits. Design of leapfrog filters is achieved through a topological factorisation:

$$B = A(D_a A^T), \quad B_L = A, \quad B_R = D_a A^T \quad (9)$$

where A is incidence matrix of the inductors in the

ladder, D_a is a diagonal matrix of reciprocal inductance values.

For lowpass ladder prototypes, B_L and B_R of (9) are the L and U factors of B , so the resulting filters are identical. This is no longer true for bandpass design where leapfrog realisation requires some extra op-amps. Since no decomposition of A is performed, its off-diagonal elements cause delay-free loops, regardless of the factorisation of B .

(c) *factorise both* A and B ($A = A_L A_R$, $B = B_L B_R$) (Type-B)

$$A_R X = B_L Y - DV + (1+z) J \quad (10a)$$

$$Y = \Phi B_R V \quad (10b)$$

$$A_L V = \Psi X \quad (10c)$$

An SC network, which is no longer canonical in the number of op-amps would be required to simulate this matrix system. Due to the absence of delay-free loops, digital simulation is possible, with high speed and low implementation cost [3].

Some points to note are:

1. The structure of the SC filter network may be kept fixed for lowpass and bandpass designs, provided a certain form of ladder prototype is simulated. This allows the filters to be programmable.
2. Active RC circuits may be derived using the same procedure, with the identification of $\Psi = \Phi = 1/s$ and $A = C$, $B = \Gamma$, $D = G$ and the alteration of the input multiplier function in equations (7,8).

INPUT STAGE REALISATION

Two input terms require to be realised for the schemes above (Table 2). The bilinear input branches sample on both even and odd clock phases requiring a sample-and-hold circuit as a preliminary stage. This necessitates an extra operational amplifier which may be a significant layout overhead for small order filters. Removal of the odd phase sampling branch solves this problem, with the penalty that the bilinear zero at the Nyquist frequency disappears and a magnitude weighting of the frequency response is introduced. Correction of these effects may be achieved by prewarping the frequency specifications by a $(1+z)$ or $\cos(\omega T/2)$ function. The component values of the original prototype ladder can be modified by a filter optimisation program to produce the required warping. This may only be necessary for low clock-to-signal frequency ratios. Such an alteration of the bilinear input branch results in a circuit having the same structure as an LDI filter with improperly realised terminations. The error introduced by this incorrect simulation may be seen from matrix form. It is well known that an extra half period delay is realised at the filter terminations after LDI transformation of the passive ladder [6].

$$\left[\frac{z^{-\frac{1}{2}}}{1-z^{-1}} C + \frac{1-z^{-1}}{z^{-\frac{1}{2}}} \Gamma + z^{-\frac{1}{2}} G \right] V = J \quad (11)$$

This can be rearranged to the form:

$$\left[\frac{1+z^{-1}}{1-z^{-1}} A + \frac{1-z^{-1}}{1+z^{-1}} B + D \right] V = \frac{z^{-\frac{1}{2}}}{1+z^{-1}} J \quad (12)$$

$$A = C/4, \quad B = C - \Gamma/4 - G/2, \quad D = G/2.$$

Eq. (12) describes a bilinear system with a $1/\cos(\omega T/2)$ weighting function at the input. Thus exact LDI design, which removes the distortion, requires modification by a factor $\cos(\omega T/2)$. This can be conveniently combined with $\sin(x)/x$ correction resulting in a $x/\tan(x)$ compensation function.

EXAMPLES

A program named PANDDA (Program for Advanced

Network Design: Digital and Analogue) has been developed, applying the matrix principles presented in this paper. The flexible nature of the program allows SC, digital, active-RC and passive RLC designs to be generated. General filter approximation and ladder weighting options are available. PANDDA is used in conjunction with ideal and non-ideal SC network analysis programs SCNAPIF [7], QUICKSCNAP [8].

A sixth-order, bandpass, elliptic prototype is designed and simulated by both type-L and type-R LUD SC filters (Figs 1 and 2). In both examples the input stage has been modified and prototype optimised according to the principles of the previous section. Scaling for maximum dynamic range has been performed. The passband edges of the SC filter are 3600Hz and 4000Hz.

Fig 3a shows that use of a single phase input branch, causes removal of the pole at half the sampling frequency. Fig 3b shows a comparison between the ideal and non-ideal filter responses in the passband for type-L and type-R LUD realisations, with non-ideal amplifier and switch parameters. The distortion of the type-L response is less than that of the type-R response. The type-R design possesses unswitched capacitive loops (e.g. C2-C3-C10-C7-C2) around the op-amp outputs and inputs. These loops have the consequences of extending the op-amp settling times and transmitting high frequency noise directly to the filter output [9]. Type-R designs do not possess such loops, as may be observed from the signal flow directions on Fig 2a; notice that charge may not circulate around the long capacitor loop (C3-C7-C11-C15-C23-C18-C14-C10-C6-C2-C3).

Table 3 shows that type-L design has lower capacitance spread than type-R. This becomes more pronounced as the bandwidth of the filter narrows.

CONCLUSIONS

For the purposes of filter design, matrix form offers a concise description of realisable networks. A regular process, involving simple manipulations of matrix equations, is now available for the derivation of filter structures. Several new SC filters simulating passive RLC ladders can be obtained in this way, one having certain advantages over traditional designs. The use of the LDI and bilinear transform in the matrix design method results in topologies differing only in their input branch. It is shown that a single phase sampling input branch may always be used, dispensing with the need for a sample-and-hold circuit.

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Name	SFG branch	Switched-capacitor realisation
Feedthrough $H_{ee}(z)$	$-\alpha$	
Non-inverting integrator $H_{ee}(z)$	$\alpha \frac{1 - \alpha z^{-1}}{1 - z^{-1}}$	
Inverting integrator $H_{ee}(z)$	$\alpha \frac{-\alpha}{1 - z^{-1}}$	

Table 1 Stray-insensitive switched-capacitor branches

Name	Input Branch	Switched-capacitor realisation
Bilinear input $H_{ee}(z)$	$-\left[\frac{1 + z^{-1}}{1 - z^{-1}} \right]$	
LUD input $H_{ee}(z)$	$-(1 + z^{-1})$	

Table 2 Two phase input branches

TABLE 3
DESIGN DATA FOR THE SC FILTER EXAMPLES OF FIG.1 AND FIG.2

Normalized Data for the LC Ladder of Fig.(1a)					
upper passband edge	1.0544	lower passband edge	0.9484		
upper stopband edge	1.1075	lower stopband edge	0.9029		
passband ripple	< 0.1 db	stopband attenuation	> 22 db		
G1	1.0	G2	1.04937	C1	8.370385
L2	0.254088	C4	3.93473	L4	0.201656
				C5	8.725127
				L5	0.11479
Component Values for the Type-R SCF of Fig.(1c)					
C1	15.912	C2	71.431	C3	5.2593
C4	2.1665	C5	1.0	C6	14.979
C7	38.627	C8	1.	C9	2.3398
C10	13.651	C11	46.620	C12	3.5384
C13	11.702	C14	20.415	C15	2.6344
C16	1.0	C17	10.485	C18	64.686
C19	1.2831	C20	1.0	C21	1.0
C22	5.6359	C23	1.0		
number of capacitors	23	number of switches	30		
number of op amps	6	total capacitance	337.366		
capacitance spread	71.431	clock frequency	128 kHz		
unit capacitance	1 pF				
Component Values for the Type-L SCF of Fig.(2b)					
C1	1.2831	C2	1.0	C3	15.620
C4	2.3015	C5	1.0	C6	4.6369
C7	9.8960	C8	1.2620	C9	1.0623
C10	21.067	C11	21.067	C12	4.1209
C13	1.0	C14	4.4922	C15	10.378
C16	2.0283	C17	1.0	C18	1.0910
C19	10.604	C20	2.4337	C21	1.0
C22	5.1269	C23	1.0		
number of capacitors	23	number of switches	25		
number of op amps	6	total capacitance	105.8765		
capacitance spread	21.0668	clock frequency	128 kHz		
unit capacitance	1 pF				

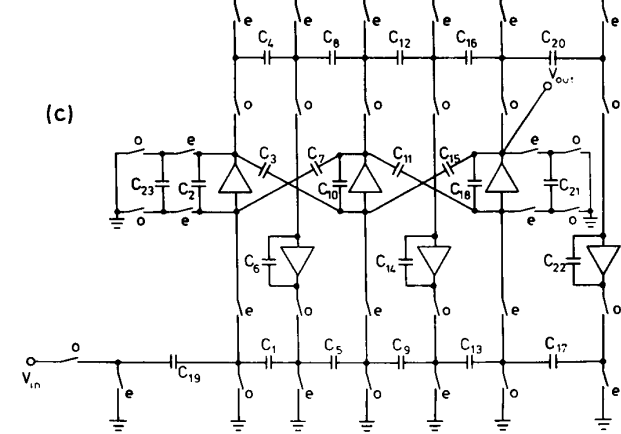
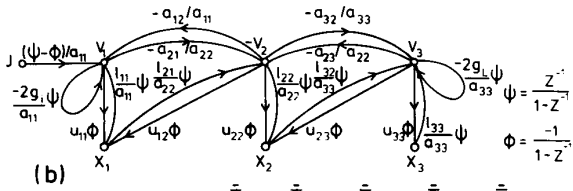
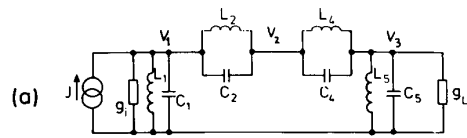
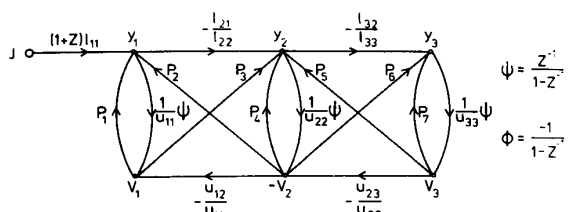


Fig. 1 (a) Terminated LC ladder passive prototype.
 (b) LUD type - R signal-flow-graph simulation of the circuit in (a).
 (c) LUD type - R SCF simulation of the circuit in (a), (single phase input).



$$\psi = \frac{Z^{-1}}{1-Z^{-1}}$$

$$\phi = \frac{-1}{1-Z^{-1}}$$

$$P_1 = \frac{4\lambda_{11}\phi + 2g_1}{l_{11}} \quad P_2 = \frac{4\lambda_{12}}{l_{11}}\phi \quad P_3 = \frac{4\lambda_{21}}{l_{22}}\phi \quad P_4 = \frac{4\lambda_{22}}{l_{22}}\phi$$

$$P_5 = \frac{4\lambda_{23}}{l_{22}}\phi \quad P_6 = \frac{4\lambda_{32}}{l_{33}}\phi \quad P_7 = \frac{4\lambda_{33}\phi + 2g_2}{l_{33}}$$

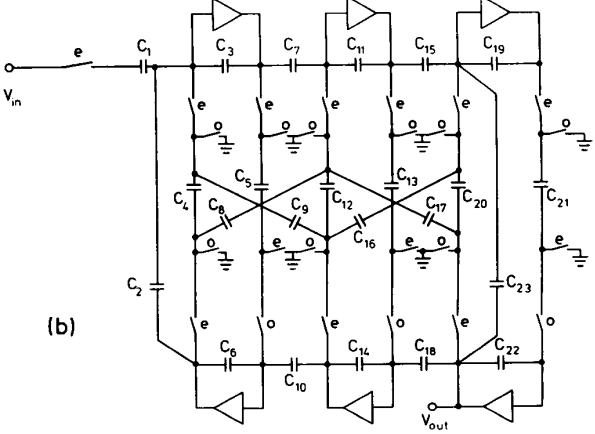


Fig. 2 (a) LUD type - L signal-flow-graph simulation of the circuit in Fig.1(a).
 (b) LUD type - L SCF simulation of the circuit in Fig.1(a) (single phase input)

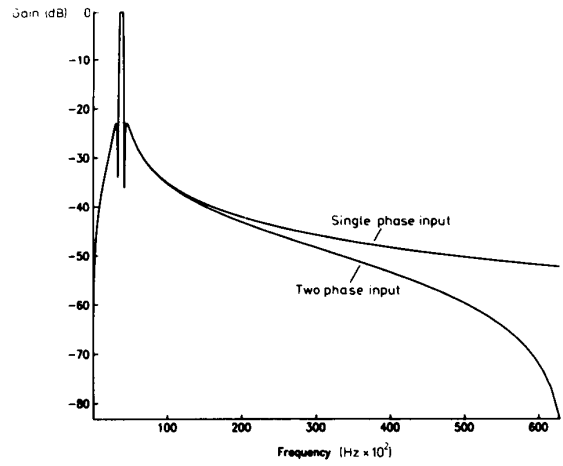


Fig 3(a) Responses of 6th order band-pass elliptic filter with two different input stage schemes

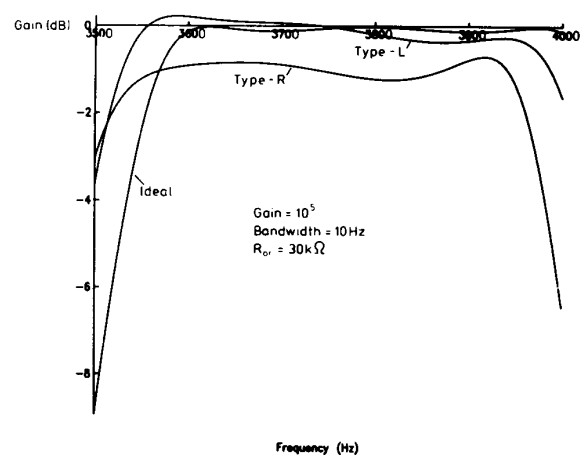


Fig 3(b) Comparison of filter passband characteristics with non-ideal amplifier and switch parameters