

Fig. 4. Layout of a testable serial-parallel multiplier.

in the logic block, the output  $PZ$  should be low (connected to  $V_{ss}$ ) in the case of n-logic and high (connected to  $V_{dd}$ ) in the case of p-logic.

In the case of static CMOS, the presence of a stuck-on transistor may result in both p- and n-networks being conducting. The output voltage thus depends on the resistance of the p- and n-network and hence increases the complexity of fault detection. Such cases do not happen in NORA CMOS because the p- and the n-network cannot be both conducting at the same time even if stuck-on occurs in the logic block. This is because the clock ( $\phi$  or  $\bar{\phi}$ ) is applied to both the pMOS and the nMOS transistor that are in series with the logic block and thus prevent both transistors to be conducting at the same time. Hence the output voltage is not dependent on the resistance of the networks and, therefore, it is easier to detect stuck-on faults. The procedure for testing stuck-on is similar to those described for other faults. For the circuit with n-logic block shown in Fig. 2, TEST2 is charged high prior to the evaluation phase. A low TEST2 during the evaluation phase with appropriate test vector inputs TV1 applied prior to, and kept constant at the evaluation phase indicates a stuck-on condition. Similarly, for the circuit with p-logic block as shown in Fig. 3, a low TEST4 during the evaluation phase with appropriate test vector inputs TV2 indicates a stuck-on condition. It can again be seen that the test for stuck-on fault and the test for stuck-at fault are overlapped to some extent, because a device stuck-on could result in the output to be either stuck-at-one or stuck-at-zero.

#### V. AREA AND TIME CONSIDERATIONS

The additional circuits (shown in Figs. 2 and 3) used to detect stuck-at, stuck-open, and stuck-on faults occupy only a small amount of area overhead and is independent of the complexity of the gate to be tested. The amount of contact cuts for the layout is also very small. This is favorable because contact cuts occupy large areas and degrade reliability of the circuit. However, by connecting many nMOS devices or pMOS devices in series may reduce the speed of operation for testing. This disadvantage is not so important because the clock can be slowed down for testing. Moreover, buffers can be inserted between the devices to reduce the delay.

#### VI. APPLICATIONS AND CONCLUSIONS

This testability enhancement technique is employed in implementing a testable serial-parallel multiplier. A prototype of multiplier with 4-bit multiplicand and 3-bit multiplier has been implemented using 4- $\mu$ m CMOS (NORA) technology, Fig. 4, the total

layout area is found to be 3.89 mm<sup>2</sup>. The multiplier takes around 11 ns to produce the product and the error signal. The additional cost for the error detection circuitry is only in the range of 10 percent of the total area.

The testability enhancement technique is useful especially where the internal nodes of the system are difficult to test. It can also be used for probe testing of wafer. In conclusion, the proposed error detection circuit, based on the structure, properties, and operations of NORA CMOS, can detect stuck-at, stuck-open, and stuck-on faults. It occupies only a small amount of area overhead and is independent of the complexity of the cell to be tested.

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#### The LUD Approach to Switched-Capacitor Filter Design

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**Abstract**—A new design method for switched-capacitor filters (SCF) is presented. It is based upon an LU matrix decomposition technique and has the distinct advantage of producing SC filter realizations containing no delay free loops. These are formed traditionally by capacitors and op-amps in leapfrog realizations. It is demonstrated that this feature should render reduced dependence of the filter response to nonideal effects such as finite amplifier GB and switch resistance. Results from realistic leapfrog and LUD SC filter realizations confirm this.

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INTRODUCTION

Passive terminated LC ladder simulations are popular techniques in switched-capacitor filter (SCF) design, as they retain the low sensitivities of the prototype passive ladders. Among various simulation methods the leapfrog-type SCF has received most attention because of its strays insensitive property [1]–[3].

There are two kinds of transformations commonly adopted in designing leapfrog SCF's: LDI and bilinear transformations [1]. LDI SCF's have the problem of strictly unrealizable terminations. Some approximation must be made and this limits their applications. Bilinear leapfrog SCF's using LDI integrators are more favorable. However, there is a major drawback for the bilinear leapfrog SCF (and, also, for LDI leapfrog SCF when the transfer function has finite transmission zeros) that there always exist delay-free loops formed by capacitors and op-amps. This increases the op-amps settling times. As a result, some considerable distortion of the transfer function may be caused by the finite GB product of op-amps and on-resistance of switches [3], [4], [6]. Incidentally the existence of delay-free loops makes digital circuit realization difficult [7]–[9].

In this paper, the matrix form derivation of leapfrog SCF is viewed first. Then a new structure of SCF based on LU decomposition is presented and the corresponding digital circuit realization is briefly discussed. No delay-free loops exist in these circuits. Examples are given to show that the new approach produces circuits with better performances than leapfrog-type circuits when nonideal effects of op-amps and MOS switches are considered.

DERIVATION OF LEAPFROG SCF IN MATRIX FORM

The first bilinear leapfrog SCF's were sensitive to stray capacitance. A further development [1] allowed application of the bilinear transformation whilst using modified LDI integrators which are completely strays insensitive. We shall derive this kind of SCF as the preliminary to the new approach.

Starting from a passive RLC prototype network which can be described by nodal equation:

$$\left( sC + \frac{1}{s}\Gamma + G \right) V = J \tag{1}$$

where  $C$ ,  $\Gamma$ , and  $G$  stand for the contribution of capacitors, inductors, and conductors respectively. Performing the bilinear transformation on (1) we have (when  $T = 2$  for simplicity)

$$\left\{ \frac{1-z^{-1}}{1+z^{-1}}C + \frac{1+z^{-1}}{1-z^{-1}}\Gamma + G \right\} V = J. \tag{2}$$

Equation (2) is equivalent to

$$AV = \left\{ -\frac{4z^{-1}}{(1-z^{-1})^2}\Gamma - \frac{2z^{-1}}{1-z^{-1}}G \right\} V + \frac{1+z^{-1}}{1-z^{-1}}J \tag{3a}$$

with

$$A = C + \Gamma + G. \tag{3b}$$

The inverse inductance matrix  $\Gamma$  in (3) can be decomposed into

$$\Gamma = A_L D_L A_L^T \tag{4}$$

where  $A_L$  is the incidence matrix of the network obtained by removing all elements except inductors, and  $D_L = \text{diag}(1/L_i)$ . Let

$$A = D_a + B \tag{5}$$

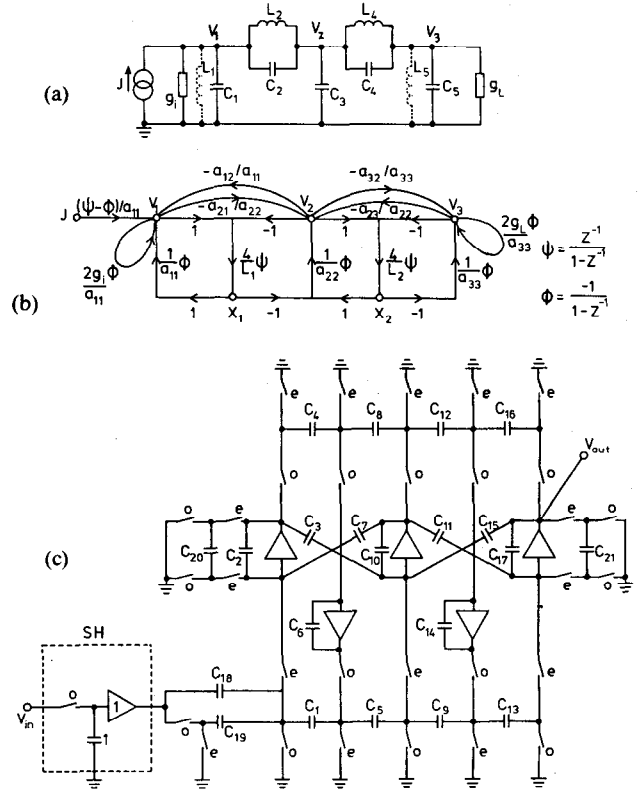


Fig. 1. (a) A terminated LC ladder passive prototype. (b) Leapfrog-type signal-flow-graph simulation of the circuit in (a). (c) Leapfrog SCF simulation of the circuit in (a).

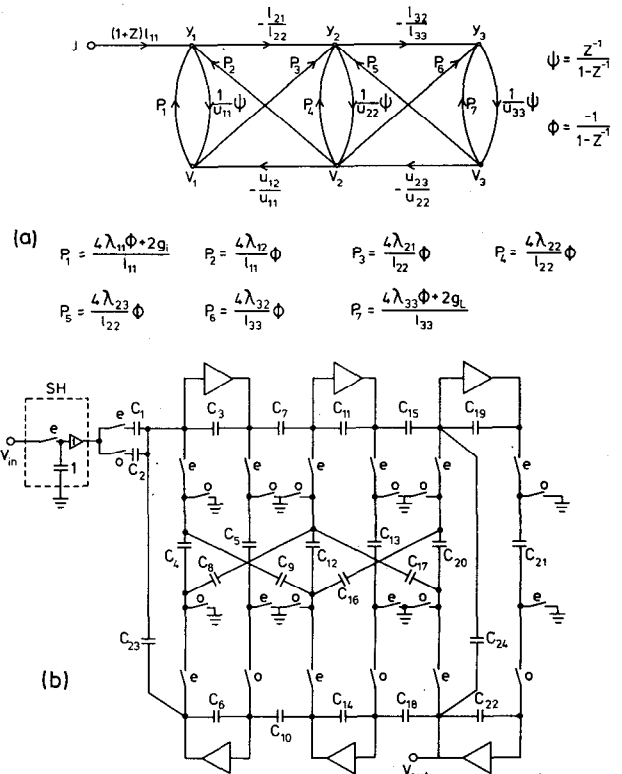


Fig. 2. (a) LUD type signal-flow-graph simulation of the circuit in Fig. 1(a). (b) LUD SCF simulation of the circuit in Fig. 1(a).

TABLE I  
DESIGN DATA FOR THE SC FILTER EXAMPLES OF FIG. 1 AND FIG. 2

Normalized Data for the LC Ladder of Fig.(1a)									
1) Fifth order Lowpass Elliptic Case									
passband edge	1.			stopband edge	1.555723827				
passband ripple	0.0436 dB			stopband ripple	41.9 dB				
G1 = GL = 1	L1 0	C1	0.867058	L2	1.223976	C2	0.137493		
C3	1.511948	L4	0.940651	C4	0.406594	C5	0.669168	L5	0
2) Sixth order Bandpass Elliptic Case									
upper passband edge	1.034			lower passband edge	0.967				
upper stopband edge	1.173			lower stopband edge	0.895				
passband ripple	< 0.25 dB			stopband attenuation	> 34 dB				
G1 = G2 = 1	C3 = 0	C1	1.6310	L1	0.014807	C2	0.38030		
L2	0.088285	C3	0.27356	L3	0.063504	C4	1.6310	L4	0.014807
Component Values for the Leapfrog SCF of Fig.(1c)									
passband edge	3.235 kHz			stopband edge	4.800 kHz				
C1	4.3117021	C2	3.8187507	C3	1.0000000	C4	1.1283536		
C5	3.8212329	C6	2.7566618	C7	1.0000000	C8	1.0000000		
C9	3.3194505	C10	8.8680304	C11	1.3122242	C12	1.6543911		
C13	2.1279985	C14	3.0446682	C15	1.2372708	C16	1.0000000		
C17	1.3110067	C18	1.7601345	C19	3.5202689	C20	3.2856668		
C21	1.0000000								
number of capacitors	21			number of switches	30				
number of op amps	5			total capacitance	52.2778				
capacitance spread	8.8680			clock frequency	32 kHz				
Component Values for the LUD SCF of Fig.(2b)									
1) Fifth order Lowpass Elliptic Case									
passband edge	3.325 kHz			stopband edge	4.8 kHz				
C1	1.125332	C2	1.125332	C3	3.664828	C4	1.128354		
C5	5.732167	C6	7.104417	C7	1.000000	C8	1.938541		
C9	1.000000	C10	1.000000	C11	7.464650	C12	3.953523		
C13	4.867762	C14	7.053555	C15	1.295663	C16	1.654369		
C17	1.351268	C18	1.000000	C19	1.905143	C20	1.000000		
C21	1.000000	C22	1.595858	C23	2.100672	C24	1.430766		
number of capacitors	24			number of switches	26				
number of op amps	6			total capacitance	62.4922				
capacitance spread	7.4646			clock frequency	32 kHz				
2) Sixth order Bandpass Elliptic Case									
upper passband edge	1 kHz			lower passband edge	0.9 kHz				
upper stopband edge	1.08 kHz			lower stopband edge	0.829 kHz				
C1	1.000000	C2	1.000000	C3	23.35666	C4	13.72274		
C5	2.353740	C6	2.807107	C7	2.180592	C8	1.030186		
C9	3.930910	C10	1.000000	C11	7.101668	C12	4.910849		
C13	4.977363	C14	5.842078	C15	6.643089	C16	5.464835		
C17	1.000000	C18	1.000000	C19	12.62665	C20	10.11870		
C21	1.000000	C22	1.375713	C23	1.432187	C24	1.000000		
number of capacitors	24			number of switches	26				
number of op amps	6			total capacitance	116.8751				
capacitance spread	23.3567			clock frequency	8 kHz				

where  $D_a$  is diagonal and all diagonal elements in  $B$  are zeros. Then (3) can be written as

$$D_a V = -BV - \frac{2z^{-1}}{1-z^{-1}}GV - \frac{1}{1-z^{-1}}A_L X + \frac{1+z^{-1}}{1-z^{-1}}J \quad (6a)$$

$$X = + \frac{4z^{-1}}{1-z^{-1}}D_L A_L^T V. \quad (6b)$$

These equations can be represented in signal-flow-graph form. Fig. 1 gives a terminated passive LC ladder with its corresponding signal-flow-graph in the discrete domain and the SCF implementation. Notice branches representing the term  $-BV$  in (6a) form two delay-free loops.

LU DECOMPOSITION (LUD)-TYPE SCF

In the last section it was shown that a leapfrog-type signal-flow-graph is formed by decomposing matrix  $\Gamma$  and realizing all nondiagonal elements in  $A$  by feedthrough branches. If  $A$  is of upper triangle or lower triangle form then these branches will not form delay-free loops. Unfortunately,  $A$  is neither of these cases for a practical ladder prototype.

One way to solve this problem is to decompose  $A$  into LU form. Let

$$A = LU \quad (7a)$$

$$Y = \frac{1-z^{-1}}{z^{-1}}UV. \quad (7b)$$

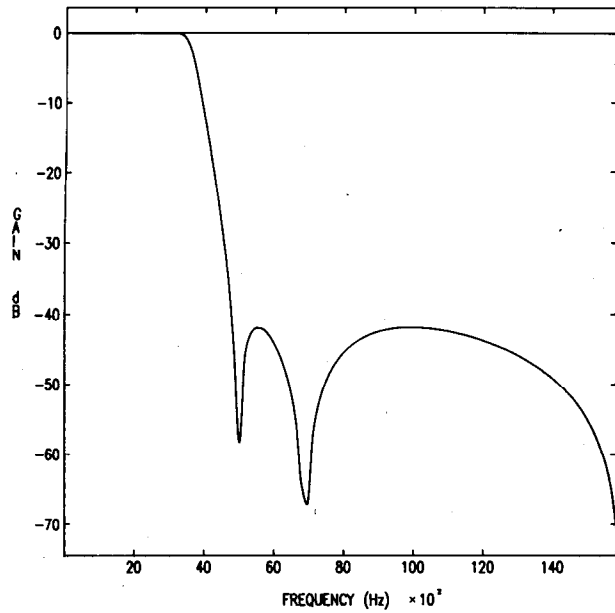
From (3) and (7) we have

$$LY = \left( -\frac{4}{1-z^{-1}}\Gamma - 2G \right) V + (1+z)J \quad (8a)$$

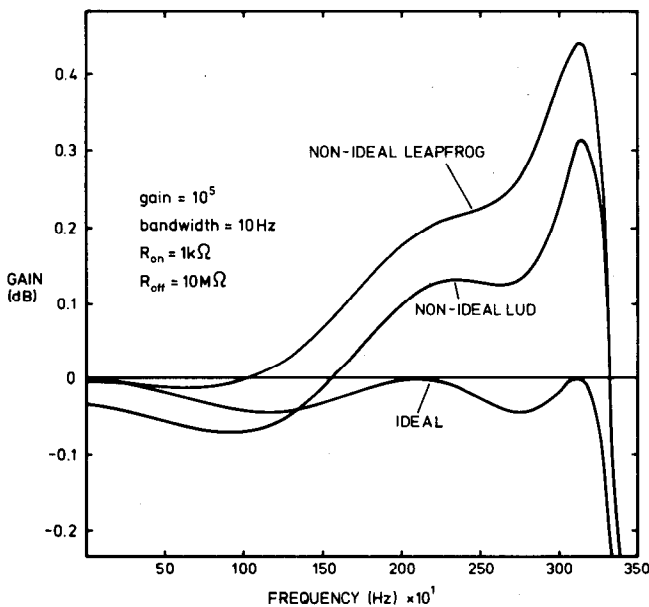
$$UV = + \frac{z^{-1}}{1-z^{-1}}Y. \quad (8b)$$

A signal-flow-graph can be drawn to represent (8); Fig. 2(a) shows one for the prototype given in Fig. 1(a).

The SCF implementation is shown in Fig. 2(b). Normally for a prototype network with  $n$  nodes,  $2n$  op-amps are required. It seems that for a prototype having more loops than nodes, we can start from a loop equation instead of the nodal equation in (1). In more general cases, a hybrid description of the prototype network can be used.



(a)



(b)

Fig. 3. (a) Response of ideal fifth-order low-pass elliptic filter (LUD). (b) Comparison of filter passband characteristics with typical amplifier and switch parameters, (sine not included).

Fig. 2(a) can be realized directly by digital circuits. In this case the number of multiplication operations must be taken into consideration. So we can decompose  $A$  into (note  $A$  is always symmetrical)

$$A = L_n D_n L_n^T \quad (9)$$

where diagonal entries of  $L_n$  are all 1 and  $D_n$  is a diagonal matrix. Thereby (8) can be rewritten as

$$L_n D_n Y = \left( -\frac{4}{1-z^{-1}} \Gamma - 2G \right) V + (1+z) J \quad (10a)$$

$$L_n^T V = + \frac{z^{-1}}{1-z^{-1}} Y. \quad (10b)$$

Approximately  $3n$  ( $n$  is the number of the nodes) coefficients need to be stored and  $4n$  multiplications performed in each period. It can be shown that this kind of digital filter is highly insensitive to finite length of coefficients.

### Examples

A program named SCNDP (SC network design program) has been developed using LUD as well as leapfrog approaches. This is used in conjunction with analysis programs SCNAPIF and SCNAPNIF [5].

Some typical filter realizations are shown in Figs. 1 and 2. The extra components in the passive prototype are required for the bandpass realization. The calculated capacitance values are listed in Table I. In the LUD realization it can be seen that one extra amplifier is only required for low-pass filters, the bandpass case utilizes the same circuit topology with changed component values and is canonic in number of amplifiers. A leapfrog bandpass realization would require a changed topology and a simple comparison does not follow. The one extra amplifier in the low-pass case will require more chip area, but this difference reduces in significance as the filter order increases. The op-amp's outputs in all circuits are adjusted to give the same level as the input. No attention has been given to minimizing the capacitance spread.

Fig. 3(a) shows the ideal filter response. Fig. 3(b) gives a comparison between ideal performance and non-ideal responses in the passband for LUD and leapfrog realizations with typical amplifier and switch parameters. The LUD realization demonstrates some improvement in performance over the equivalent leapfrog circuit for typical parameter values.

Preliminary sensitivity studies indicate that the LUD realization possesses similar properties to the leapfrog structure, except at  $\omega = 0$  in the low-pass case where a drop in magnitude response is observed. This is a subject of further work.

### CONCLUSION

A new kind of structure for SC filters is presented. Results obtained show that the proposed circuits demonstrate better performance than leapfrog circuits in certain non-ideal cases. It can be observed also that the particular ranges of non-ideal parameters pose serious influence on both circuits. Work is being undertaken to formally eliminate these effects in the design procedure.

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