

Filter realisation by passive network simulation

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Abstract: General simulation methods of passive networks are investigated. A new simulation approach based on LU matrix decomposition is presented. This approach can be used to design active-RC, switched-capacitor and digital networks. The resulting system demonstrates very low sensitivities with respect to component values. New digital realisations, in particular, reveal structures of low complexity, high speed of operation and low cost of implementation.

1 Introduction

A wide variety of design methods are available for digital filter circuits. Direct methods, including cascade biquads and follow-the-leader (FL), have the advantage of simplicity but the penalty of high sensitivity [1]. The effort devoted to low-sensitivity structures has achieved notable success. In particular, wave and lattice approaches have developed into a distinguished family [2, 3]. Modification of the leapfrog method drawn from active-RC circuits has also attracted much attention [4-6]. An interesting recent development is the introduction of the lossless bounded real (LBR) concept with several promising structures emerging [7-9]. The remaining problem with these low-sensitivity circuit designs is that they are generally complicated, suffering from high hardware cost or limitation of operation speed, especially for high-order realisations.

This paper discusses a new approach based on passive ladder simulation in matrix form. The LU matrix decomposition is employed to derive new filter structures. Besides retaining the low-sensitivity of the prototype, the new method also has the important property of relatively low hardware cost and high operation speed. Some strategies are adopted to obtain structures most suitable for parallel processing. Because the design method is unified through matrix manipulations, the resulting circuit structures are regular, allowing easy programmable implementation.

This method has been previously proposed for switched-capacitor (SC) realisation [10, 11]. For simplicity of comprehension, the application to active RC circuit design is outlined first in this paper, and the development of the digital case is then discussed in detail. Examples are given comparing the performance of the new design with those of other methods.

Discussions are restricted to the lowpass case. The principles are the same for other types of RC circuits and also for bandpass digital design [10, 11]. For the high-pass digital case a well known transformation of $z^{-1} \rightarrow -z^{-1}$ can be used. For the bandstop digital case the technique adopted is somewhat different and will be presented elsewhere.

2 Matrix form simulation of passive ladders

Leapfrog structures have been very popular in active-RC and SC filter design and are conventionally explained as methods simulating the voltage/current relationships in RLC ladders [12-14]. The structure is derived according to these voltage/current relations, which can be a tedious procedure. A more systematic derivation is now presented as the preliminary to further developments in succeeding sections.

The procedure starts with a typical passive RLC prototype network, Fig. 1a, which can be described by the nodal equation

$$(sC + s^{-1}\Gamma + G)V = J \quad (1)$$

where C , Γ and G represent the contributions of capacitors, inductors and conductors, respectively. For convenience V is defined by $[v_1, -v_2, v_3, -v_4, \dots]^T$ to make all the entries of C , Γ and G positive. Notice the inverse inductance matrix Γ in eqn. 1 can be decomposed according to network topology into

$$\Gamma = A_L D_L A_L^T \quad (2a)$$

where A_L is the incidence matrix of the inductor sub-network and $D_L = \text{diag}(L_1^{-1}, L_2^{-1}, \dots)$.

Define a new set of variables

$$X = s^{-1} D_L^T A_L V \quad (2b)$$

with

$$(sC + G)V = -A_L X + J \quad (2c)$$

For an allpole lowpass filter (Fig. 1a) C is diagonal and $(sC + G)^{-1} = \text{diag}[(sc_1 + g_{in})^{-1}, (sc_2)^{-1}, (sc_3)^{-1}, \dots, (sc_n + g_L)^{-1}]$. X and V can be expressed in a recursive form

$$\begin{bmatrix} V \\ X \end{bmatrix} = \begin{bmatrix} \mathbf{0} & -(sC + G)^{-1} A_L \\ s^{-1} D_L A_L^T & \mathbf{0} \end{bmatrix} \begin{bmatrix} V \\ X \end{bmatrix} + \begin{bmatrix} (sc_1 + g_{in})^{-1} J \\ \mathbf{0} \end{bmatrix} \quad (3)$$

A signal flow graph (SFG), Fig. 1b can be drawn to represent eqn. 3 and the corresponding active-RC implementation follows directly (Fig. 1c). The output of every op-amp represents a variable either in V or in X . For every nonzero entry in the coefficient matrix of eqn. 3 there is a corresponding connection between two op-

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amps. For circuits with series capacitors (Fig. 2a) matrix C will have off-diagonal elements and this would appear

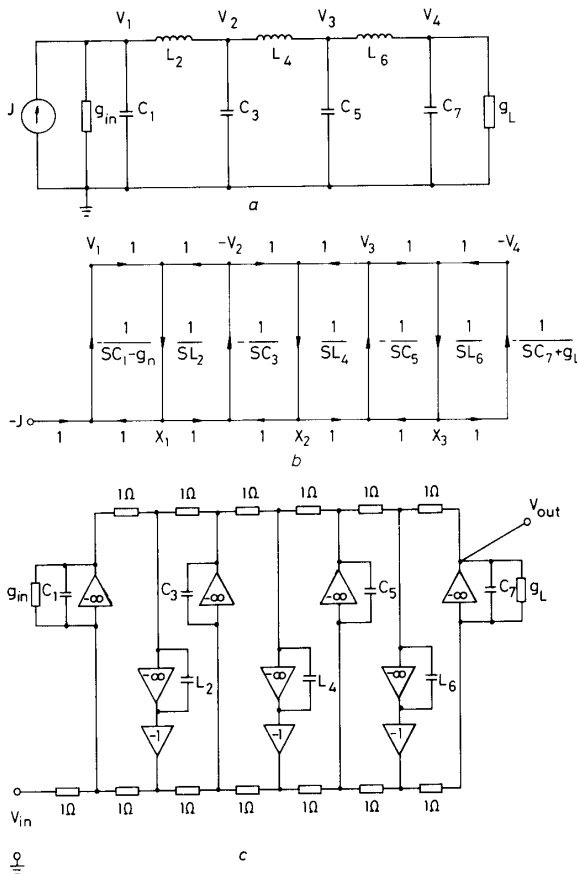


Fig. 1 7th-order Chebyshev lowpass ladder

a Circuit diagram

$$\begin{aligned} g_{in} &= 1\text{S} & g_L &= 1\text{S} \\ c_1 &= 3.585\text{F} & L_2 &= 4.330\text{H} \\ c_3 &= 6.370\text{F} & L_4 &= 4.789\text{H} \\ c_5 &= 6.370\text{F} & L_6 &= 4.330\text{H} \\ c_7 &= 3.585\text{F} & & \end{aligned}$$

b Leap-frog type SFG simulation of the passive circuit

c Corresponding active-RC realisation (normalised)

to make the matrix inversion $(sC + G)^{-1}$ in eqn. 3 somewhat more complicated. In this case eqn. 3 can be rewritten as

$$\begin{bmatrix} V \\ X \end{bmatrix} = \begin{bmatrix} -(sC_{\text{diag}} + G)^{-1}sC_{\text{offd}} & -(sC_{\text{diag}} + G)^{-1}A_L \\ s^{-1}D_L A_L^T & 0 \end{bmatrix} \times \begin{bmatrix} V \\ X \end{bmatrix} + \begin{bmatrix} (sC_{11} + g_{in})^{-1}J \\ 0 \end{bmatrix} \quad (4)$$

where $C = C_{\text{diag}} + C_{\text{offd}}$, $C_{\text{diag}} = \{c_{ii}\}$ and $C_{\text{offd}} = \{c_{ij} | i \neq j\}$ contain the diagonal and off-diagonal elements of C , respectively. Now the SFG and the corresponding circuit implementation can be obtained from eqn. 4 (see Figs. 2b, c). Branches representing the term $-(sC_{\text{diag}} + G)^{-1}sC_{\text{offd}}$ in eqn. 4 form three feed-through loops, shown in the upper part of Fig. 2b. These feed-through loops, which are realised by cross-coupled capacitors, increase the high-frequency noise levels; as can be seen from Fig. 2c, the high frequency noise created by each op-amp will be fed directly via the cross-coupled capacitors to the output. They also extend the settling time of op-amps in SC realisations and render digital

realisation difficult. In the next Section, a new simulation structure is suggested to overcome this problem.

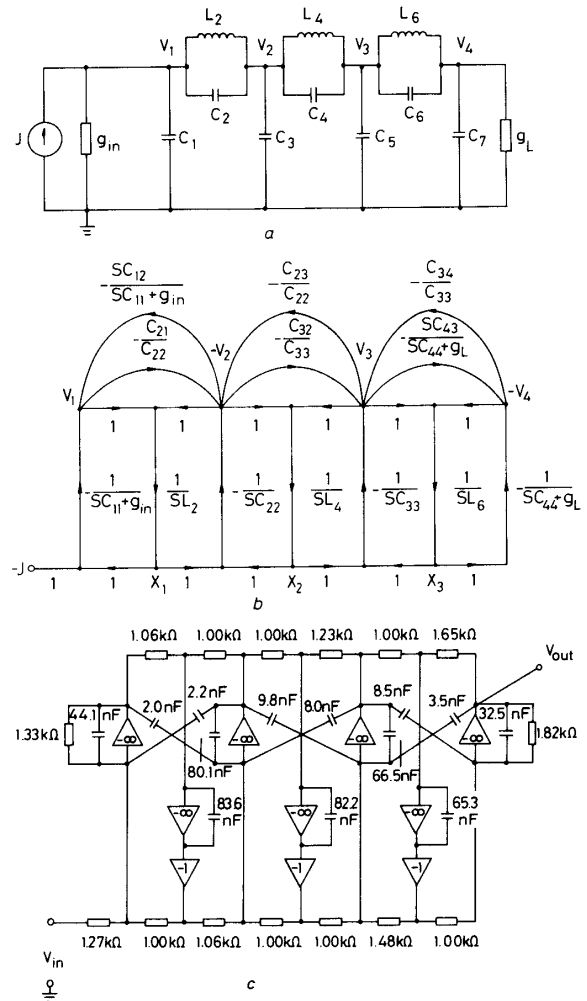


Fig. 2 7th-order elliptic lowpass ladder

a Circuit diagram

$$\begin{aligned} g_{in} &= 1\text{S} & g_L &= 1\text{S} \\ c_1 &= 3.450\text{F} & c_2 &= 0.1717\text{F} & L_2 &= 4.137\text{H} \\ c_3 &= 5.601\text{F} & c_4 &= 0.8016\text{F} & L_4 &= 3.828\text{H} \\ c_5 &= 5.328\text{F} & c_6 &= 0.5722\text{F} & L_6 &= 3.659\text{H} \\ c_7 &= 3.082\text{F} & & & & \end{aligned}$$

b Leap-frog type SFG simulation of the passive circuit

c Corresponding active-RC realisation (scaled for maximum dynamic range and denormalised, 3.4 kHz)

3 The LU decomposition simulation method

The elimination of feed-through loops is possible. Let matrix C in eqn. 1 be decomposed into LU form [15]

$$C = LU \quad (5a)$$

As matrix C in the nodal equation (eqn. 1) is always symmetric for passive networks, eqn. 5a can be expressed in symmetric form with D being a diagonal matrix.

$$C = U^T D U \quad (5b)$$

Choose $L = U^T D$ and introduce a new set of variables

$$X = s D U V \quad (5c)$$

From eqns. 1 and 5

$$U^T X = -s^{-1} \Gamma V - G V + J \quad (6a)$$

$$DUV = s^{-1}X \quad (6b)$$

To show how the system of eqns. 6 can be represented by a SFG form, choose U with all the diagonal entries being 1 and separate U into diagonal and off-diagonal terms:

$$U = I + U_{\text{offd}} \quad (7)$$

From eqns. 6 and 7 a recursive representation of V and X is obtained:

$$\begin{bmatrix} X \\ V \end{bmatrix} = \begin{bmatrix} -U_{\text{offd}}^T & -(s^{-1}\Gamma + G) \\ s^{-1}D^{-1} & -U_{\text{offd}} \end{bmatrix} \begin{bmatrix} X \\ V \end{bmatrix} + \begin{bmatrix} J \\ 0 \end{bmatrix} \quad (8)$$

Then the so-called LUD-type SFG and corresponding active-RC implementation can be obtained according to eqn. 8 (see Fig. 3). This circuit configuration with altered component values can also realise an 8th order bandpass filter. No feed-through loop exists in the circuit. Only in the lowpass case is one extra op-amp required when compared with the leapfrog approach. In other cases the number of amplifiers can be made canonical.

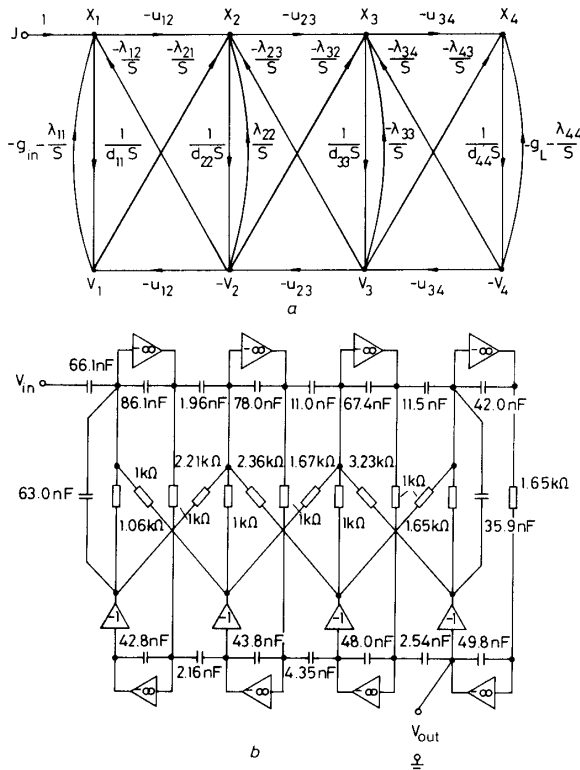


Fig. 3 LUD type simulation of circuit in Fig. 2a
a Diagram
b Corresponding active-RC realisation (scaled for maximum dynamic and denormalised, 3.4 kHz)

For a prototype with more loops than nodes, it is possible to start with a loop description of the network instead of eqn. 1. In more general cases, hybrid descriptions of the prototype can be used.

4 The LUD and leapfrog (LL) approach for discrete systems

It is now logical to examine the application of this theory to discrete implementations. To afford some means of comparison with existing approaches, Fig. 4 shows cascaded biquad and wave digital realisations of a standard

elliptic filter (Fig. 2a). Both the biquad and wave filters are canonical in terms of the number of multipliers whereas the wave digital filter requires a higher number of additions and delays and offers a slower speed of operation because multiplications must be performed in some hierarchical sequence [1, 9]. This Section will develop new structures which offer some noteworthy improvements.

4.1 Standard LL discrete system

Perform the bilinear transform on eqn. 1 (let sampling period $T = 2$ s for simplicity)

$$\left(\frac{1-z^{-1}}{1+z^{-1}} C + \frac{1+z^{-1}}{1-z^{-1}} \Gamma + G \right) V = J \quad (9)$$

To produce a system without delay-free loops, the following manipulations are required. Eqn. 9 is equivalent to

$$\left(A + \frac{4z^{-1}}{(1-z^{-1})^2} \Gamma + \frac{2z^{-1}}{1-z^{-1}} G \right) V = \frac{1+z^{-1}}{1-z^{-1}} J \quad (10a)$$

with

$$A = C + \Gamma + G \quad (10b)$$

For simplicity rewrite eqn. 10a as

$$(A + \Psi\Phi 4\Gamma + \Psi 2G)V = \Psi(1+z)J \quad (11)$$

with

$$\Psi = z^{-1}/(1-z^{-1}) \quad (12a)$$

$$\Phi = 1/(1-z^{-1}) \quad (12b)$$

It is interesting that Ψ and Φ constitute a pair of LDI integrators [4]. The relationship between bilinear and 'exact' LDI transformed systems is discussed elsewhere [11]. As matrix A is always symmetric, it can also be decomposed into the form

$$A = U^T D U \quad (13)$$

where D is used in the same way as in eqn. 5 and let $U = I + U_{\text{offd}}$. This leads to the discrete LUD system

$$\begin{bmatrix} X \\ V \end{bmatrix} = \begin{bmatrix} -U_{\text{offd}}^T & -(\Phi 4\Gamma + 2G) \\ \Psi D^{-1} & -U_{\text{offd}} \end{bmatrix} \begin{bmatrix} X \\ V \end{bmatrix} + \begin{bmatrix} (1+z)J \\ 0 \end{bmatrix} \quad (14)$$

The corresponding SFG is shown in Fig. 5, and is suitable for SC realisation [10]. The realisation of input function $(1+z)$ can be accomplished by multiplying by z^{-1} giving $(1+z^{-1})$, but introducing a delay of one period.

For digital realisation Γ can be decomposed as in the leapfrog method, $\Gamma = A_L D_L A_L^T$, in this way the number of multiplications is reduced. The corresponding standard LL (LUD-leapfrog) can be realised directly by the circuit shown in Fig. 6a.

Now it is essential to take into consideration some factors related to the operation speed. Let

$$m = \text{order of the filter} \quad (15a)$$

$$n = \text{number of nodes of the prototype} \quad (15b)$$

$$T_s = \text{sampling period} \quad (15c)$$

$$T_m = \text{time for one multiplication operation} \quad (15d)$$

$$T_a = \text{time for one addition operation} \quad (15e)$$

For an ordinary odd-order lowpass RLC ladder, $m = 2n - 1$. Examining eqns. 15 and Fig. 6a carefully, it

can be seen that when the transfer factors $\{c_i\}$ of the horizontal branches in Fig. 6a are general numbers, the oper-

along horizontal branches must be performed serially, for the upper line from left to right and for the lower line

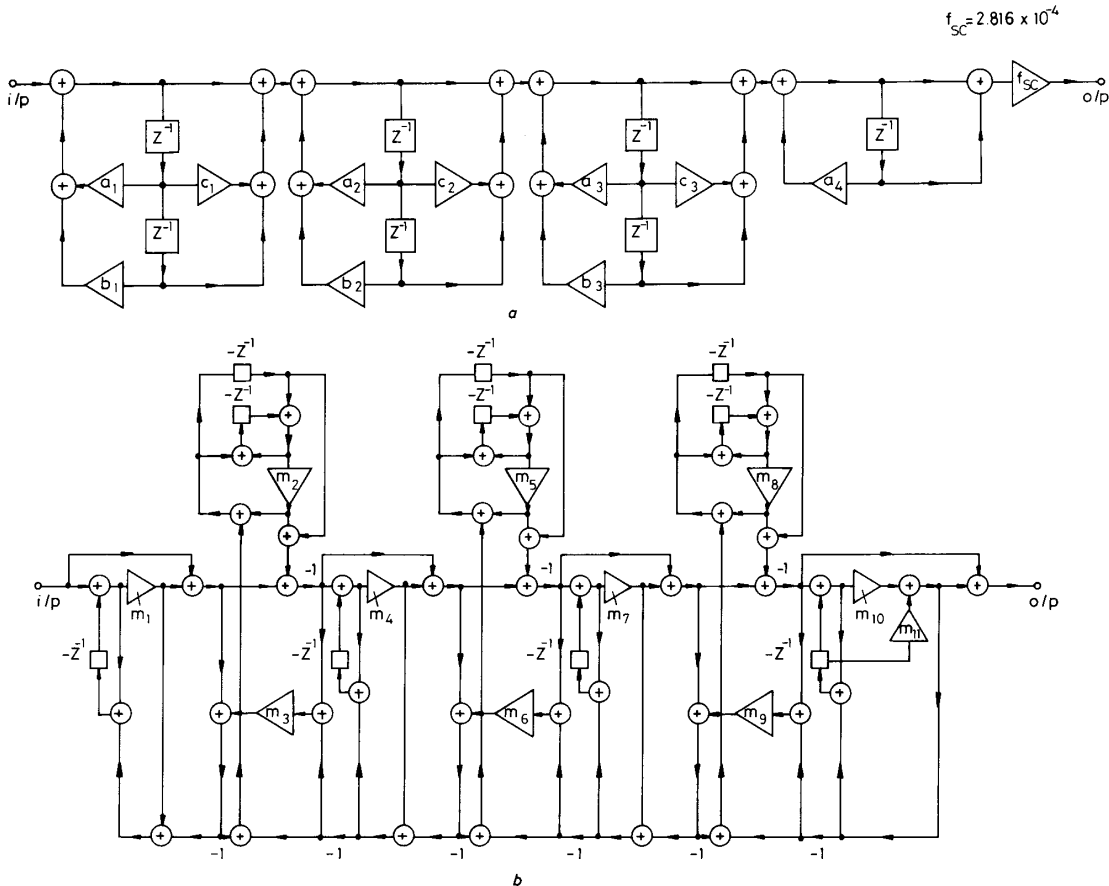


Fig. 4 Realisations of the elliptic filter

a Cascade biquadratic digital realisation

$$\begin{aligned} a_1 &= 1.498 & b_1 &= 0.6331 & c_1 &= 0.3442 \\ a_2 &= 1.488 & b_2 &= 0.7751 & c_2 &= -1.013 \\ a_3 &= 1.522 & b_3 &= 0.9252 & c_3 &= -0.7097 \\ a_4 &= 0.7541 & & & & \end{aligned}$$

b Wave digital realisation

$$\begin{aligned} m_1 &= -0.7748 & m_5 &= -0.7532 & m_9 &= 0.1203 \\ m_2 &= -0.4140 & m_6 &= 0.1511 & m_{10} &= -0.6899 \\ m_3 &= 0.08522 & m_7 &= -0.8550 & m_{11} &= -0.5811 \\ m_4 &= -0.9366 & m_8 &= -0.6774 & & \end{aligned}$$

ation speed is limited by

$$T_s \geq \frac{m+5}{2} \cdot T_a + \frac{m+1}{2} \cdot T_m \quad (16)$$

because in every period, additions and multiplications

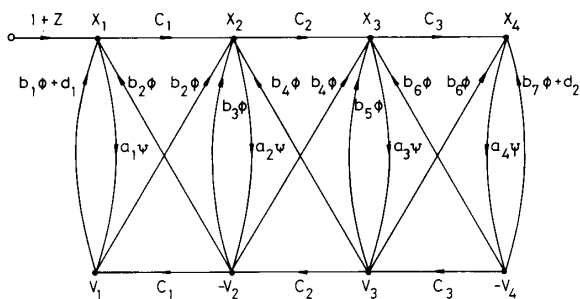


Fig. 5 LUD-type SFG for the elliptic filter

$$\begin{aligned} a_1 &= 0.2056 & b_1 &= -0.9668 & c_1 &= -0.0850 \\ a_2 &= 0.1420 & b_2 &= -0.9668 & c_2 &= -0.1509 \\ a_3 &= 0.1412 & b_3 &= -2.011 & c_3 &= -0.1201 \\ a_4 &= 0.2070 & b_4 &= -1.045 & & \\ b_5 &= -2.138 & d_1 &= -2 & & \\ b_6 &= -1.093 & d_2 &= -2 & & \\ b_7 &= -1.093 & & & & \end{aligned}$$

from right to left. Since $T_m \gg T_a$, the limit is dominated by the multiplication time. In the following we shall show some strategies to improve this limitation on operation speed.

4.2 Modified LL system

The limitation given by eqn. 16 can be reduced by scaling all nonzero elements in U to the nearest powers of 2, as the operation required to multiply a number by 2^{-k} is simply to shift it by k bits. It is also possible to scale all nonzero entries in U to ± 1 s, but this results in a very large coefficient spread, which is undesirable. The scaling procedure can be performed in terms of matrix transformations. Let S be a diagonal constant matrix, pre- and post-multiply the matrices in eqn. 11 by S . Let

$$\begin{aligned} A_s &= SAS & B_s &= SA_L 4D_L A_L^T S & G_s &= S2GS \\ V_s &= S^{-1}V & J_s &= SJ \end{aligned} \quad (17)$$

A new system is obtained with a transfer function differing from that of eqn. 11 only by a constant.

$$(A_s + \Psi\Phi B_s + \Psi G_s)V_s = \Psi(1+z)J_s \quad (18)$$

Scaling is carried out so that A_s will decompose into

$$A_s = U_s^T D_s U_s \quad (19)$$

where every diagonal element of U_s is 1 and also the upper-diagonal elements are powers of 2. It can be verified that this procedure is possible provided A_s is tri-diagonal, which is always the case for a ladder structure.

According to the decomposition of B_s , several systems can be obtained as listed in the following:

(i) Type M1 (Fig. 6b)

Use the straightforward decomposition of B_s according to eqn. 17:

$$B_s = SA_L 4D_L A_L^T S \quad (20)$$

In the lowpass case there are $(n-1)$ inductors in the prototype (Fig. 2a). D_L is $(n-1) \times (n-1)$ and A_L is $n \times (n-1)$. This also means that the rank of B_s is at

most $n-1$, which is an important property related to the system behaviour at $\omega = 0$, as shown in the next Section.

(ii) Type M2 (Fig. 6c)

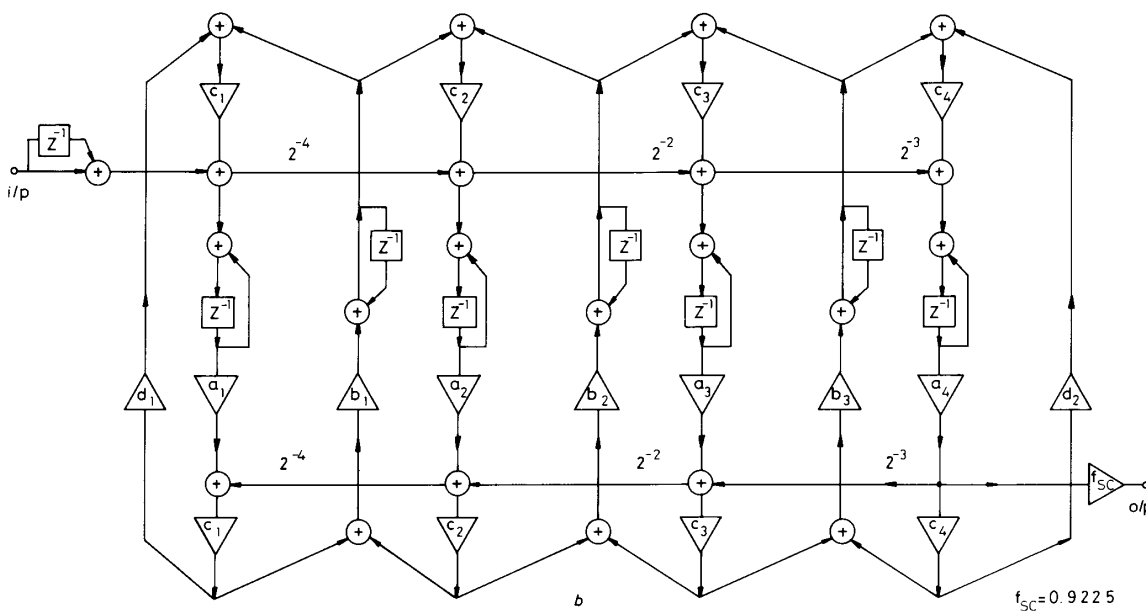
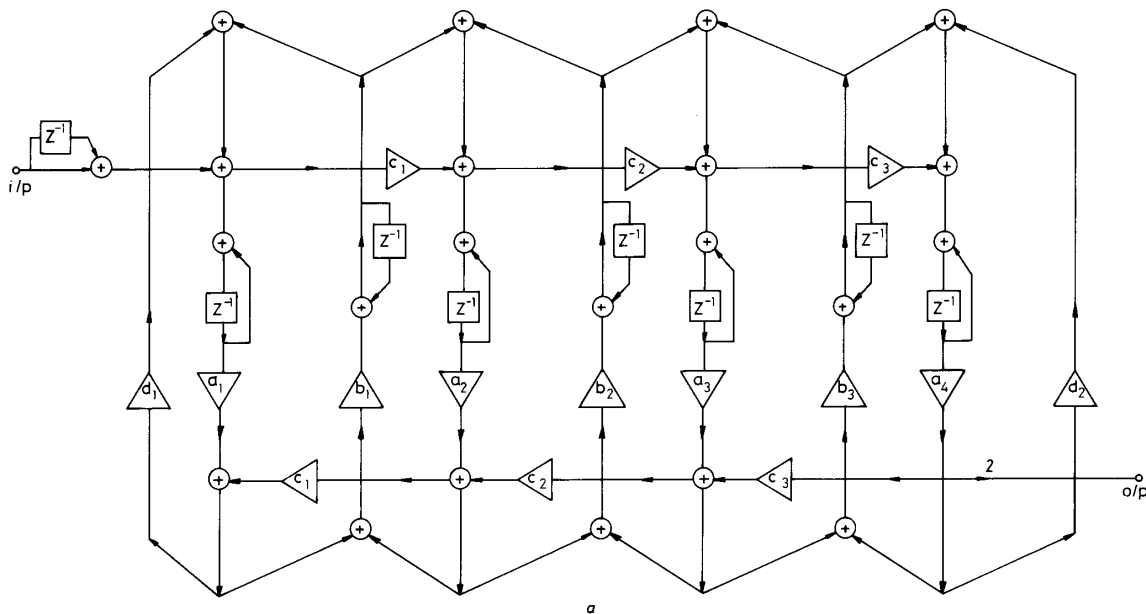
LU decomposition can also be performed on B_s

$$B_s = U_b^T D_b U_b \quad (21)$$

with diagonal entries of U_b being 1. As just mentioned, the rank of B_s is $n-1$, so that at the last step of LU decomposition the pivot is zero. In this case D_b and U_b can be expressed in $(n-1) \times (n-1)$ and $(n-1) \times n$ matrices, respectively.

(iii) Type M3 (Fig. 6d)

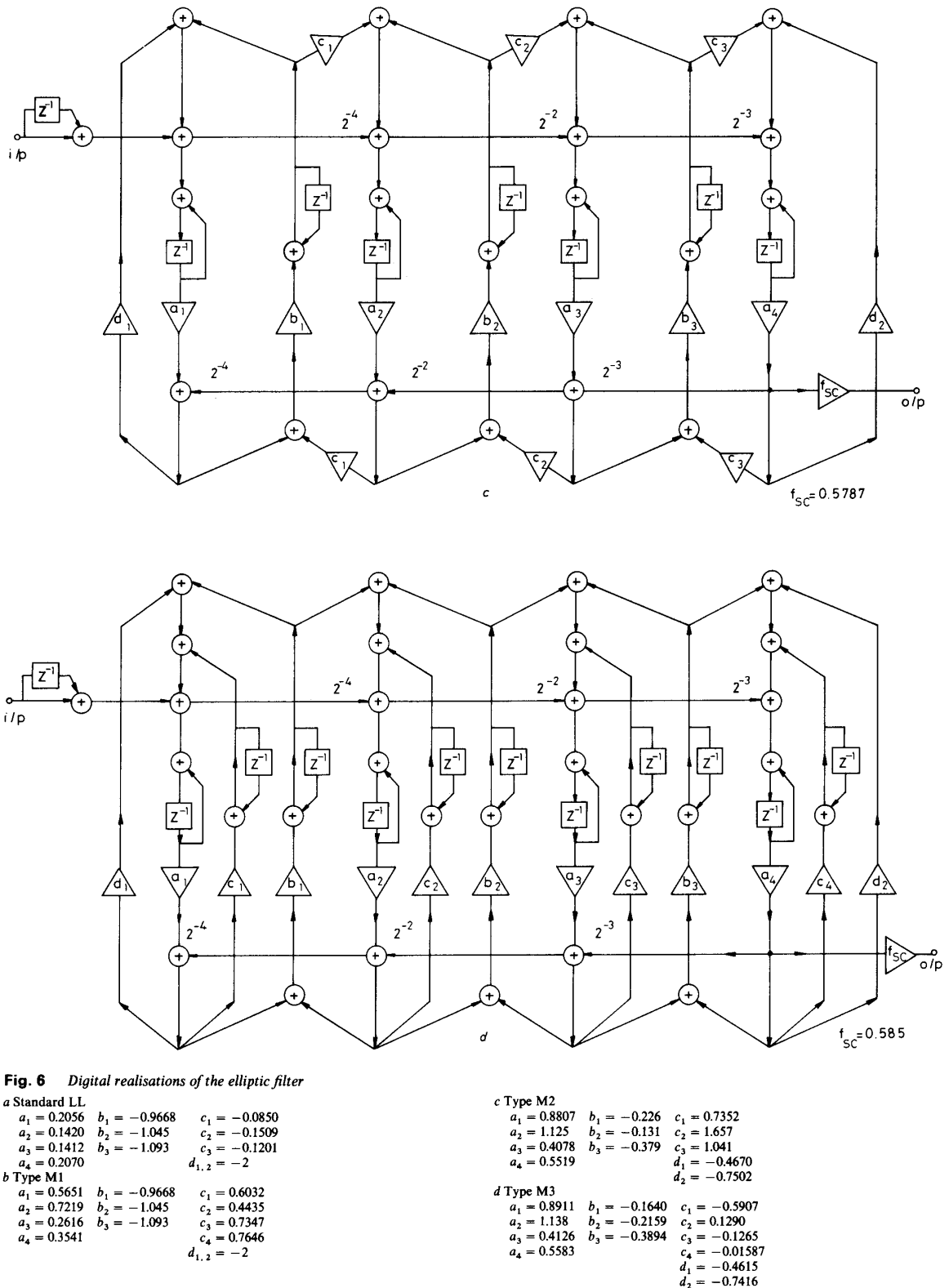
$$B_s = A_b D_b A_b^T + D_m \quad (22)$$



with all entries of A_b being either 1 or -1 . It will be shown that although this type of circuit has an improved speed limitation, it has high sensitivity at $\omega = 0$.

4.3 Examples

The following example illustrates the design procedures for a Standard LL and a Type M1 circuit. For the



passive network, Fig. 2a, eqn. 1 becomes

$$\left\{ s \begin{bmatrix} 3.62 & 0.171 & & \\ 0.171 & 6.57 & 0.802 & \\ & 0.802 & 6.71 & 0.577 \\ & & 0.577 & 3.66 \end{bmatrix} + s^{-1} \begin{bmatrix} 0.242 & 0.242 & & \\ 0.242 & 0.503 & 0.261 & \\ & 0.261 & 0.535 & 0.273 \\ & & 0.273 & 0.273 \end{bmatrix} + \begin{bmatrix} 1 & & & \\ & 0 & & \\ & & 0 & \\ & & & 1 \end{bmatrix} \right\} V = \begin{bmatrix} J_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

where $V = [v_1, -v_2, v_3, -v_4]^T$. Let $s = (1 - z^{-1}) / (1 + z^{-1})$ and follow the procedure eqns. 9-14. The relevant matrices are

$$A = \begin{bmatrix} 1 & & & \\ 0.085 & 1 & & \\ & 0.151 & 1 & \\ & & 0.121 & 1 \end{bmatrix} \begin{bmatrix} 4.86 & & & \\ & 7.04 & & \\ & & 7.08 & \\ & & & 4.83 \end{bmatrix} \times \begin{bmatrix} 1 & 0.085 & & \\ & 1 & 0.151 & \\ & & 1 & 0.121 \\ & & & 1 \end{bmatrix} \quad (24a)$$

$$4\Gamma = \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \\ & & & 1 \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \\ & & & 1 \end{bmatrix} \quad (24b)$$

$$2G = \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \quad (24c)$$

The standard LL realisation can now be drawn (Fig. 6a).

To produce a type M1 realisation, continue by choosing the scaling matrix S (from eqn. 17)

$$S = \text{diag} [0.603, 0.444, 0.735, 0.765] \quad (25)$$

Then for eqns. 17-20

$$A_s = SAS = U_s D_s U_s^T = \begin{bmatrix} 1 & & & \\ 2^{-4} & 1 & & \\ & 2^{-2} & 1 & \\ & & 2^{-3} & 1 \end{bmatrix} \times \begin{bmatrix} 1.77 & & & \\ 1.39 & & & \\ & 3.82 & & \\ & & 2.82 & \end{bmatrix} \begin{bmatrix} 1 & 2^{-4} & & \\ & 1 & 2^{-2} & \\ & & 1 & 2^{-3} \\ & & & 1 \end{bmatrix}$$

$$B_s = S4\Gamma S = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \times \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \\ & & & 1 \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \\ & & & 1 \end{bmatrix} \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix}$$

$$G_s = S2GS = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \times \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \quad (26)$$

The type M1 realisation shown in Fig. 6b follows immediately.

4.4 Comments

Since the transfer coefficients of the horizontal branches in Figs. 6b-d are all 2^k , and assuming shift and add has the same cost as addition, then for M1 and M2 the operation speed is limited by

$$T_s \geq \frac{m+5}{2} T_a + 3T_m \quad (27)$$

and for M3 the limit is given by

$$T_s \geq \frac{m+5}{2} T_a + 2T_m \quad (28)$$

All these new systems demonstrate a high degree of parallelism [1], and types M1 and M2 will show low sensitivity; thus a combination of the features of the biquad cascade and the wave filters is possible. As these new structures only use some simple matrix operations (see eqn. 14), they are particularly attractive in the case where an array processor is available.

It is important to distinguish between the number of multiplications and the number of multiplication coefficients to be stored in the new structure. Traditionally, in biquad and wave realisations these two processes are inextricably linked. In some of these new methods (standard LL, types M1 and M2), because of their symmetrical structures, two identical multiplications $\{c_i\}$ can be undertaken serially by one multiplier. For hardware implementation, therefore, the number of multipliers required is nearly cononical for these circuits. The adders can be shared in a similar way.

The methods introduced in this Section can be applied directly to bandpass but not to highpass and bandstop design. The difficulty is that for these latter cases the transfer function is not of zero value at $z = -1$ (corresponding to $s = \infty$ in continuous domain). However, the input function of eqn. 14, $(1 + z^{-1})|_{z=-1} = 0$. This implies that the transfer function from $(1 + z)J$ to the output must be infinite at $z = -1$ to facilitate cancellation, which inevitably results in an unstable system. For the highpass case this difficulty can be overcome by using a frequency transformation of $z^{-1} \rightarrow -z^{-1}$ to obtain the desired system from a lowpass

reference. For the bandstop case some different techniques are adopted which are beyond the scope of this paper.

5 Comparison of the various approaches

In the above Sections four types of digital filters simulating passive ladders have been proposed (standard LL and types M1–M3). Now they are compared with each other as well as with cascade biquad and wave realisations.

5.1 Sensitivity estimates

When the coefficient matrices in eqns. 11 and 18 are realised by digital circuits, they will deviate from their ideal values owing to finite wordlength. This also happens when they are realised by SC circuits, owing to element deviations. It is observed that the sensitivities of all four types of circuits differ most significantly at $\omega = 0$. This effect is now explained mathematically.

Making the standard substitution

$$j\Omega = j \tan(\omega T/2) = \frac{1 - z^{-1}}{1 + z^{-1}} \Big|_{z = e^{j\omega T}} \quad (29)$$

eqn. 9 becomes

$$[j(\Omega C - \Omega^{-1}\Gamma) + G]V = J \quad (30)$$

Denote

$$Y = j(\Omega C - \Omega^{-1}\Gamma) + G \quad (31)$$

Use the following properties, which always hold true for a nodal description of a passive ladder (eqn. 1):

(a) C , Γ and G are all tri-diagonal matrices; hence, Y is also tri-diagonal

(b) J has only one nonzero element, i.e. $J = (J_{in}, 0, \dots, 0)$

(c) G has only two nonzero elements $g_{11} = g_{in}$ and $g_{nn} = g_L$

(d) output is the nodal voltage v_n .

From these properties and Cramer's rule it can be found for output v_n

$$v_n = \frac{\prod_{i=1}^{n-1} [j\Omega c_{(i+1,i)} - (j\Omega)^{-1} \gamma_{(i+1,i)}]}{\det |Y|} J_{in} \quad (32)$$

where $\Gamma = \{\gamma_{(i,j)}\}$ and $C = \{c_{(i,j)}\}$.

It can be shown that when $\Omega \rightarrow 0$,

$$\det |Y| \rightarrow (j\Omega)^{-n} \det(\Gamma) + (j\Omega)^{-(n-1)} [g_{11} \det(\Gamma)_{11} + g_{nn} \det(\Gamma)_{nn}] + (j\Omega)^{-(n-2)} \quad (33)$$

By comparing the power of $(j\Omega)^{-1}$ in the denominator and numerator it can be seen that in order to retain the output v_n nonzero, the coefficient of $(j\Omega)^{-n}$ in $\det |Y|$ must be zero. This leads to the following:

Remark: The system given in eqn. 30 has nonzero response at $\Omega = 0$ only if Γ is singular. The response is given by

$$v_n = \frac{\prod_{i=1}^{n-1} \gamma_{(i+1,i)}}{g_{11} \det(\Gamma)_{11} + g_{nn} \det(\Gamma)_{nn}} J_{in} \quad \text{at } \Omega = 0 \quad (34)$$

Otherwise, if Γ is nonsingular, then $v_n = 0$ at $\Omega = 0$.

Using this result for a lowpass filter, it would seem mandatory to ensure that Γ is singular. However, for LUD it is easily seen that deviation in the entries of Γ may cause it to become nonsingular; this is also true for type M3 from the relation that $\Gamma = S^{-1}(B_s/4)S^{-1}$. Only Standard LL, M1 and M2 will always guarantee singular Γ or B_s , whatever the deviation in entries, since the decompositions of Γ or B_s in these three structures involve multiplications of matrices with only $(n-1)$ rows or columns. The resulting matrices can never have rank greater than $n-1$.

Incidentally, the extra zeros introduced at the origin can be viewed as an advantage or disadvantage according to the filter application; for instance, low-frequency noise suppression can be facilitated by these zeros.

5.2 Implementation cost

Table 1 gives a comparison of the implementation cost of the various types of digital filter proposed in this paper, as well as for the biquad and wave filters used for reference. It can be seen that type M3 is a special case. In the remaining five structures the numbers of multiplier coefficients to be stored are roughly equal. For the number of additions, delays and speed of operation, the biquad approach appears best, the wave filter is worst, with Standard LL, M1 and M2 being in between these extremes.

The lower limitation on T_s for the cascade biquad is achieved by assuming that a delay is inserted between every successive biquad block, so ensuring independent processing of the signal, but this increases the signal delay between input and output.

If adders are time-shared, then the numbers required for LL and its derived types can be much less than the numbers of additions listed in Table 1. For example, the minimum number of adders for type M1 is $(m+1)/2$, provided that other relevant figures in Table 1 are kept unchanged.

Table 1: Comparison of implementation cost and operation speed of various digital realisations for an odd-order lowpass elliptic function

Function	Cascade biquad	Wave	Standard LL	Type M1	Type M2	Type M3
Number of additions	$2m$	$6m - 2$	$3m + 1$	$3m + 1$	$3m + 1$	$\frac{7m + 5}{2}$
Number of multiplier coefficients to be stored (scale factor f_{sc} not included)	$\frac{3m - 1}{2}$	$\frac{3m + 1}{2}$	$\frac{3}{2}(m + 1)$	$\frac{3m + 5}{2}$	$\frac{3}{2}(m + 1)$	$\frac{3m - 5}{2}$
Number of delays	m	$\frac{3m - 1}{2}$	$m + 1$	$m + 1$	$m + 1$	$\frac{3m + 4}{2}$
Lower bound on T_s (T_m and T_a are multiplication and addition times, respectively)	$2T_a + T_m$	$3mT_a + mT_m$	$\frac{m + 5}{2} T_a + \frac{m + 1}{2} T_m$	$\frac{m + 5}{2} T_a + 3T_m$	$\frac{m + 5}{2} T_a + 3T_m$	$\frac{m + 7}{2} T_a + 2T_m$

m = order of function

5.3 Design examples

In Fig. 7 the ideal response of a bilinear transformed digital elliptic lowpass response is given. Its prototype is simply the lowpass ladder in Fig. 2a (C-071536 Saal notation [16]). All six type digital structures are simulated using the same prototype. Sampling frequency is 32000 Hz. It is assumed that floating-point storage of coefficients is used. All the coefficients are truncated to the nearest smaller number.

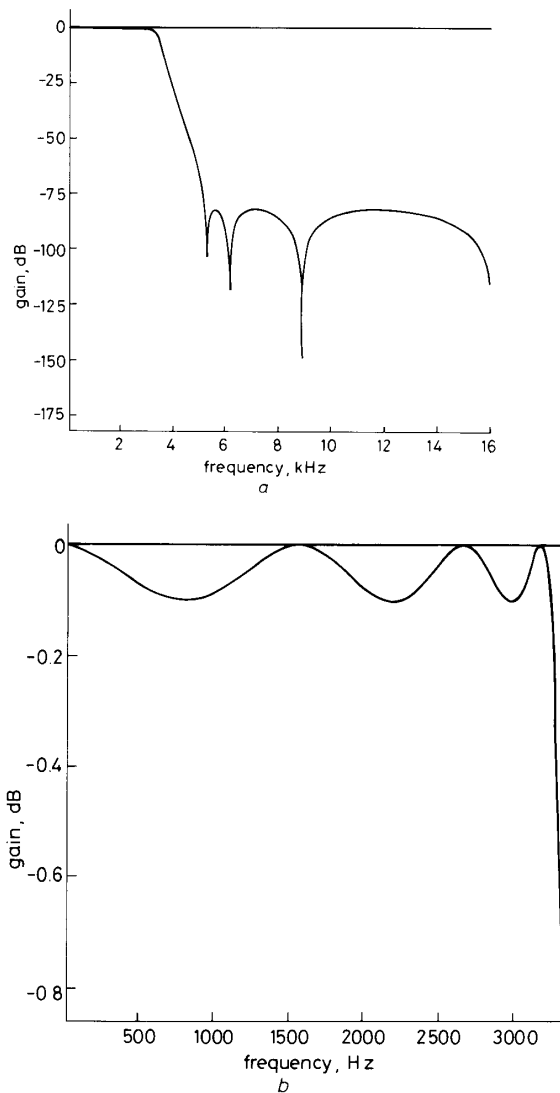


Fig. 7 Ideal response of elliptic filter
a Overall ideal response (wave digital with 16 bits)
b Ideal passband response of elliptic filter

The detailed passband responses for 8-bit implementation given in Fig. 8 show that a droop at zero-frequency occurs for type M3 and quite serious overall distortion for the biquad, whereas all other responses are almost ideal. When the wordlength is reduced to 4 bits, the overall filter response for wave and M1 is retained with reasonable accuracy while biquad response variation is dramatic, Fig. 9. The passband detail comparison of wave, M1, M2 and M3 realisation with 4 bits is also shown in Fig. 10. The zero-frequency droop exhibited by type M3 supports the mathematical prediction.

6 Conclusions

A new approach to the simulation of passive filter structures by active-RC and digital means has been developed. A detailed comparison of the various digital implementations has been undertaken and reveals that although the sensitivity of a wave digital filter is usually optimum, it can be approached by types standard LL, M1 and M2. However, in practical realisations types M1 and M2 will out-perform all others, apart from the biquad, in terms of speed of operation and number of additions and delays. For increased order, the wave filter shows linear increases in both multiplication and addition times, whereas the alternatives have a linear dependence only in addition time. So for sensitivity, speed of operation and cost of implementation, the new structures offer attractive possibilities, especially for high order realisations.

The scaling technique introduced in modified LL types in this paper may also find useful application in other digital filter implementations, and is worthy of further investigation.

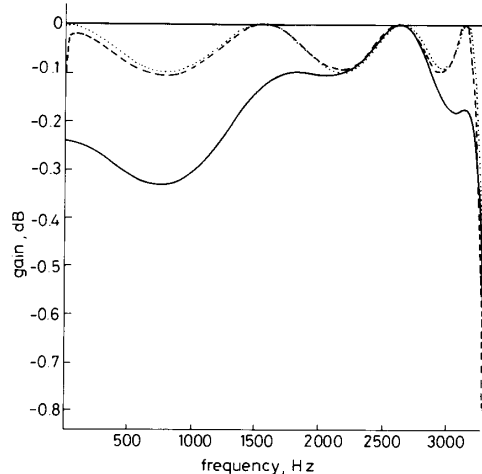


Fig. 8 Filter passband responses with 8-bit digital realisation
 — Biquad
 - - - M3
 ····· Wave, M1, M2

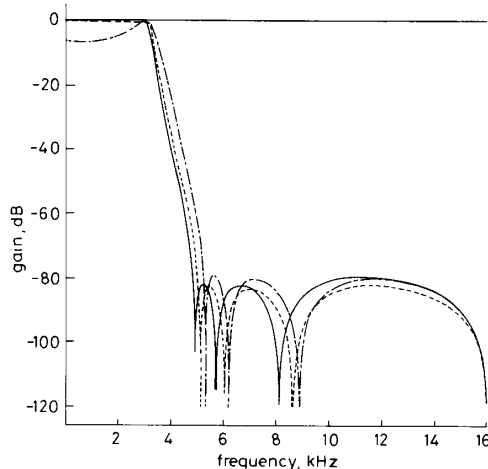


Fig. 9 Overall frequency response of elliptic filter with 4-bit digital realisation
 — M2
 - - - Wave
 ····· Biquad

The problem of truncation error analysis in these new structures is a more complex study and is the subject of future work.

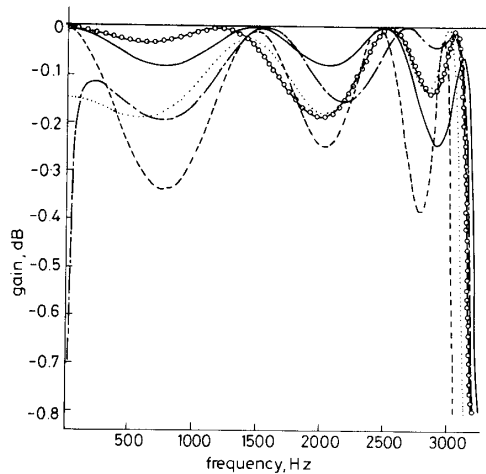


Fig. 10 Filter passband responses with 4-bit digital realisation

○—○ Wave
 — Standard LL
 - - - Type M1
 - · - Type M3
 ····· Type M2

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