

TABLE I
ELECTRONIC CHARACTERISTICS OF THE 8×8 NEURAL NET

	G_0	u_{thr}	ρ	γ	C_0
Mean Value	108	-70 mV	510 K Ω	4 ns	2 pF
Distribution	5%	10%	96%	5%	-

TABLE II
PERFORMANCE ESTIMATION OF THE 8×8 NEURAL NET CONTROLLER

Average rank	Average Efficiency	Throughput	Analog Computation
8	98%	120ns	120ns
6	99.66%	120ns	120ns
4	100%	120ns	120ns
2	100%	120ns	120ns

totally optimal configuration matrices, the analog computation which results from the set of synaptic weights of (4) leads to very satisfactory throughput performance.

IV. REAL-TIME SIMULATION AND OPTIMIZATION OF AN 8×8 NEURAL NET CONTROLLER

Given an arbitrary input request matrix, the problem of maximizing the throughput of the crossbar reduces to finding numerical values for the set of synaptic weights defined in (4), and the characteristics of the amplifiers of an $N \times N$ neural net which would compute optimal configuration matrices in the least amount of time. It is clearly impossible to simulate the analog computation of a configuration matrix for each of the $2^{N^2} N \times N$ binary matrices. For $N=8$, there are already of the order of 10^{19} possible input request matrices. In order to estimate the performance of the net, we have generated separate subsets of 500 input request matrices by choosing their matrix elements to be "1" with a probability χ and "0" with a probability $1-\chi$, χ being a positive number between 0 and 1. Within each subset, the analog computation of a configuration matrix associated to each input request matrix has been real-time simulated by integrating on a VAX 8650 the set of coupled differential equations (1). The selected electronic characteristics of a VLSI implementation of the neural cells are reported in Table I for the $2\text{-}\mu\text{m}$ CMOS technology.

In Table I, G_0 , u_{thr} , ρ and γ denote the average gain, offset, input resistance and propagation delay of the amplifiers respectively, and C_0 is the capacitance per connection. Such a distribution of the input resistances of the neurons is chosen in order to break the symmetry of the neuron time-constants so as to enhance the performance of the neural dynamics.

For $N=8$, the resistances between neurons of the same row and the same column have been randomly chosen distributed around 4 k Ω within 1 percent. The initial voltages of the "free" neurons have been randomly distributed in the interval $[-2.5\text{ mV}, +2.5\text{ mV}]$ around the ground potential. The stability of the analog computation with respect to noise has been tested by simulating, at the input of each inverter, a white noise gaussianly distributed around 0 V with a standard deviation of 10 μV . With this set of parameters and initial conditions, the time-evolution of the 8×8 neural net controller has been simulated for a period of 120 ns. The results of the simulation are reported in Table II for subsets of input request matrices having an average rank of 2, 4, 6, and 8 respectively. (The rank of an input request matrix being

interpreted here as the maximum total number of packets that can be transmitted through the crossbar switch without destructive interference.)

The statistical estimations reported in Table II indicate that an 8×8 neural net controller which has the above characteristics is expected to compute configuration matrices within a period of 120 ns, and with at least 98 percent of average throughput efficiency.

V. CONCLUSIONS

This letter has demonstrated the efficiency of neural networks to arbitrate the packets at the input of an 8×8 crossbar switch with nearly optimal throughput performance. The proposed architecture computes configuration matrices in a lapse of time of approximately 100 ns, with an average throughput efficiency of at least 98 percent.

The number of neural interconnections of this architecture is of the order of N^3 (instead of N^4 for a fully connected neural net), N being the dimension of the crossbar. This reduction in the number of neural interconnections will facilitate hardware implementation of the proposed neural net arbitrator with VLSI technology, and perhaps of larger size controllers, e.g., 16×16 . As for the 8×8 , the resistance of the larger neural nets can be optimized through computer simulations of the real-time evolution of their neurons for various samplings of the input request matrices.

Finally, in view of the simplicity of this architecture, i.e., synaptic weights having the same sign and absence of external input currents, an implementation based on opto-electronic or photonic technologies would probably be more suitable for the larger size and faster switch controllers.

ACKNOWLEDGMENT

The authors are indebted to Dr. S. M. Walters for suggesting the problem and for stimulating discussions.

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The TWINTOR in Bandstop Switched-Capacitor Ladder Filter Realization

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Abstract—A new design for strays-insensitive bandstop switched-capacitor (SC) ladder filter structures is introduced. A two channel scheme obviates the need for term cancellation in realizing bandstop-type operators and is less demanding on opamp settling time.

Manuscript received November 9, 1988. This letter was recommended by Associate Editor T. R. Viswanathan.

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IEEE Log Number 8926456.

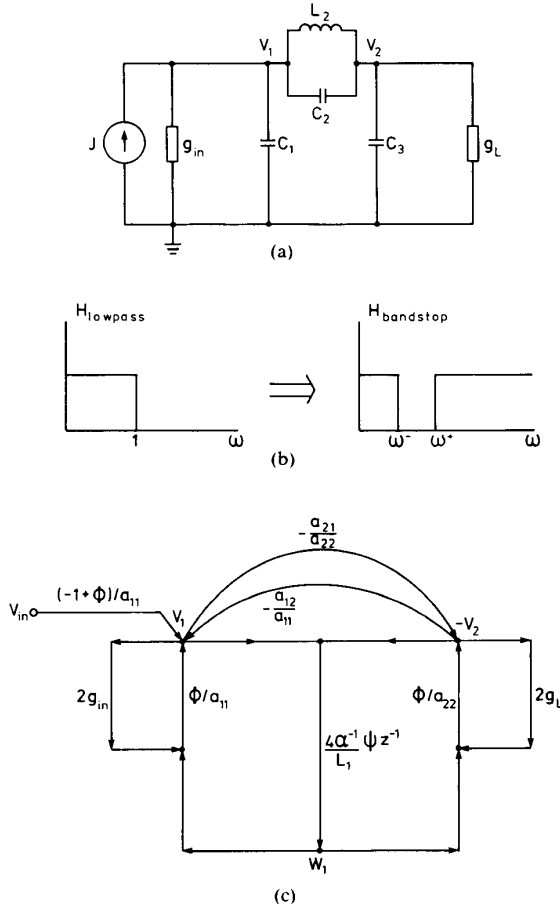


Fig. 1. (a) A third-order normalized low-pass ladder. (b) Low-pass to bandstop transformation. (c) The signal flowgraph of leapfrog-type simulation.

I. INTRODUCTION

Switched-capacitor (SC) filter structures based on passive ladder simulations have attracted much attention because of their low sensitivity properties. However, an instability problem exists in the design of bandstop SC ladders by stray-insensitive LDI integrators [1]. A second-order building block technique has been proposed in [2] to overcome this difficulty.

In this paper a new type of second-order building-block called a TWINTOR (TWinned INTEGRATOR) is introduced for bandstop SC ladder design. The circuit uses two signal channels to directly realize the basic bandstop operators without term cancellations [2], and also reduces the required opamp operation speed by a factor of two. Either single-input or differential-input integrators are allowed, giving flexibility for fabrication.

II. THE TWINTOR CIRCUIT

Following a matrix leapfrog method [3], [4] a passive low-pass reference RLC ladder, Fig. 1(a), is described by the nodal admittance matrix equation

$$\left(sC + \frac{1}{s} \Gamma + G \right) = V = J \quad (1)$$

where C , Γ , and G are admittance matrices formed by the contributions of capacitors, inductors, and resistors, respectively. The voltage vector $V = [v_1, -v_2, v_3, -v_4, \dots]$ to ensure all the

entries of the matrices non-negative. It is well known that in the continuous-time domain a symmetric bandstop function can be derived from a normalized low-pass one by transformation [5], (see Fig. 1(b)):

$$s \rightarrow a^{-1} \left(\frac{s}{\omega_m} + \frac{\omega_m}{s} \right)^{-1} \quad (2)$$

with

$$a = \frac{\omega_m}{\omega^+ - \omega^-}, \quad \omega_m = \sqrt{\omega^+ \omega^-}.$$

Substitute (2) into (1) and perform the bilinear transformation $s = 2(1 - z^{-1})/T(1 + z^{-1})$,

$$\left\{ a^{-1} \left(\frac{2}{\omega_m T} \frac{1 - z^{-1}}{1 + z^{-1}} + \frac{\omega_m T}{2} \frac{1 + z^{-1}}{1 - z^{-1}} \right)^{-1} C + a \left(\frac{2}{\omega_m T} \frac{1 - z^{-1}}{1 + z^{-1}} + \frac{\omega_m T}{2} \frac{1 + z^{-1}}{1 - z^{-1}} \right) \Gamma + G \right\} V = J. \quad (3)$$

Multiply through (3) by the coefficient of Γ and rearrange to give

$$(A - 4\alpha z^{-1} \Psi \Phi \Gamma - \Phi 2G) = (-1 + \Phi) J \quad (4)$$

where

$$\Phi = (\beta z^{-1} - 1)/(1 - z^{-2})$$

$$\Psi = (z^{-1} - \beta)/(1 - z^{-2})$$

$$A = \alpha^{-1} C + \alpha \Gamma - \Gamma - G$$

with

$$\mu = \omega_m T/2$$

$$\alpha = a(\mu^{-1} + \mu)$$

$$\beta = (\mu^{-1} - \mu)/(\mu^{-1} + \mu).$$

Topologically, decompose Γ into

$$\Gamma = A_L D_L A_L^T \quad (5)$$

where A_L is an incidence matrix of the inductors in the ladder, D_L is a diagonal matrix of reciprocal inductance values. With this (4) can be rewritten in the form

$$\begin{cases} AV = \Phi(A_L W + 2GV) + (-1 + \Phi) J & (6a) \\ W = 4\alpha^{-1} z^{-1} \Psi D_L A_L^T V & (6b) \end{cases}$$

A signal flowgraph can be drawn to represent (6), Fig. 1(c) which can be replaced by a SC circuit. The frequency-dependent operators Ψ and Φ given by (4) are realized with a new TWINTOR second-order strays-insensitive biquad scheme, Fig. 2(a). In a TWINTOR each opamp is operated only in every other period, T . The charge relations for the circuit of Fig. 2(a) are

$$C_e [y^e(n) - y^e(n-2)] = -C_1 x^e(n) + C_2 x^0(n-1) \quad \text{when } n \text{ even} \quad (7a)$$

$$C_3 [y^0(n) - y^0(n-2)] = -C_1 x^0(n) + C_2 x^e(n-1) \quad \text{when } n \text{ odd.} \quad (7b)$$

Therefore, the overall transfer function is given by

$$Y(z) = \frac{1}{C_3} \frac{C_2 z^{-1} - C_1}{1 - z^{-2}} X(z). \quad (8)$$

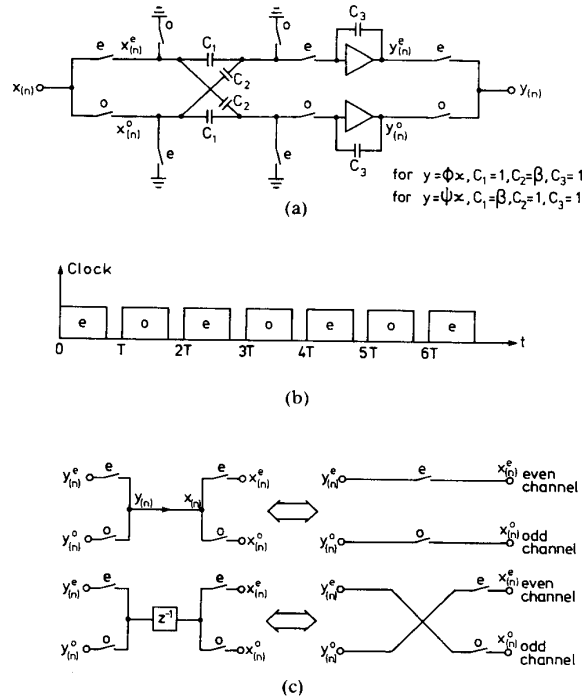


Fig. 2. (a) A TWINTOR circuit. (b) The clock waveform. (c) Two channel equivalent connectors of TWINTOR's.

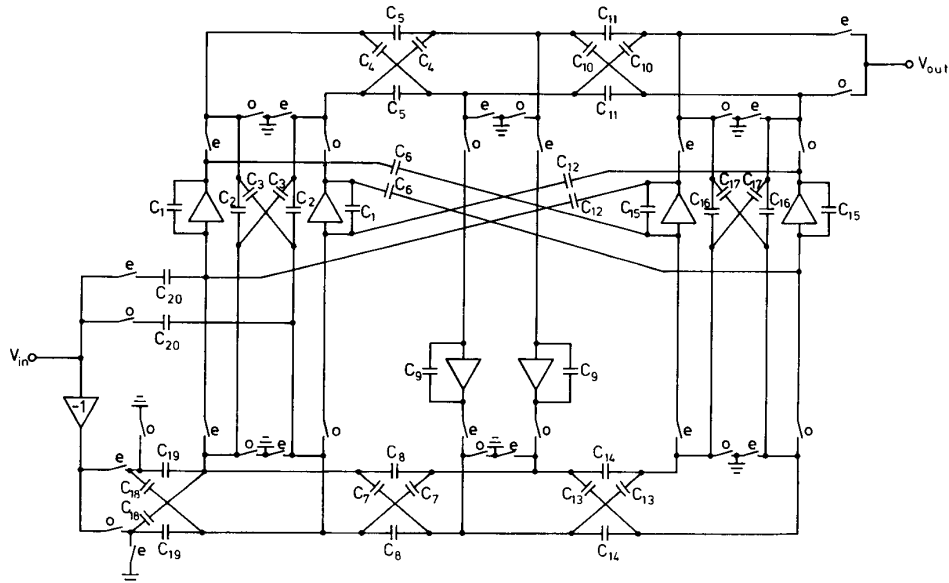


Fig. 3. A sixth-order bandstop SC bichannel filter realization.

Notice that the denominator $(1 - z^{-2})$ is exactly realized without term cancellation.

It can be seen from Fig. 2(b) that now the clock period is $2T$ compared to T in a conventional LDI integrator SC circuit. This means that the operation speed for the whole circuit, determined by sampling frequency, can be doubled without requiring an increase in opamp speed.

By selecting suitable capacitance values Φ and Ψ can be easily implemented. When TWINTORS are connected together to form

a ladder structure, some simplifications are possible by separating signals into two channels, Fig. 2(c). The first equivalence in Fig. 2(c) is obvious. For the second equivalence, notice that a sampling signal of an even (odd) channel opamp output in a odd (even) period is actually the signal held from the previous period, therefore a delay factor, z^{-1} , is realized. A number of switches are saved by this two channel technique.

An overall sixth-order bichannel bandstop SC ladder is shown in Fig. 3 with the low-pass RLC ladder of Fig. (1a) as reference

TABLE I
DESIGN DATA FOR THE SIXTH-ORDER SC BANDSTOP FILTER

Specifications for the Bandstop SC Filter			
lower passband edge	4.5 kHz	upper passband edge	5.5 kHz
lower stopband edge	3.5 kHz	upper stopband edge	6.5 kHz
passband ripple	< 0.1 dB	stopband attenuation	> 26 dB
sampling frequency	100 kHz		

Normalized Data for the Lowpass SC Ladder Reference Filter				
$G1 = GL = 1$	C1 0.91646	L2 0.96995	C2 0.17046	C3 0.91646

Component Values for the Bandstop SC Filter				
C1 14.79097	C2 1.414525	C3 1.398662	C4 1.614900	C5 1.633215
C6 15.64070	C7 37.44417	C8 37.86882	C9 1.000000	C10 1.141830
C11 1.154780	C12 10.93656	C13 37.86304	C14 38.29245	C15 10.57509
C16 1.011341	C17 1.000000	C18 1.977572	C19 2.000000	C20 1.000000
number of capacitors	40	number of switches	30	
number of op amps	6	total capacitance	439.51	
capacitance spread	38.29			

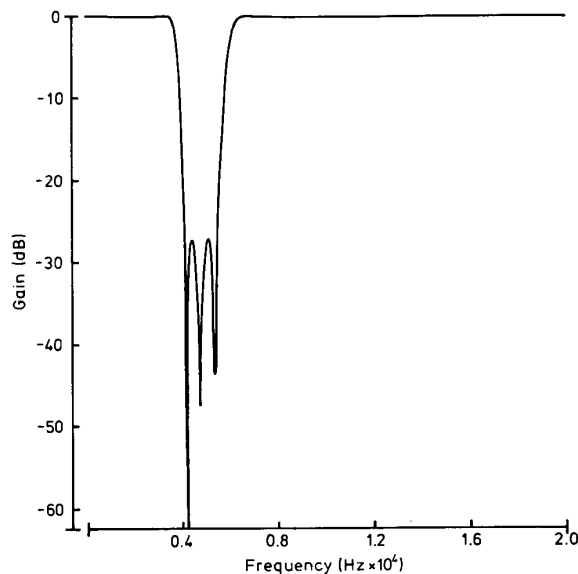


Fig. 4. Computed response of the SC bandstop filter.

prototype. The specifications and the component values are listed in Table I. The simulated response of the SC bandstop ladder is shown in Fig. 4. A negative input is required to realize the constant term in (6a), which may be avoided by the technique of [6].

III. CONCLUSIONS

A new strays-free SC circuit scheme has been proposed for bandstop SC ladder design. A major feature of the new circuit is that the clock period required is $2T$ so that the circuit can operate at a higher speed without extra demands on opamp performance.

ACKNOWLEDGMENT

The authors are grateful for the valuable help from R. K. Henderson.

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An Improved Search Algorithm for the Design of Multiplierless FIR Filters with Powers-of-Two Coefficients

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Abstract—An improved algorithm is presented for the discrete optimization of FIR digital filter coefficients which are represented by a canonic signed-digit (CSD) code, i.e., numbers representable as sums or differences of powers-of-two. The proposed search algorithm allocates an extra nonzero digit in the CSD code to the larger coefficients to compensate for the very nonuniform nature of the CSD coefficient distribution. This results in a small increase in the filter complexity however the improvement in the frequency response is substantial. The coefficient optimization is performed in two stages. The first stage searches for an optimum scale factor and the second stage consists of a local bivariate search in the neighborhood of the scaled and rounded coefficients.

I. INTRODUCTION

High-speed digital filtering applications (sample rates in excess of 10 MHz) generally require the use of custom application specific integrated circuits (ASIC's). Programmable signal processors cannot accommodate such high sample rates without an

Manuscript received November 2, 1988. This work was supported in part by the University of California MICRO Program and TRW, Inc. under Grant 87-066. This letter was recommended by Associate Editor T. R. Viswanathan.

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