Further Improve Circuit Partitioning using GBAW Logic Perturbation Techniques

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Motivation

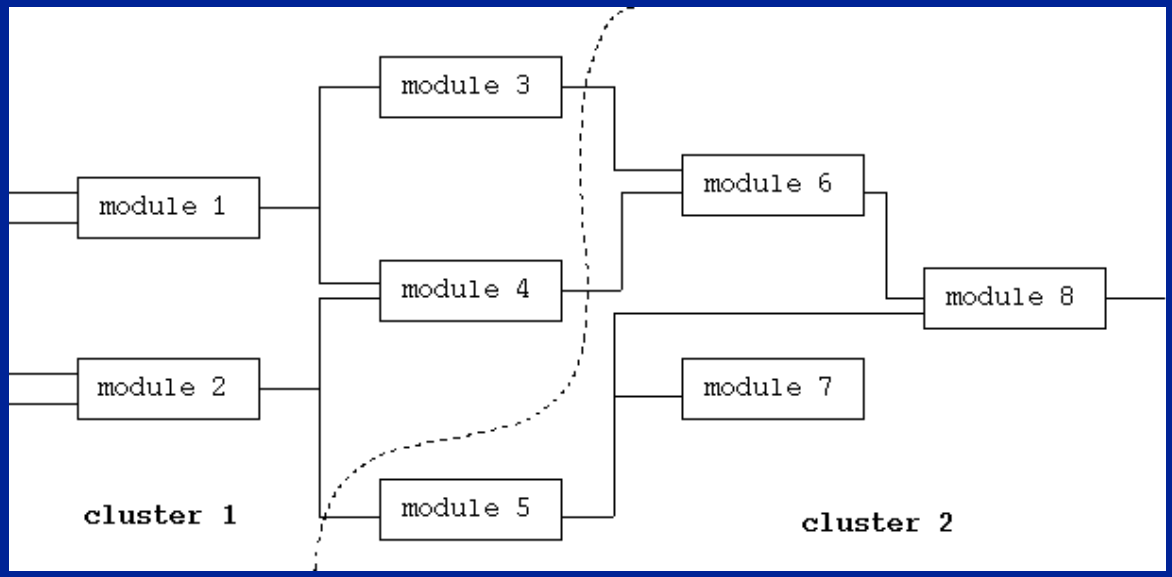
- Due to design complexity, I/O limitation and some other reasons, a chip is normally partitioned into sub-chips.
- Each sub-circuit consists of modules and nets.
- Our goal is to minimize the connecting wires between partitions with balance constraints.
- An improved partitioning result can be achieved if we consider the logic relationship between modules.

Outline

- Introduction
  - Circuit Partitioning
  - Alternative Wiring
- Application of Alternative Wiring
- GBAW – Graph-Based Alternative Wiring
- Circuit Partitioning using GBAW technique
- Experimental Results on Multi-way partitioning
- Conclusion & Future Work

Introduction - Circuit Partitioning

- **Objective: Given a circuit is divided into several clusters, such that the interconnecting wires between clusters is minimized with balance constraints.**
- **There are several applications:**
  - **Packaging, Synthesis, Optimization, …**



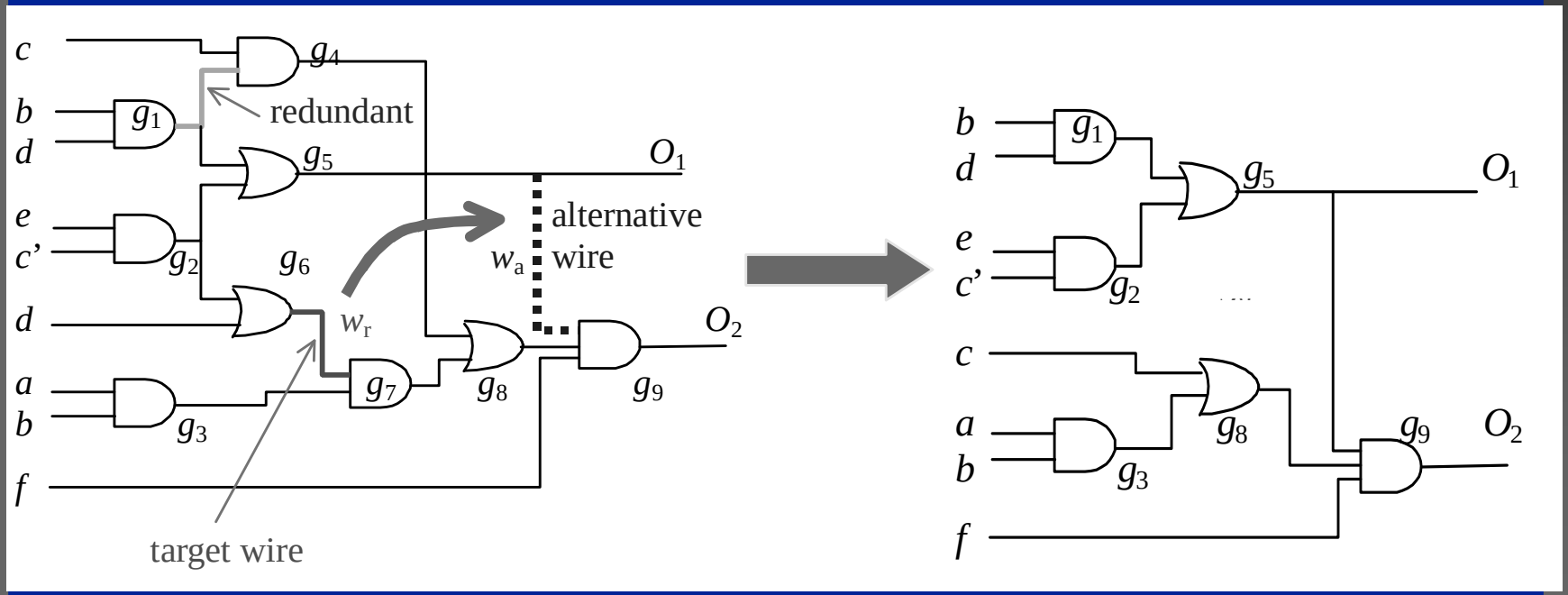
Introduction – Alternative Wiring

- **What is Alternative Wire?**
  - **Add a wire into a circuit**
  - **Another wire (target wire) becomes redundant**
  - **Remove target wire.**
  - **Without changing the circuit functionality.**

- **2 Powerful Alternative Wiring Tools**
  - **RAMBO – Automatic Test Pattern Generation (ATPG)-based**
  - **GBAW – Graph-based**

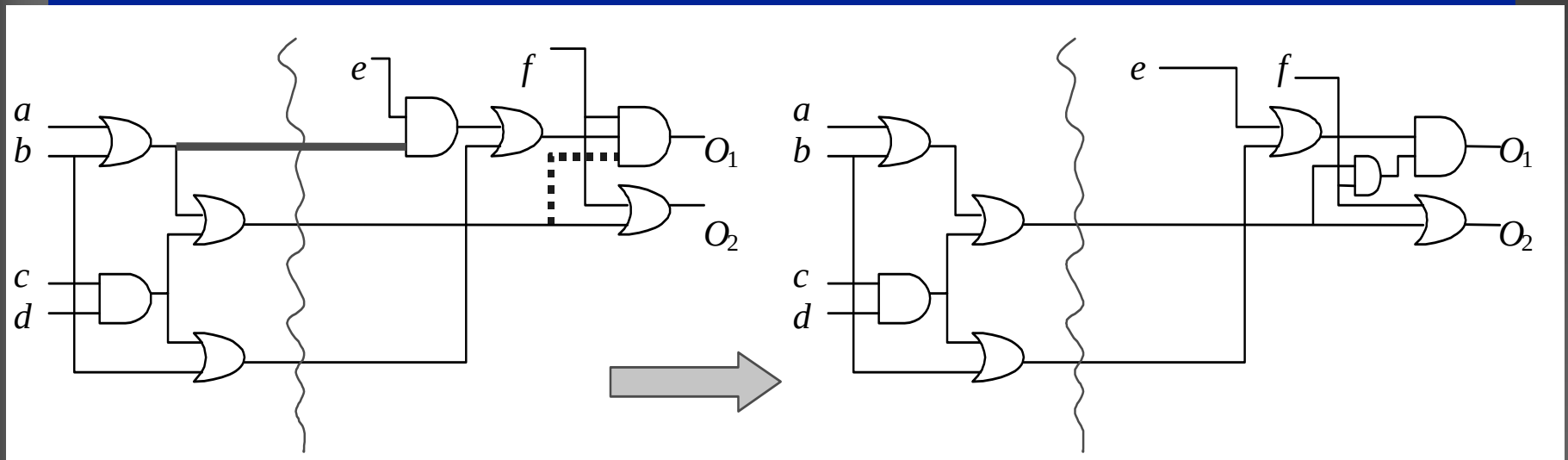
Alternative Wiring - Application 1

- **Useful in different areas**
  - **Logic Optimization**
    - **final circuit becomes smaller**



Alternative Wiring - Application 2

- **Circuit Partitioning**
  - **the interconnect wire between partitions is reduced from 3 to 2.**



(*a*) An alternative wire in an irredundant circuit

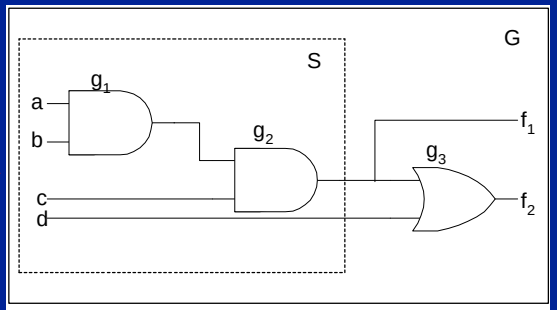
(*b*) No gain for logic synthesis, but gain for partitioning

GBAW

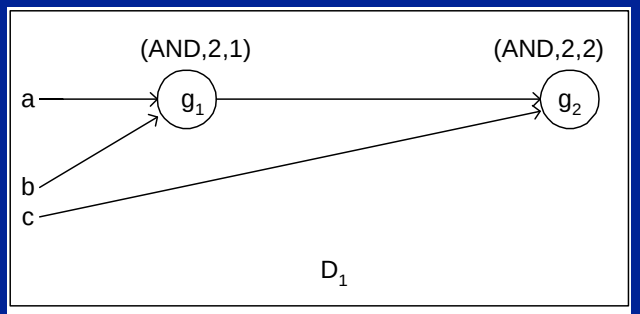
- A graph-based alternative wiring scheme
- Search alternative wire by *isomorphism* between local sub-networks and the pre-defined patterns.
- Can do both forward and backward search.
- Use *Configuration* to denote a Boolean network.
- No need of Boolean knowledge.
- Powerful in finding alternative wire and Very Fast!

GBAW – Configuration

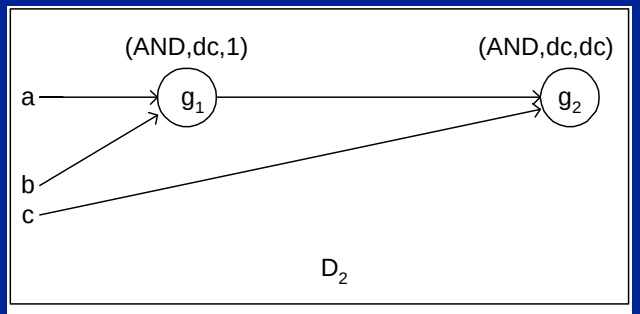
- A Boolean network G with its sub-network S. Below shows the mapping from network to *configuration*.
- Node y define as a triplet (*op*, $d^-(y)$, $d^+(y)$)
  - op is the Boolean operator (AND, OR, NAND, NOR)
  - $d^-(y)$ is the in-degree of y, $d^+(y)$ is the out-degree of y.
  - (AND, dc, dc) → both fanins or fanouts are also *don't care*.



(a) Boolean network G



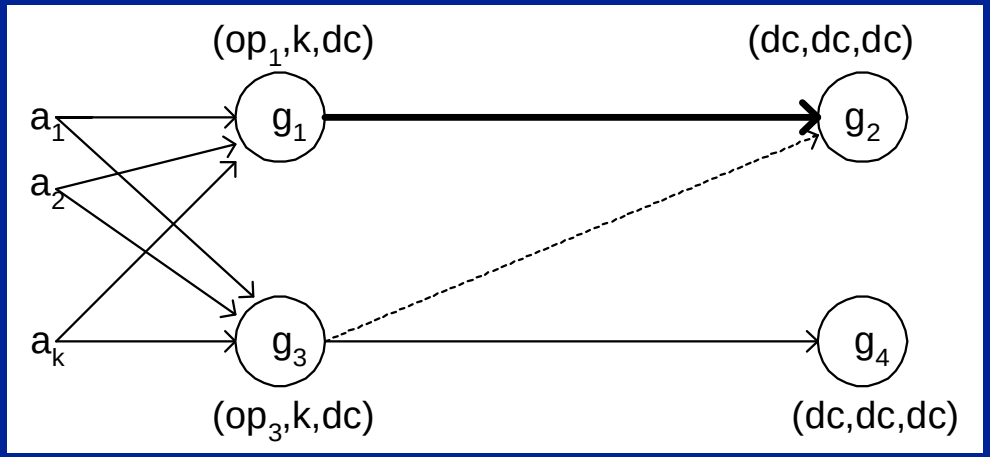
(b) A configuration of S



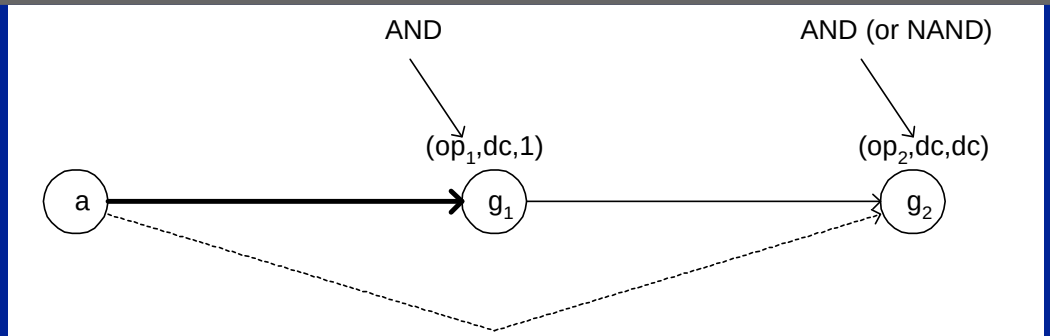
(c) Another configuration of S

0-local pattern

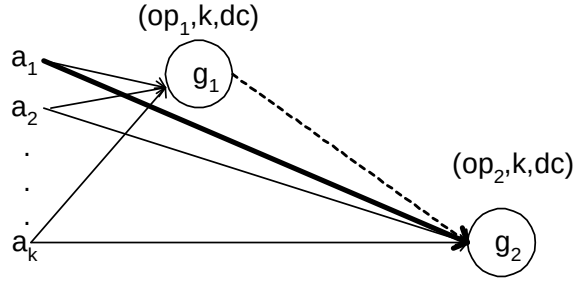
- Bold line → target wire
- Dotted line → alternative wire
- 0-local means the edge distance between target and alternative wire is 0.



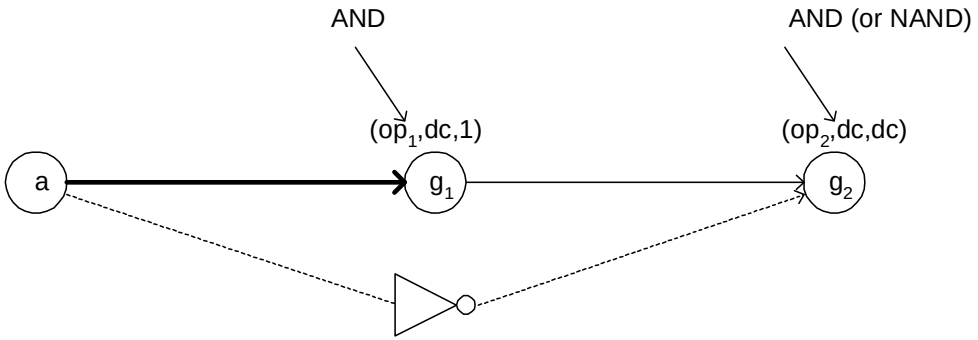
1-local patterns



(a) Case 1-1, op_1=AND, op_2 =AND (or NAND); or op_1=OR, op_2=OR(or NOR)

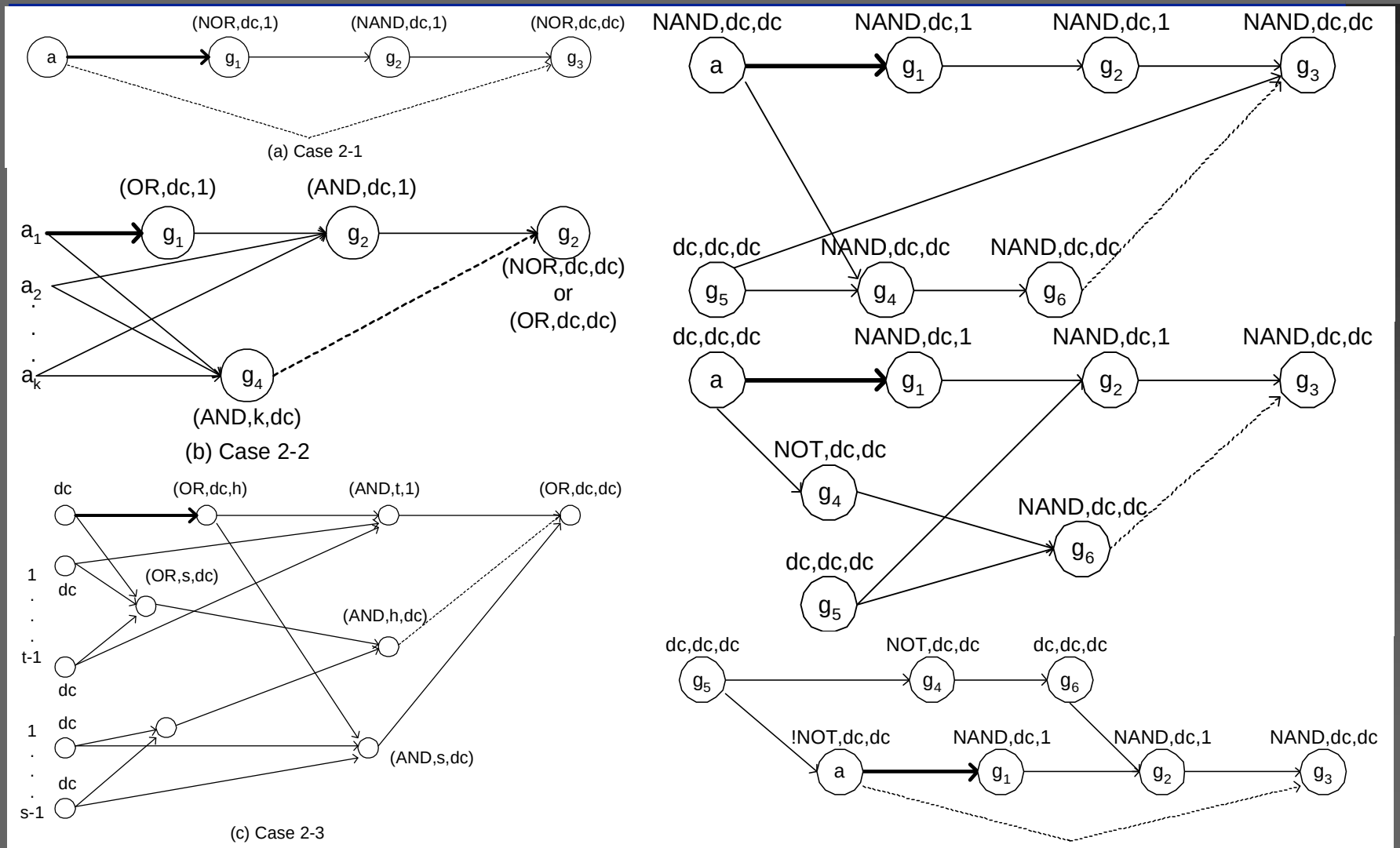


(b) Case 1-2, op_1=AND, op_2 =AND (or NAND); or op_1=OR, op_2=OR(or NOR)



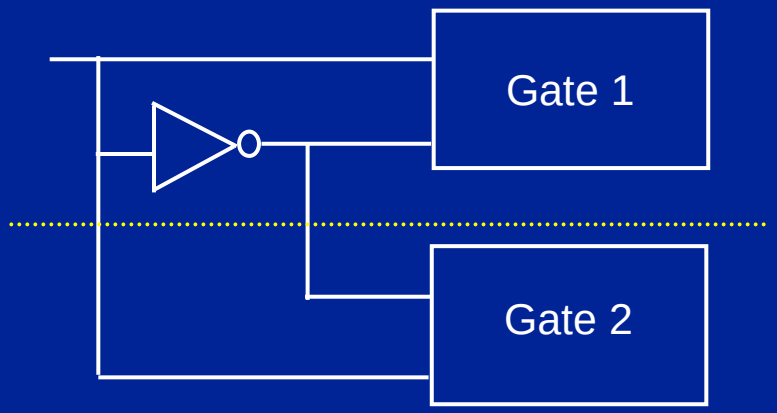
(c) Case 1-3, op_1=NOR, op_2 =NAND (or AND); or op_1=NAND, op_2=OR(or NOR)

2-local patterns

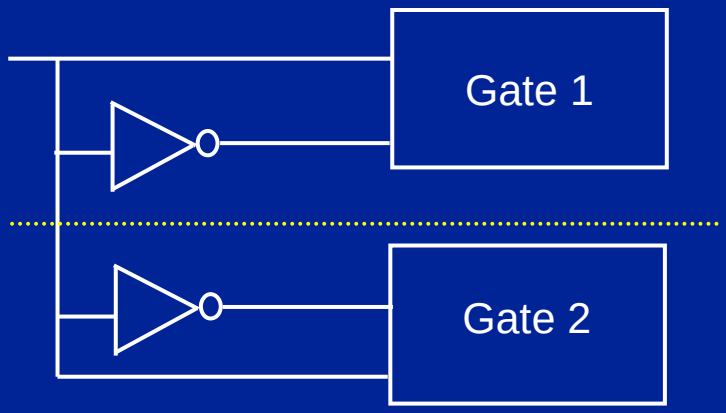


Circuit Partitioning – GBAW technique

- **Modeling the circuit as graph**
- **Methods for graph partitioning**
  - **No change to the graph – KL or FM algorithm**
  - **Modify the graph by replications (more areas)**
  - **Couples the graph domain (nodes and edges) and the logic domain (function performs by each node)**



Cut wire = 2

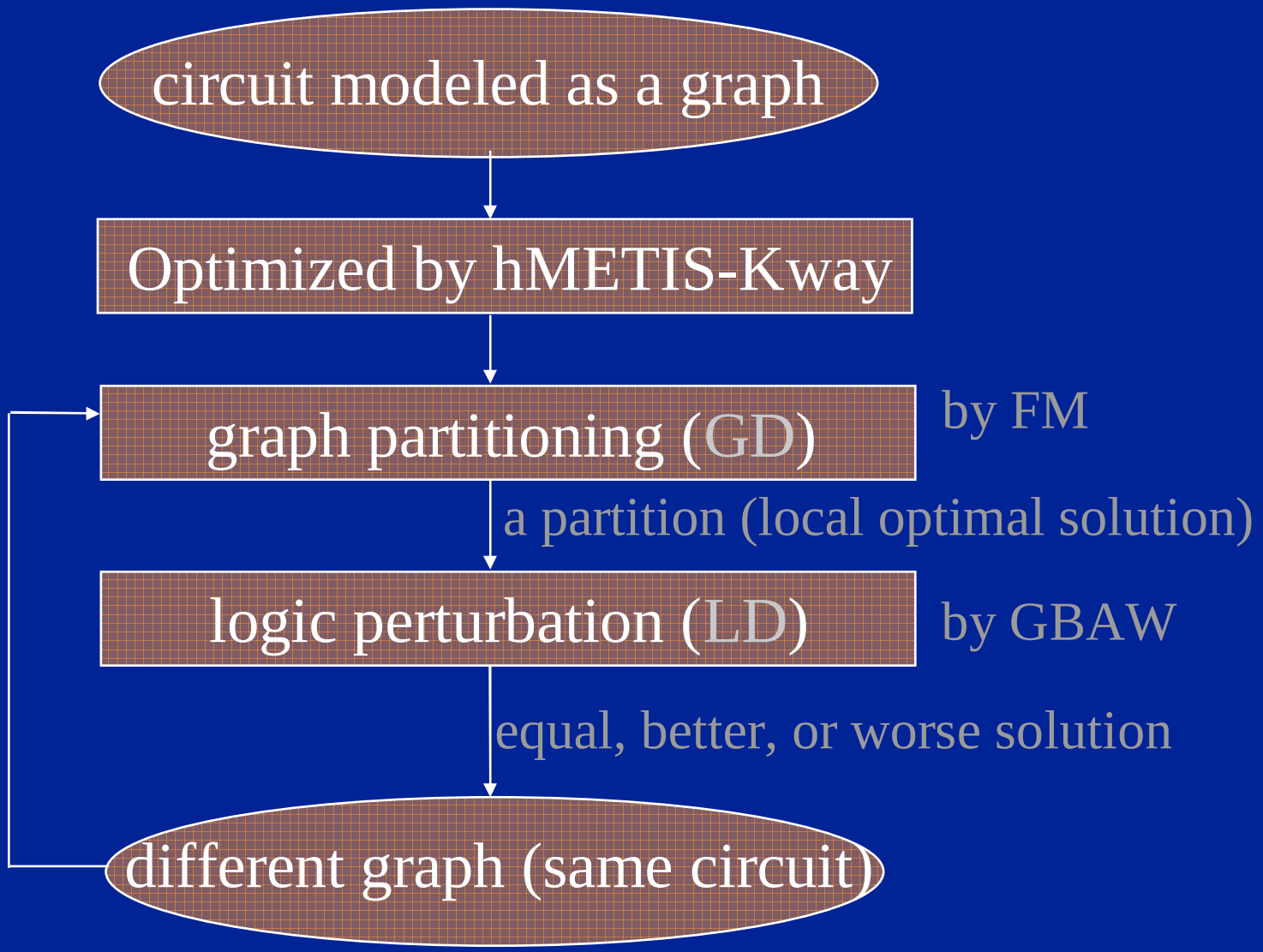


Cut wire = 1

Circuit Partitioning – GBAW technique

- **Our approach**
  - **Obtain excellent partitioning result from state-of-the-art HMETIS-Kway.**
  - **Graph domain – choose *ANY* graph partitioning**
    - **Choose FM for its simplicity and efficiency.**
    - **Proposed by *Fiduccia and Mattheyses in 1982.***
  - **Logic domain only applies GBAW technique**
    - **Apply GBAW (GP) to search for another better partitioning result → fast and reduce the cut cost**
- **Key: *Even optimum graph partitioning results can still be improved***
- **Experiments were conducted on 2 to 5 way partitioning on MCNC benchmark circuits.**

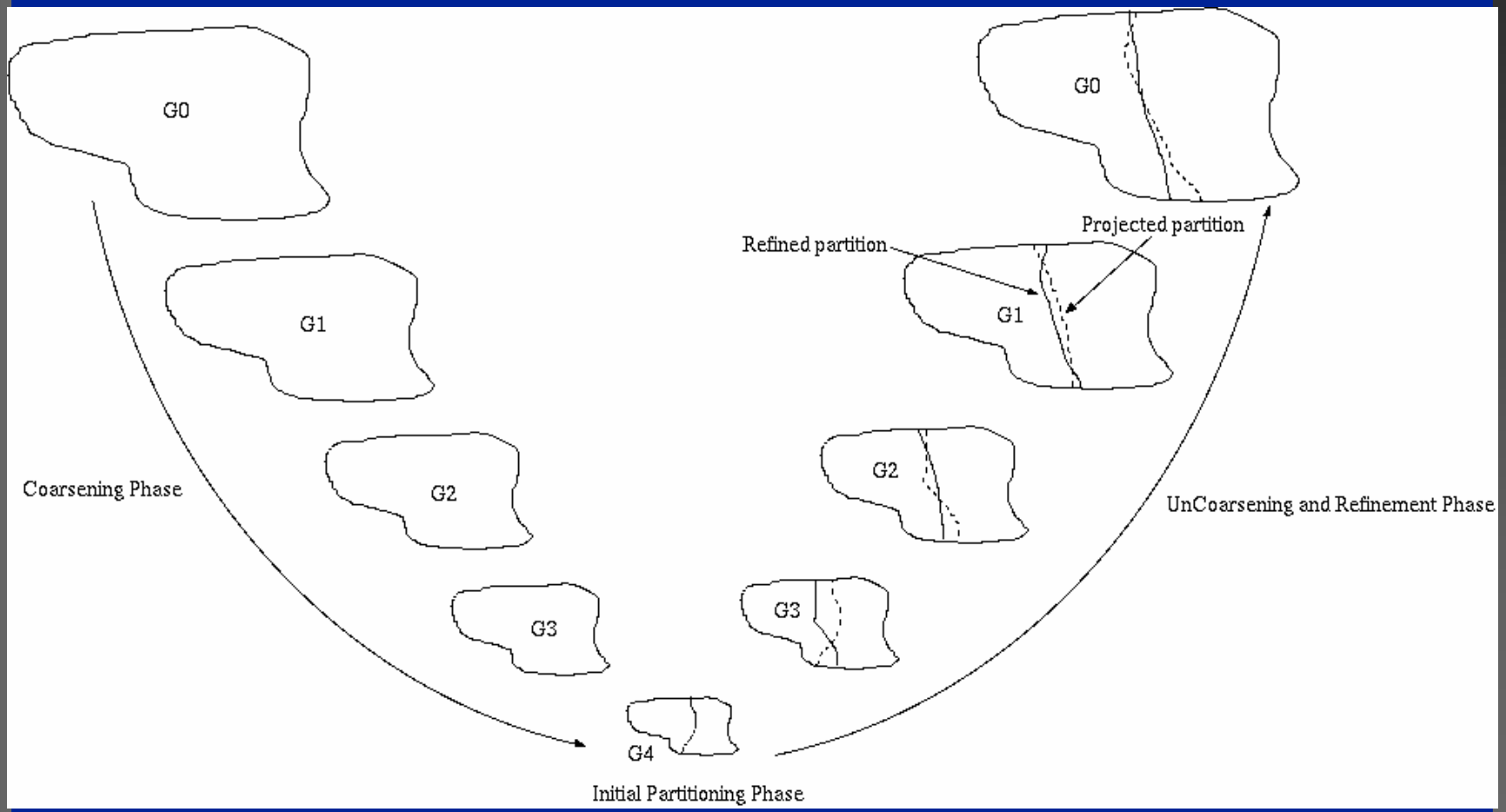
Overview Flow



HMETIS-Kway – state-of-the-art

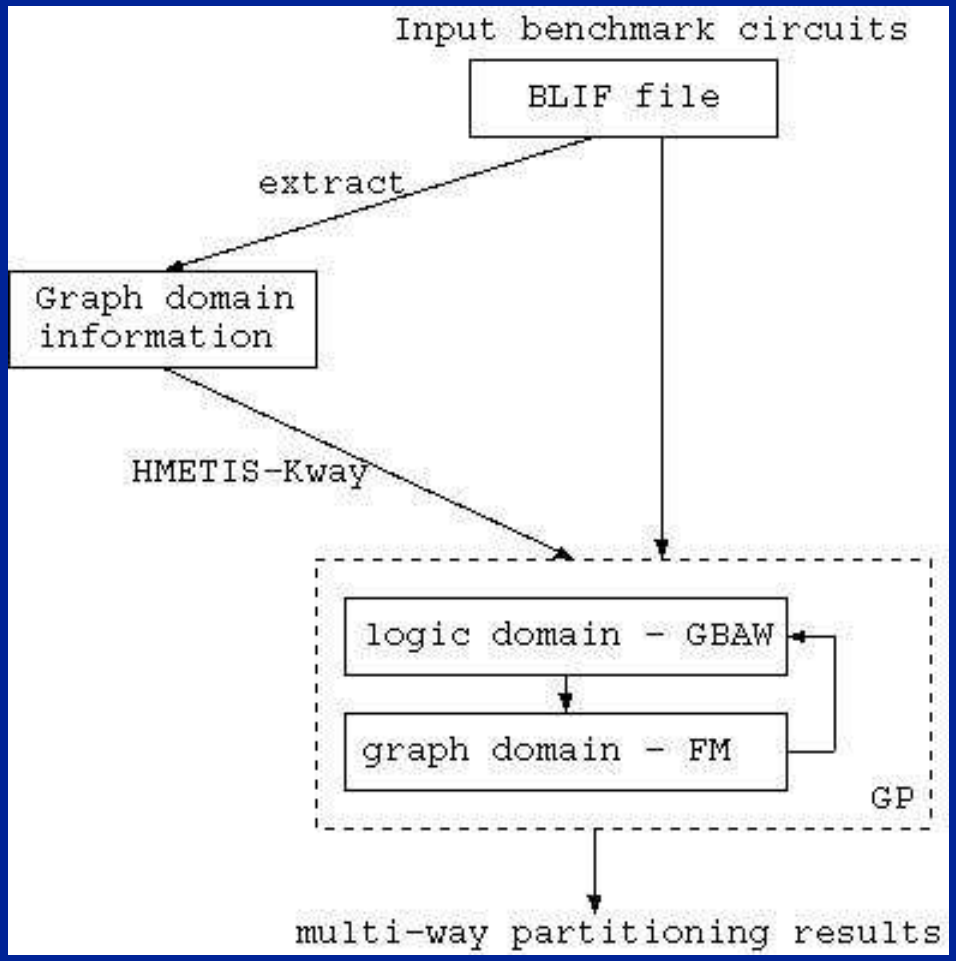
- Increasing complexity of Physical Design, use multi-level approach to break down the problem size
- Phase 1 – Coarsening
  - Merge vertices to form a new vertex
  - Size of new graph / hypergraph reduce fast
- Phase 2 – Initial Partitioning
  - Apply k-way partitioning algorithm on a small problem
- Phase 3 – Uncoarsening and Refinement Phase
  - Project back to the original graph
  - More degree of freedom in finer graph, refinement scheme is necessary to improve final solution

Multi-level Partitioning – 3 phases



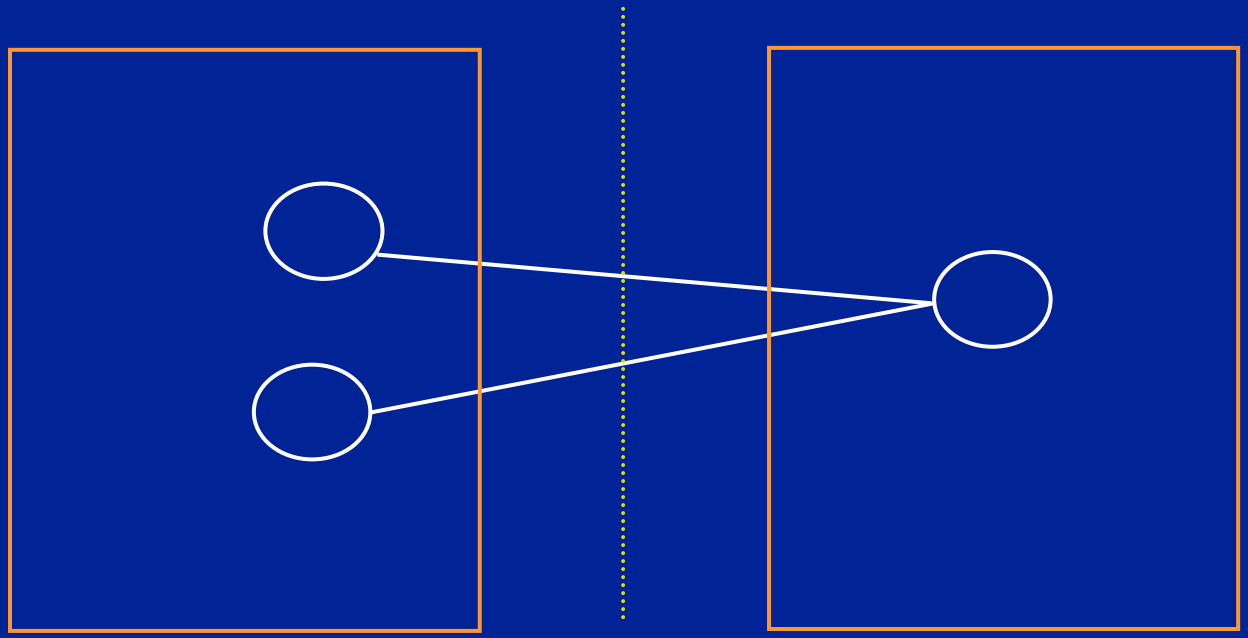
Pre-process the benchmarks

- **There are totally 26 benchmarks.**



Cut wire and Cut cost

- **Cut wire is the wire connecting between different partitions.**
- **Cut cost is the number of partition the hyper-edge connecting with.**



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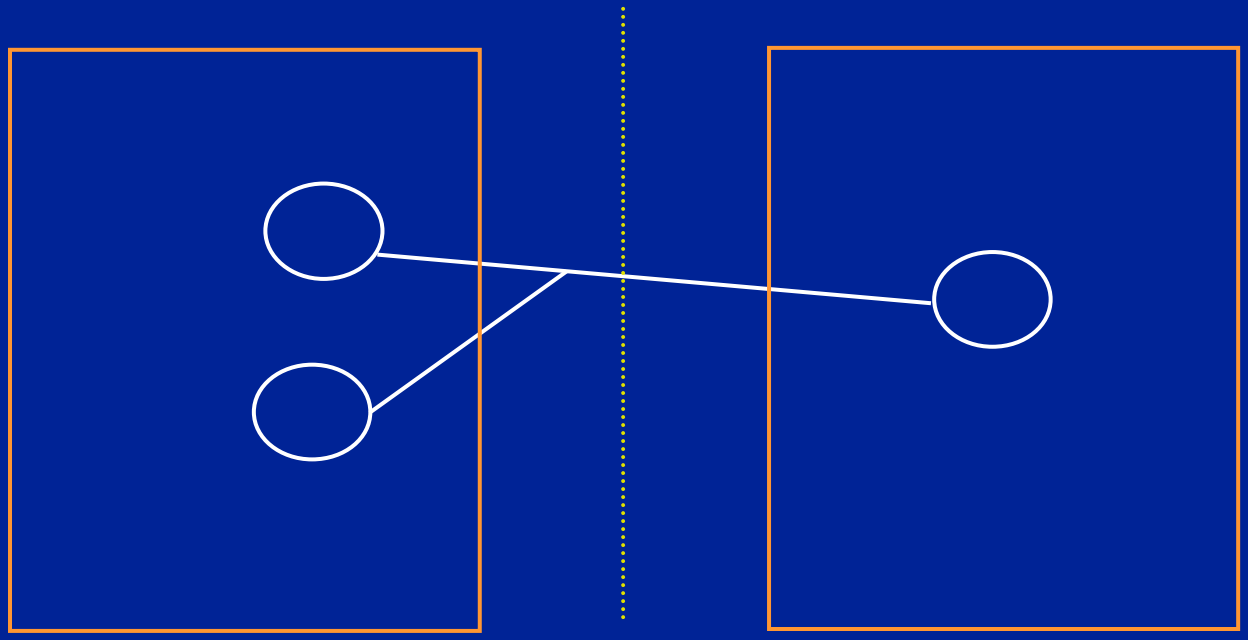
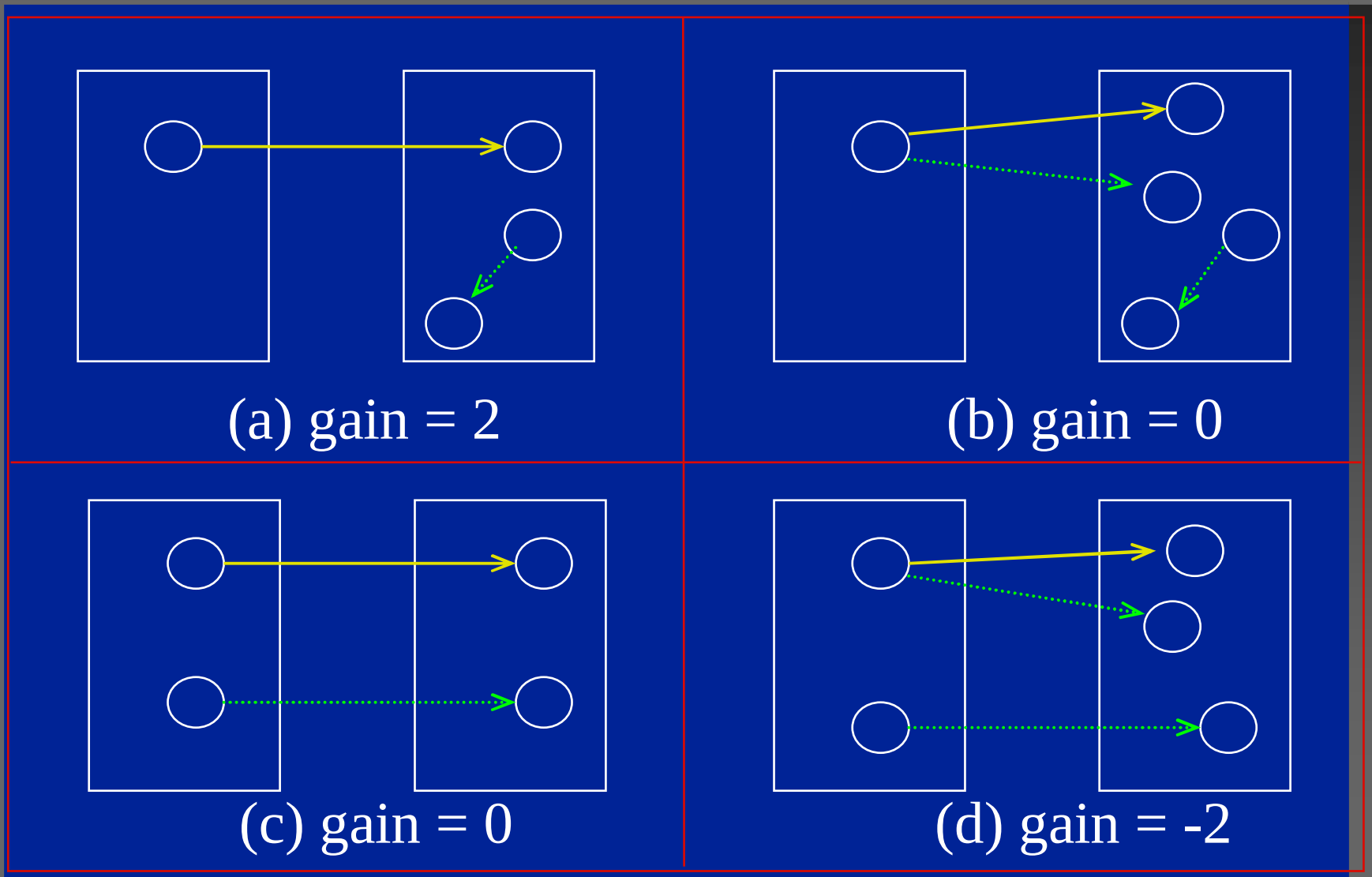


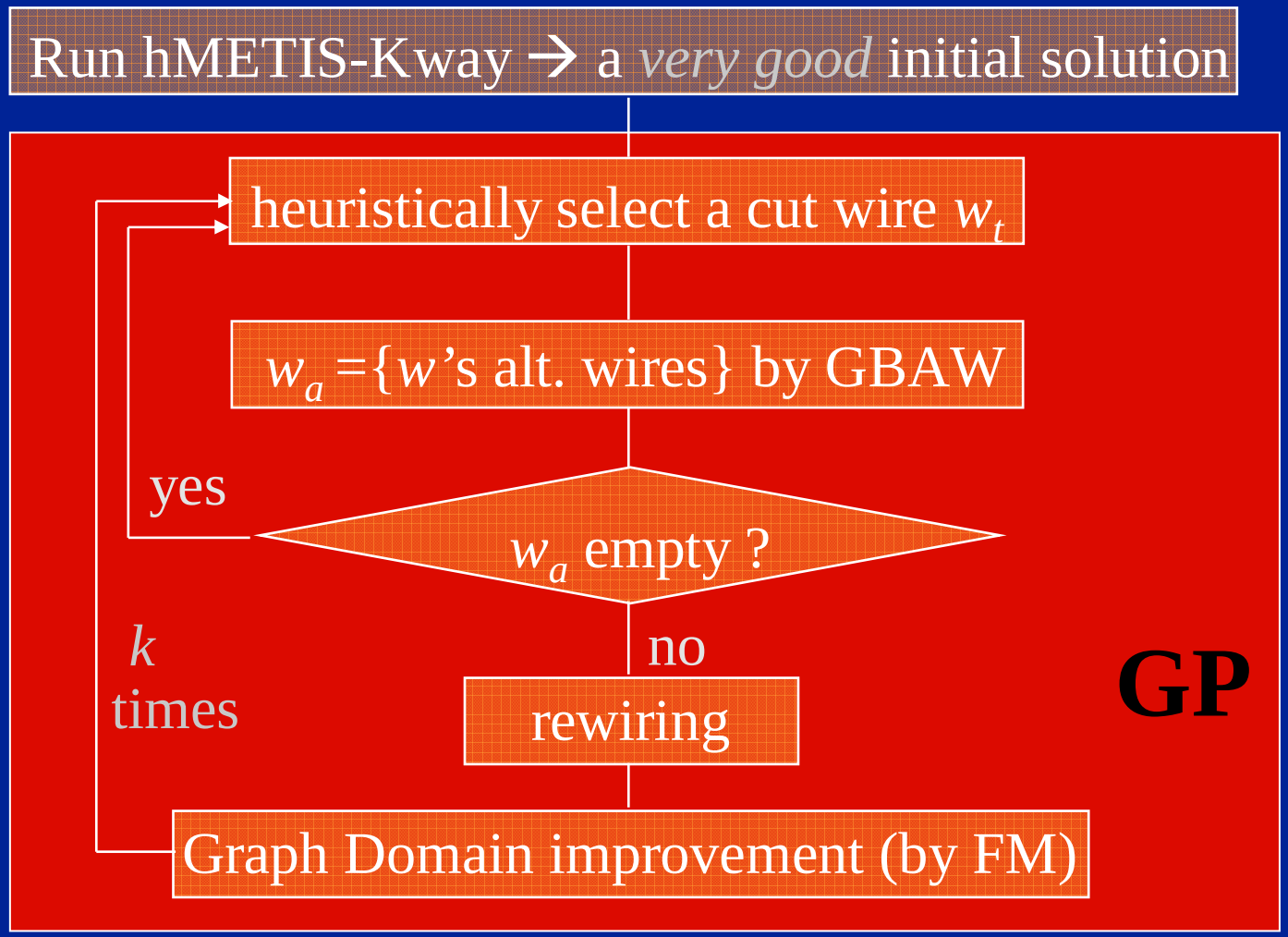
Cut wire = 2

Cut cost = 2

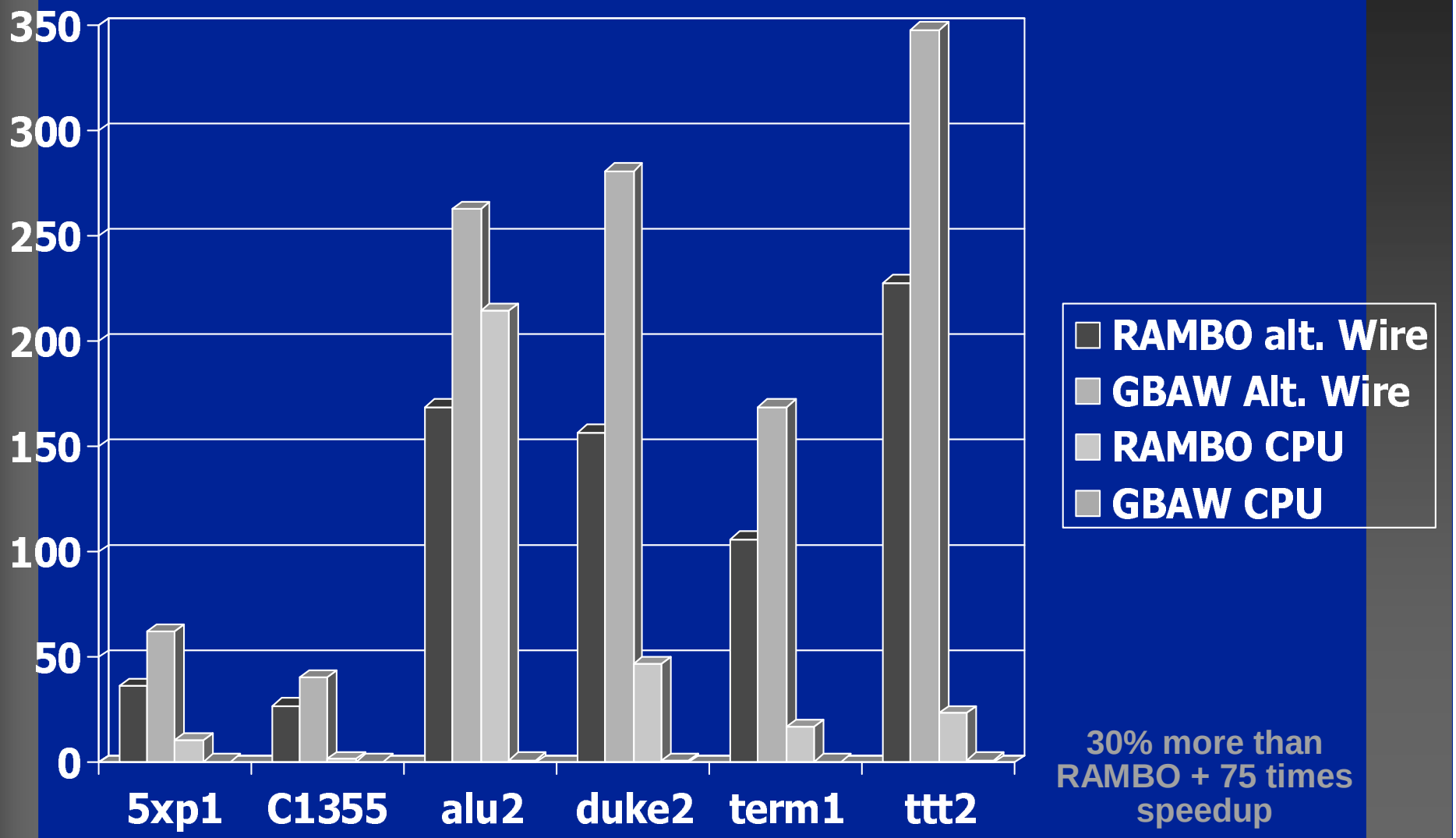
Pin gain after rewiring



GP algorithm



Alternative wiring statistics of RAMBO and GBAW



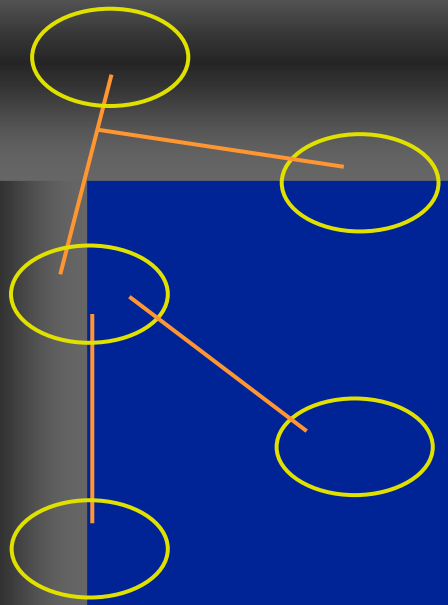
30% more than RAMBO + 75 times speedup

Experimental Results

Circuit	HMETIS-Kway			GP		
	Area	#lits	Cut cost	Area	#lits	Cut cost
5xp1	61:71	235	30	73:63	239	28
C2670	516:527	1444	42	517:531	1449	34
C432	119:119	392	44	118:130	402	36
…	…	…	…		…	…
C7552	1281:1141	4105	18	1286:1142	4111	18
alu4	428:357	1470	140	438:360	1481	120
des	1727:2112	6655	236	1565:2282	6663	146
rot	441:383	1251	54	442:384	1253	46
Total		45506	1850		45656	1576
Average					+0.33%	-14.48%

Comparison of 2-way partitioning by using hMETIS-Kway & GP

Experimental Results by GP



	hMETIS-Kway		GP	
	#lits	Cut cost	#lits	Cut cost
2-way	45506	1850	45656 (+0.33%)	1576 (-14.48%)
3-way	45506	3339	45748 (+0.53%)	2999 (-10.18%)
4-way	45506	4250	45784 (+0.61%)	3864 (-9.08%)
5-way	45506	5185	45828 (+0.71%)	4706 (-9.24%)

Partitioning comparison between hMETIS-Kway & GP

Conclusion & Future Work

- Presented a framework which integrates GBAW to multi-way circuit partitioning.
- We can apply any graph domain partitioner to GP and experimental results showed GP is able to reduce the cutcost over excellent results.
- Future Work
  - Apply GBAW on the timing optimization of FPGA routing and other physical design problems.

The End

- **Please feel free to ask any question !**

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