yield all the information such as the thickness of the gate oxide, buried-oxide as well as the SOI film, along with the doping density in the film and the substrate.

**Reinforcing effect of coverlayers on the fatigue life of copper-kapton flex cables.** Alan T. Zehnder and Anthony R. Ingraffea. *IEEE Transactions on Components, Packaging and Manufacturing Technology—Part B*, 1995, 18(4), 704. Flex cables constructed of copper sandwiched between Kapton (polyimide) fail under repeated bending due to the formation and propagation of fatigue cracks in the copper. It is observed that fatigue life of rolled-annealed copper cables with a coverlayer of Kapton is significantly higher than cables without a coverlayer. This result is explained using a fracture mechanics analysis where the Kapton layers bridge across cracks in the copper, shielding the crack from the full stresses. This retards crack growth, hence increasing fatigue life of the cables.

**Application of direct strain measurement to fatigue studies in surface solder joints.** Yan C. Chan, D. J. Xie, J. K. L. Lai, and I. K. Hui. *IEEE Transactions on Components, Packaging and Manufacturing Technology—Part B*, 1995, 18(4), 715. A direct method to measure the fatigue life of surface mount solder joints is proposed. This approach makes use of a quad flat pack (QFP) solder-printed circuit board (PCB) assembly as a shear specimen. After the assembly and thermal stress screening tests, the specimen is cut in half at the PCB. The displacement or strain variations between the split PCB's during mechanical strain cycling reflect the fatigue properties of the solder joints. This approach is useful to predict the fatigue life of a practical surface solder joint in electronic products and applicable to any leaded and leadless surface joints. The measurement of joint strain and chip stiffness can reveal fatigue status in the solder joint system, which is important to the understanding of its fatigue mechanism.

**Prediction of equilibrium shapes and pedestal heights of solder joints for leadless chip components.** Vivek Jairazbhoy. *IEEE Transactions on Components, Packaging, and Manufacturing Technology—Part A*, 1996, 19(2), 224. The reliability of solder joints for surface mount components is closely related to the joint shape and “pedestal” (stand-off) height, i.e. the thickness of the fillet that separates the metallized surface of the component from the pad on the circuit board. In this paper, an analysis is presented to predict the profiles and pedestal heights of equilibrium solder joints that attach surface mount components to printed circuit boards. The common case of two-dimensional (2-D) joints with negligible solder density effects is considered. A criterion is also derived that represents the minimum critical volume of solder required to produce a “theoretically nonzero pedestal height,” below which the model is inapplicable. The critical solder volume produces a convex joint. The criterion suggests that if a 2-D joint is concave and within the model simplifications, force equilibrium cannot exist on a component at a positive pedestal height. Extensions to cases in which solder density effects are significant are also discussed. The analysis results in a system of coupled nonlinear algebraic equations which are solved numerically. The sensitivity of joint shape and pedestal height to geometric and physical parameters is examined. Comparisons between the theory and experiment show good agreement.

**Dielectric breakdown I: a review of oxide breakdown.** J. F. Verweij and J. H. Klooijwijk. *Microelectronics Journal*, 1996, 611. This paper gives an overview of the dielectric breakdown in thin oxide layers on silicon. First test methods are discussed, followed by their application to the estimation of the oxide lifetime. The main part of the paper is devoted to the physical background of the intrinsic breakdown. Finally, defect-related or extrinsic breakdown is discussed.

**Sheet resistance and layout effects in accelerated tests for dielectric reliability evaluation.** F. Plo. *Microelectronics Journal*, 1996, 27, 675. Different extrapolation algorithms can be used to calculate gate oxide lifetime from accelerated reliability tests. The measurement is often carried out on large area capacitors in order to be statistically meaningful with respect to the active oxide area of the devices. This also allows a reduction of test time and therefore of cost. However, both the capacitor layout and the sheet resistance either of gate or of substrate or of interconnections can have a huge impact on the correctness of the experimental data. In this work it will be shown that lifetime forecast can be largely over-estimated due to series resistance. Moreover, a non-optimized layout of the capacitor can induce a non-uniform stress on the oxide due to sheet resistance effects. The validity of the accelerated test is also questionable in this case. Some guidelines to avoid errors in the collection of raw data will also be given.

**Fatigue life studies on defect-free solder joints fabricated from modified reflow soldering.** D. J. Xie, Yan C. Chan, J. K. L. Lai, and I. K. Hui. *IEEE Transactions on Components, Packaging and Manufacturing Technology—Part B*, 1996, 19(3), 679. This paper describes the improved characteristics of defect-free solder joints fabricated through modified reflow soldering. The modified method only requires that the solder joints are split for a very short time during a conventional solder reflow. The fatigue properties and microstructure of the solder joints are critically studied. It is found that the method of splitting is effective in eliminating pore formation (both gas and shrinkage pores) and inclusions in solder joints. The method is applicable to various solder pastes, whether it be no-clean or water-soluble. Thermal and mechanical fatigue cycling tests show...