CITY UNIVERSITY OF HONG KONG
Department of Electronic Engineering
OBTL Course Description Form

Course Title: Digital System Design with VHDL

Course Code: EE4204

Units: 3

Level: B4

Course Aims & Objectives:
This course presents the student with a top down methodology for VLSI design using VHDL. The objective is to develop students' knowledge and expertise in the specialization of VLSI design with VHDL; present the techniques required for the design of complex integrated systems from an initial specification down to final implementation with FPGA for rapid prototyping via top-down design methodology. The course is emphasized on hands-on experience of using state-of-the-art EDA tool to the complete design of a VLSI system implemented with FPGA. Students will be equipped with the knowledge necessary to design basic VLSI circuits for rapid prototyping using VHDL.

Intended Learning Outcomes:
On completion of this course, the students will be able to
1. Apply the fundamental knowledge of VHDL to model a digital circuit
2. Make use of VLSI technology for digital ASIC implementation.
3. Use EDA tool with VHDL to complete design of a digital system
4. Design digital system in top-down approach and implement the design with FPGA

Syllabus:
Introduction
Programmable Logic Primer; What is VHDL; Top-down Design methodology; Describe and Synthesis approach

VHDL Basics
Design Units; Entity; Architecture; Configuration; Package and Library

VHDL Modelling
Data Objects; Data Types; Signal and Variables; Operators; Expression; Process Concurrency; Concurrent and Sequential Statements; Advanced Data Type

Structural VHDL Modelling
Component Declaration; Component Specification; Port Map Command; Generic Map Command; Configuration; Direct Instantiation

Hardware Modelling
General Guidelines of VHDL Synthesis; Combinational Logic; Synchronous Logic; ROM, RAM, Storage Elements, Flip-flops, Latches, Tristate Buffers; Synchronous Sets and Resets System; Asynchronous Sets and Resets System; Register Inference; Multiplexer, Buses, Decoders, Encoders, Counters, Comparators, Adders, Multipliers, Shift Registers, FIFO Registers, Stack Registers; Resource Sharing; Clock Generators; Two Phase Clocking.
Finite State Machine
Moore Machine; Mealy Machine; Asynchronous State Machine; State Machine with Clocked Outputs; State Coding; FSM Initialization; FSM Synthesis

RTL Synthesis
Optimization and Mapping; Design Constraints; Best Case Optimization

Simulation and Verification
Functional Verification; Timing Analysis

Test Bench
Level of Test bench; Waveform Generators

Laboratory Experiment:
Lab 1. Top-down Design Environment with VHDL, Design Entry, Simulation
Lab 2. Design Entity, Architecture and Behavioural Modelling
Lab 3. Structural Modelling
Lab 4. Data Path Design and Control Path Design
Lab 5. Design a digital system with VHDL, test and verify the design, logic synthesis and post synthesis verification

Teaching pattern:
  Duration of course: 1 semester
  Suggested lecture/tutorial/laboratory mix: Lecture Hour: 26 hours
  Tutorial Hour: 6 hours
  Laboratory Hour: 15 hours

Assessment pattern:
  Examination duration: 2 hours, at the end of the semester
  Percentage of coursework, examination, etc.: 40 % CW; 60 % Exam

Course works are in the forms of assignment, test and project.

For a student to pass the course, at least 30% of the maximum mark for the examination must be obtained, and a laboratory attendance of at least 75% recorded.

Pre-requisites: (please quote course code & title)
EE2000 Logic Circuit Design

Pre-cursor: (please quote course code & title)
Nil

Exclusive Course: (please quote course code & title)
Nil

Equivalent Courses: (please quote course code & title)
Nil

Equivalent to the Old Course Code and Title: (please quote course code & title)
IT4204 Digital System Design with VHDL

Textbook:
Reference Book:

Kevin Skahill: VHDL for Programmable Logic, (Addison-Wesley and Longman)

Stefan Sjoholm and Lennart Lindh: VHDL for Designers, (Prentice Hall)