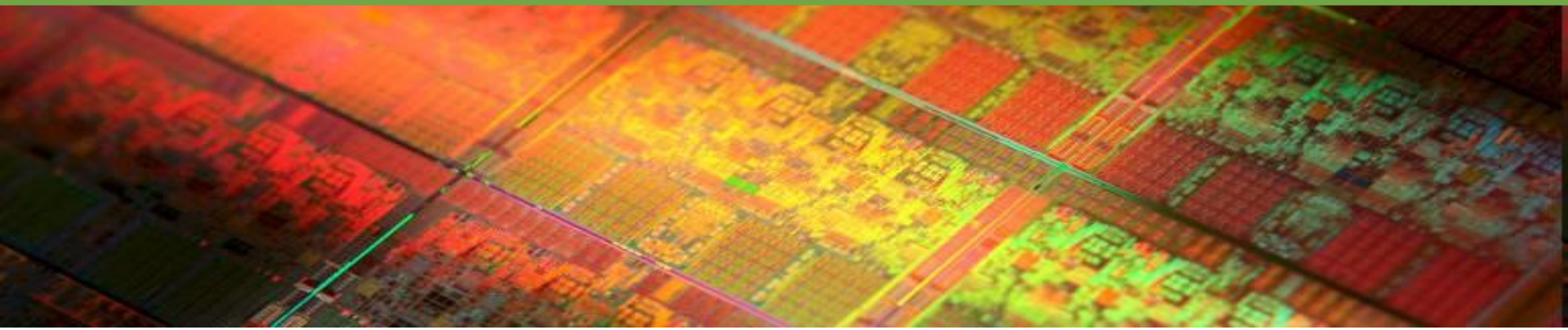
CityU-Learning Summer Talk 2020



講座題目： 一切從「芯」開始・智能
手機是如何運算的

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CityU
香港城市大學
City University of Hong Kong
專業 創新 胸懷全球
Professional·Creative
For The World

什麼是計算？ Computing?

DETECT LANGUAGE | CHINESE | ENGLISH ⇄ ENGLISH | CHINESE (TRADITIONAL) | CHINESE

computer engineering

computer engineering
計算機工程

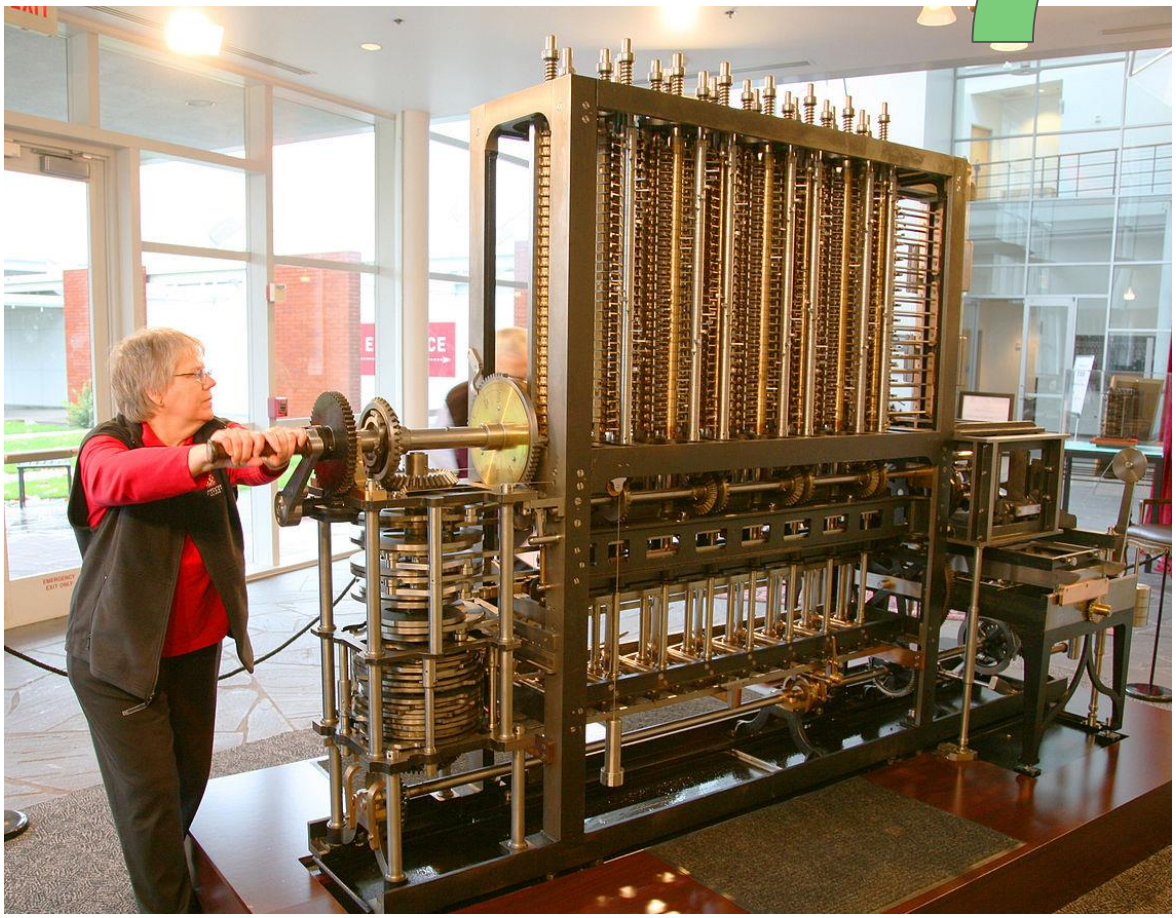
computer engineering student
計算機工程專業的學生

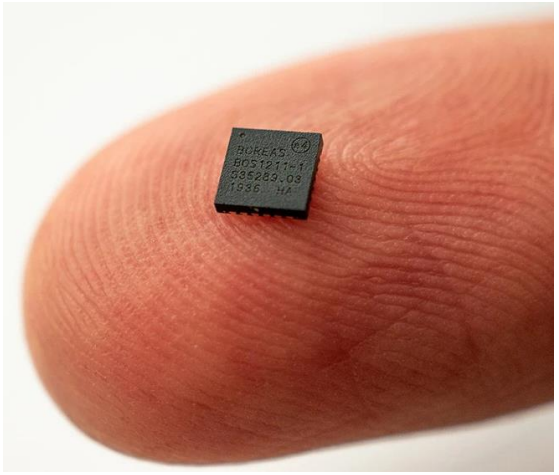
計算機工程

Jìsuànjī gōngchéng

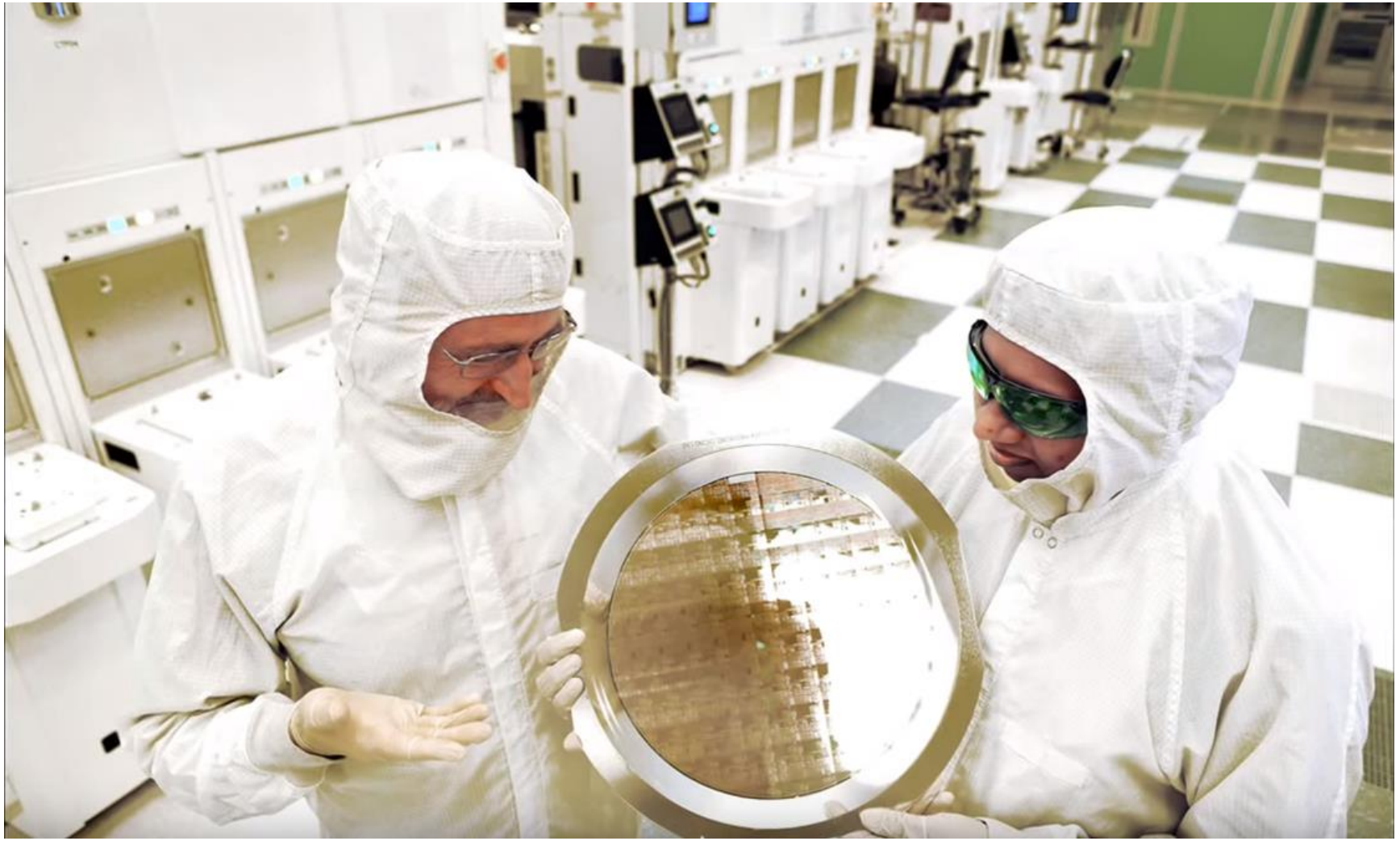
Send feedback

機械計算　到　電子計算





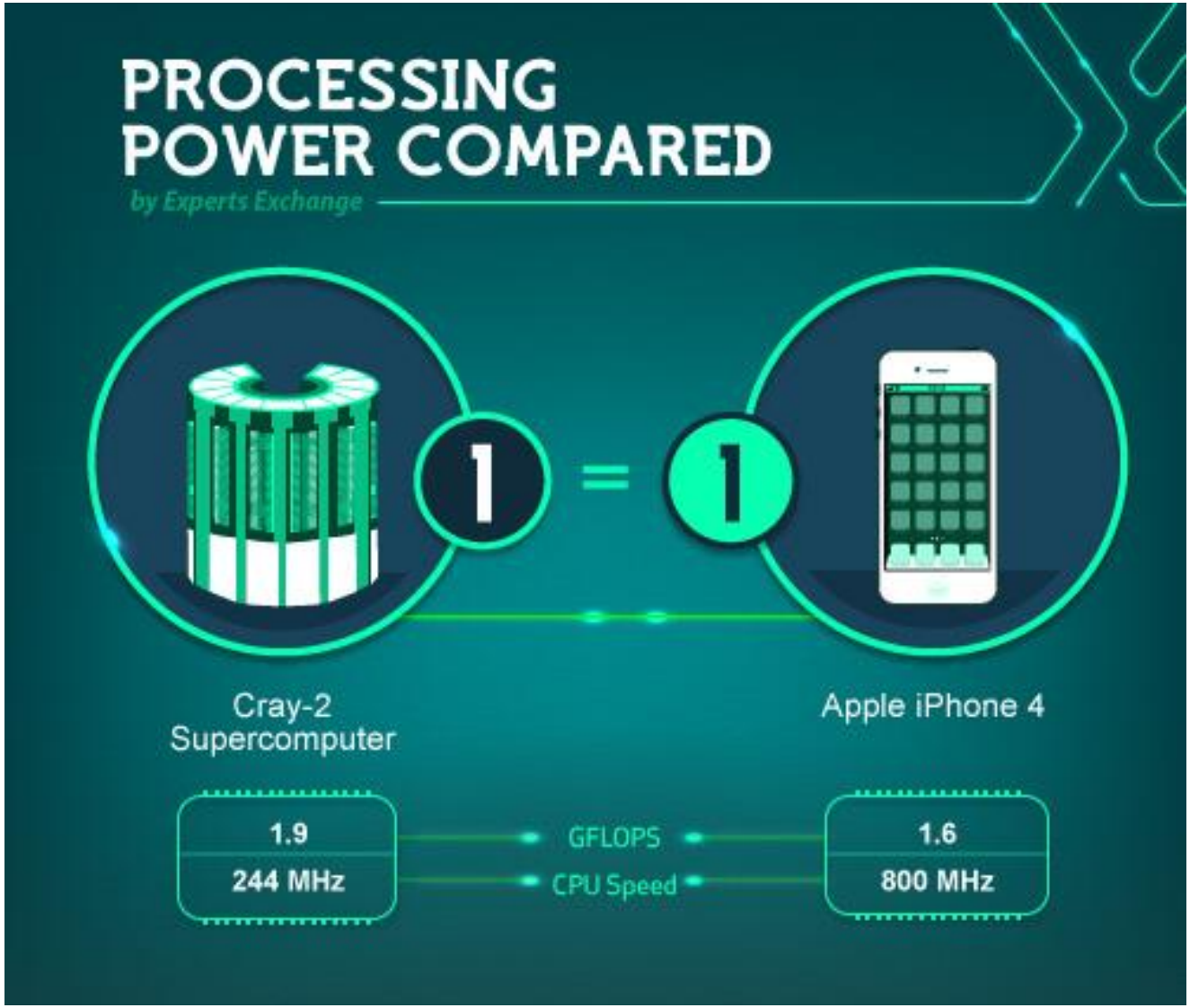
太空人?



拆解　智能手機

CRAY-2 Supercomputer (1985) $16M USD

你的手機是一台超級計算機



每秒浮點運算次數

- Integer:
  - 2 x 3 = 0010 x 0101
- Floating-point:
  - 1.23456 x 8.765432

- floating point operations per second (FLOPS, flops or flop/s) is a measure of computer performance.

Computer performance

Name	Unit	Value
kiloFLOPS	kFLOPS	10^3
megaFLOPS	MFLOPS	10^6
gigaFLOPS	GFLOPS	10^9
teraFLOPS	TFLOPS	10^{12}
petaFLOPS	PFLOPS	10^{15}
exaFLOPS	EFLOPS	10^{18}
zettaFLOPS	ZFLOPS	10^{21}
yottaFLOPS	YFLOPS	10^{24}

Floating point number浮點運算

- Floating point
  - A method represent a real number
  - Large dynamic range
  - $N = fraction \times 2^{exponent}$, stored as

  - For example:
    - $(5.25)_{10} = (101.01)_2 = +(1.0101)_2 \times 2^2$

2+127=129=1000_0001

5.25
=
5 + 0.25
=
101 + 0.01

Since the exponent can be negative, we should add 127 as bias for single precision

Floating point number浮點運算

- Another example:
  - $(0.333)_{10} \approx (0.010101)_2 = (1.0101)_2 \times 2^{-2} = 0.328125$

4-bit mantissa
Diff=0.004875

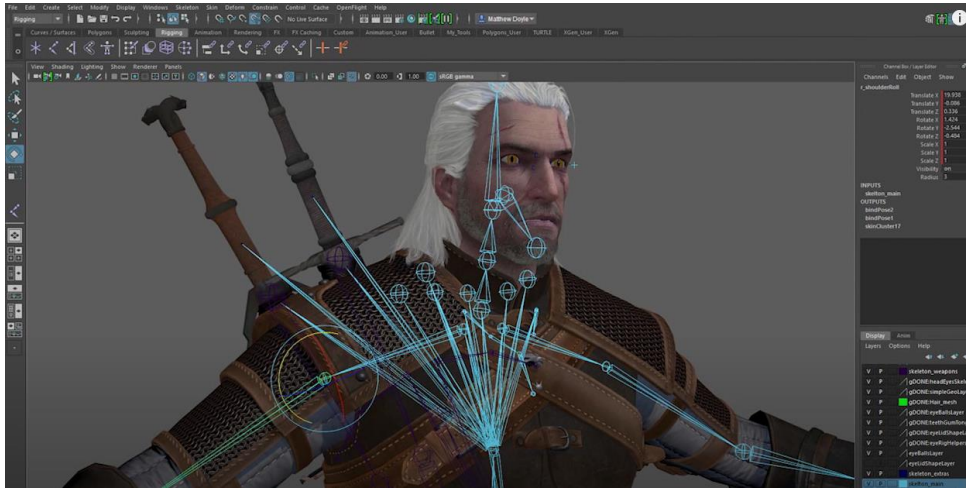
8-bit mantissa
Diff=0.00096875

$\approx (0.0101010100)_2 = (1.01010100)_2 \times 2^{-2} = 0.33203125$

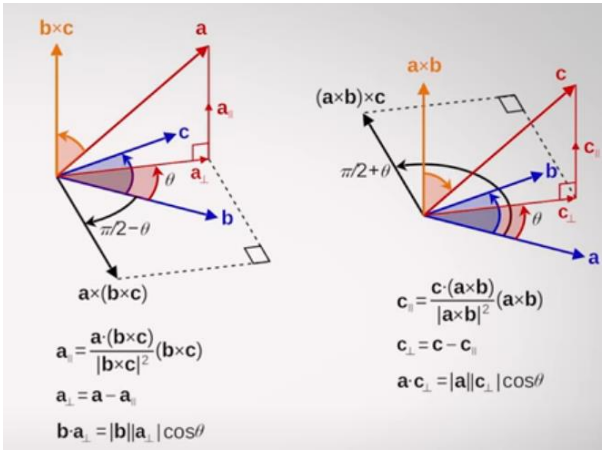
Not every number can be precisely interpreted!

Floating point number浮點運算

- Why use floating point number
  - Easy to interpret very small and very large numbers
  - For image rendering like fig (1), lots of vector based computation like fig (2) needed.

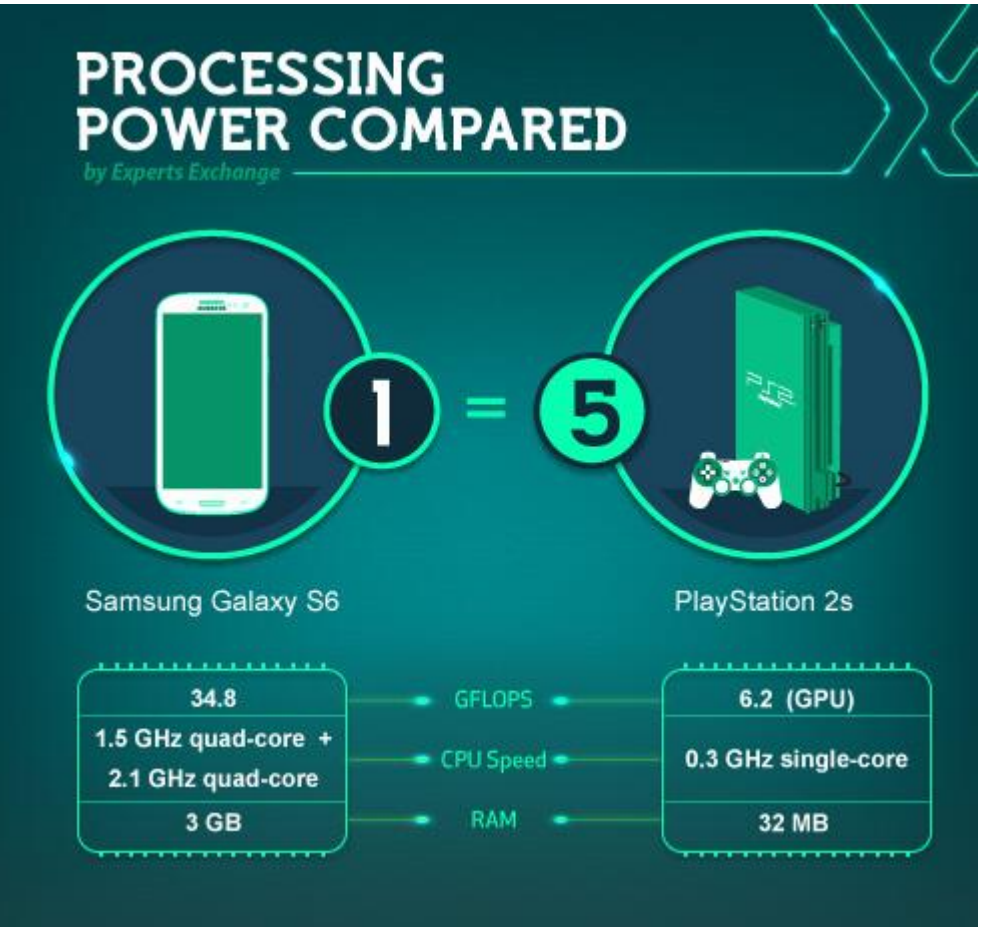


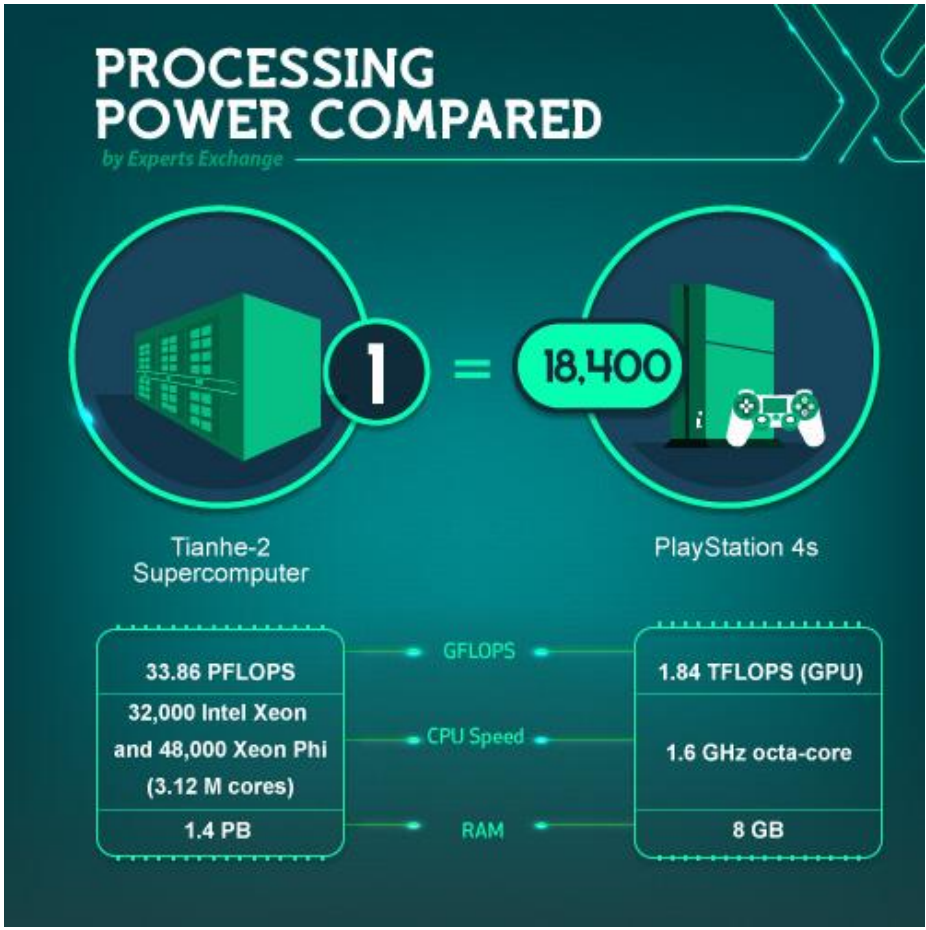
@Techquickie



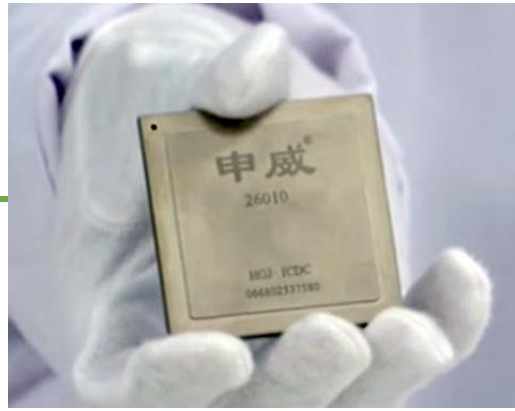
Polling FP

你的手機有多快？


PROCESSING
POWER COMPARED
by Experts Exchange
1
=
5
Samsung Galaxy S6
PlayStation 2s
34.8
1.5 GHz quad-core +
2.1 GHz quad-core
3 GB
GFLOPS
CPU Speed
RAM
6.2 (GPU)
0.3 GHz single-core
32 MB


PROCESSING
POWER COMPARED
by Experts Exchange
1
=
18,400
Tianhe-2
Supercomputer
PlayStation 4s
33.86 PFLOPS
32,000 Intel Xeon
and 48,000 Xeon Phi
(3.12 M cores)
1.4 PB
GFLOPS
CPU Speed
RAM
1.84 TFLOPS (GPU)
1.6 GHz octa-core
8 GB

Super Computer – World #4

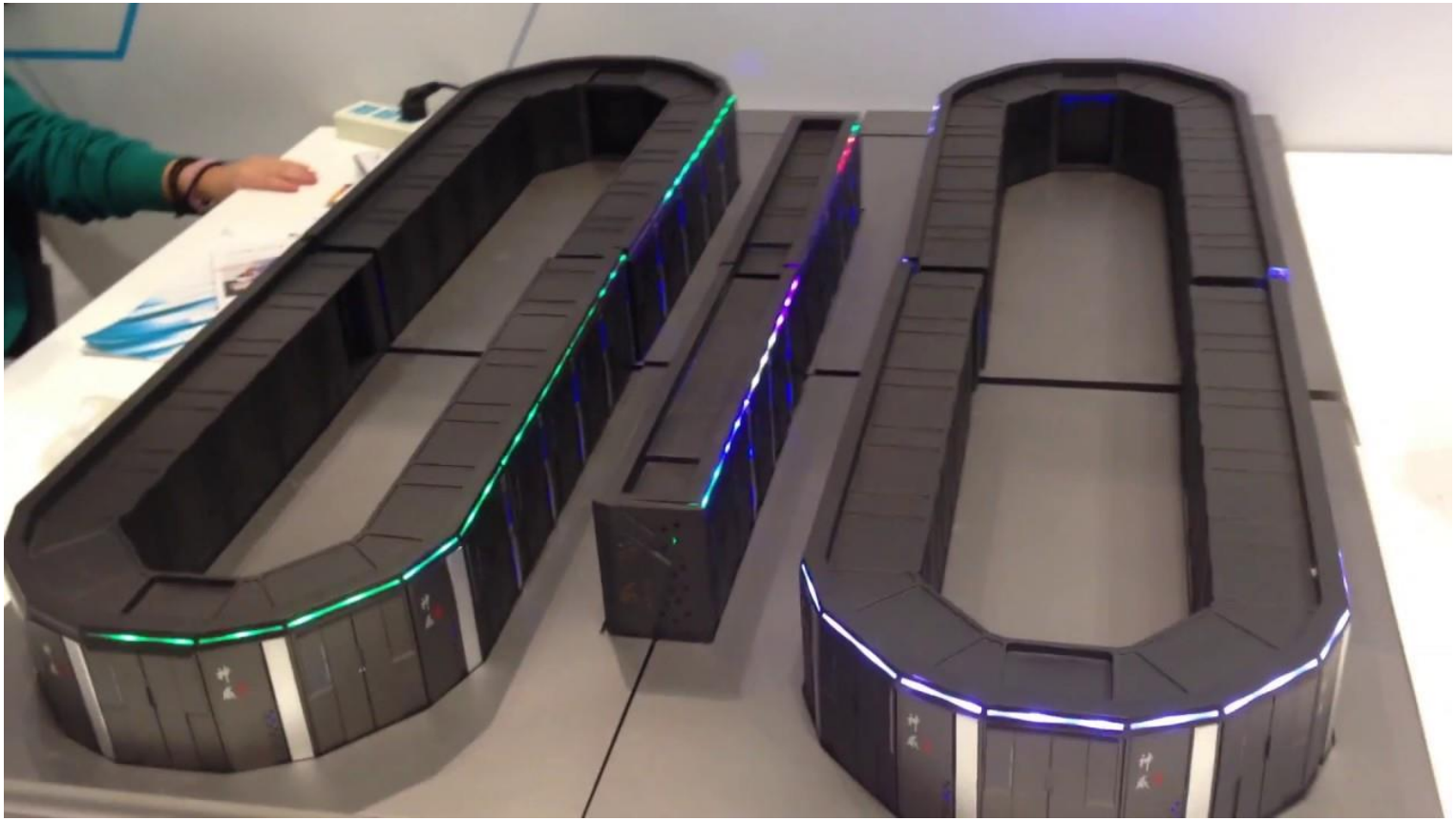


- In China, 125.4 PFLOP/s

InnoTech Expo 2017

2017 創科博覽 InnoTech Expo
鑑古追今 開創未來

- Design & Develop by Chinese Researchers
- What do you see below?

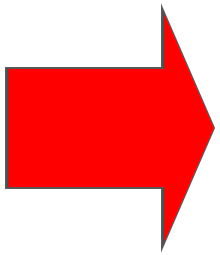


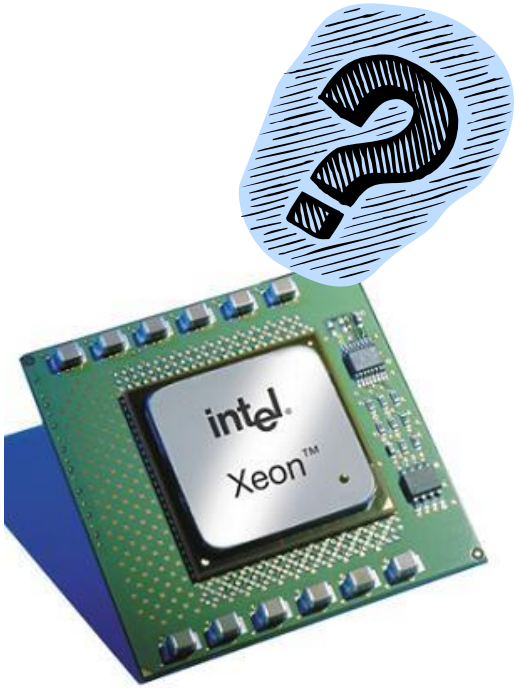
微處理器是如何製造的？

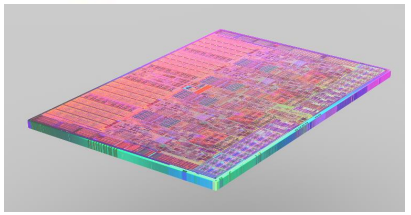
- Have you ever wondered how the microprocessor, the brain 'behind the magic' of your PC, is made?

用沙子做成的？

- Do you believe microprocessor is made from sand?

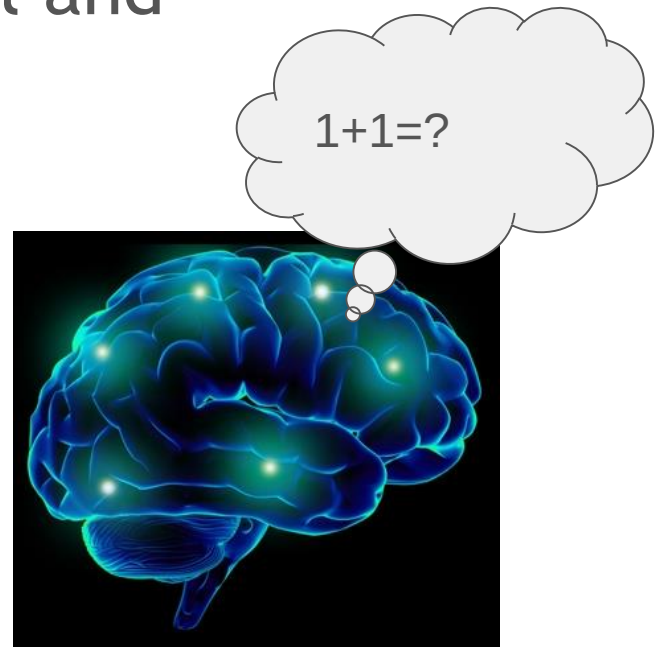






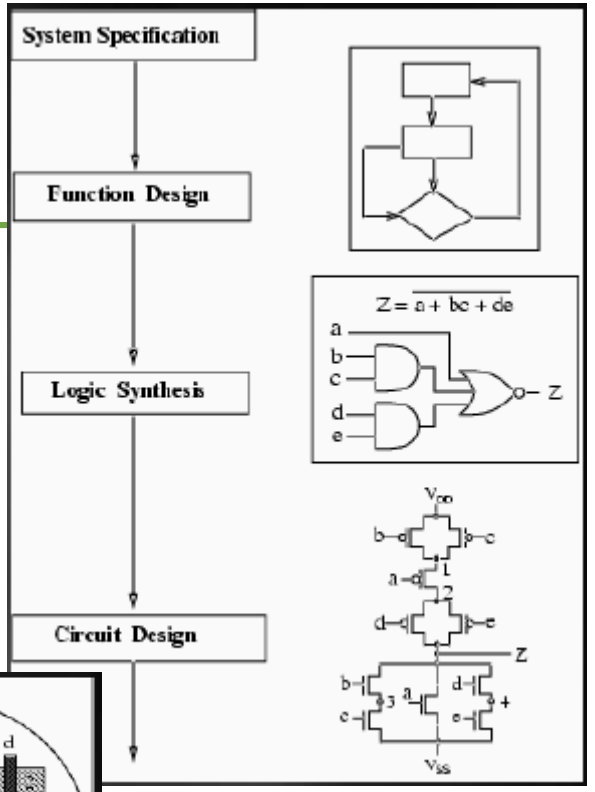
什麼是一加一？

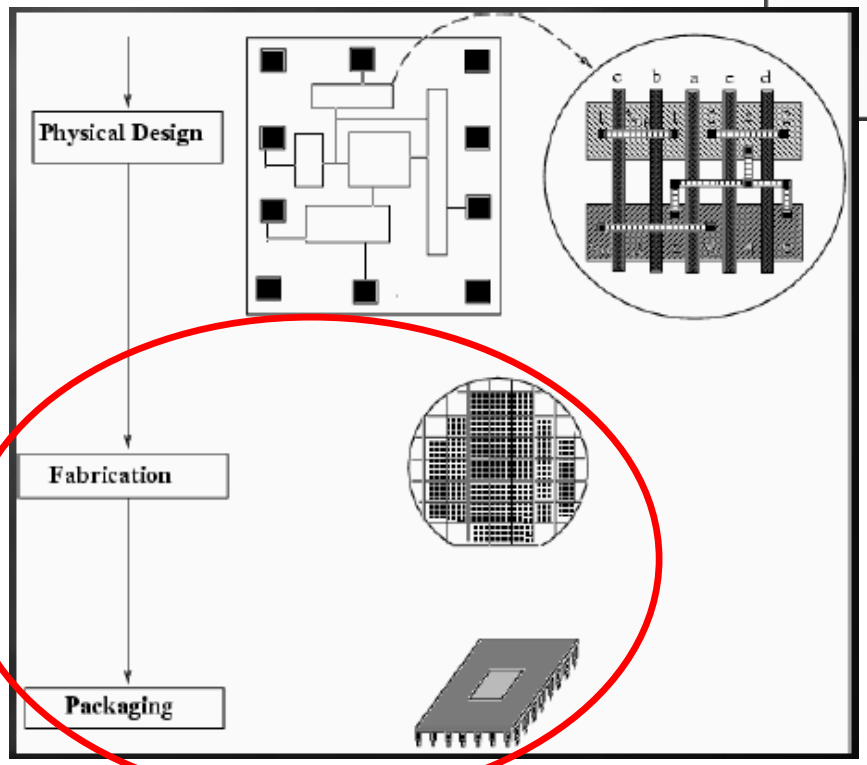
- Microprocessor is the brain of the computer and intelligent device
- Perform arithmetical, logical and input/output operations



芯片設計週期

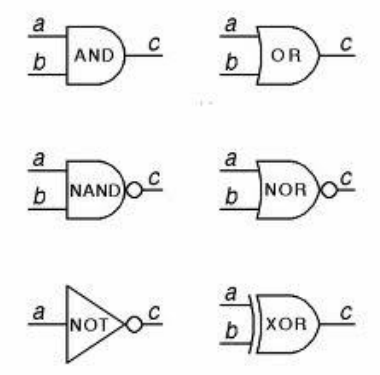
- Design Specification
- Functional Design
- Logic Design
- Circuit Design
- Physical Design
- Fabrication
- Packaging
- IC delivery



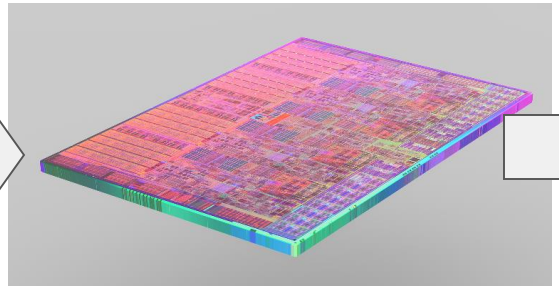


從邏輯門到 集成電路

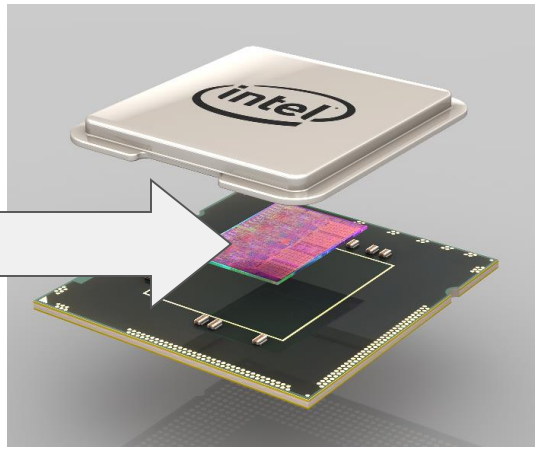
- Logic gates perform arithmetical, logical and input/output operations
- Key question: How to build the logic gates?



Logic gates



Microprocessor die



Microprocessor chip

AND gate / OR gate 與門/或門?

Truth Table for AND gate

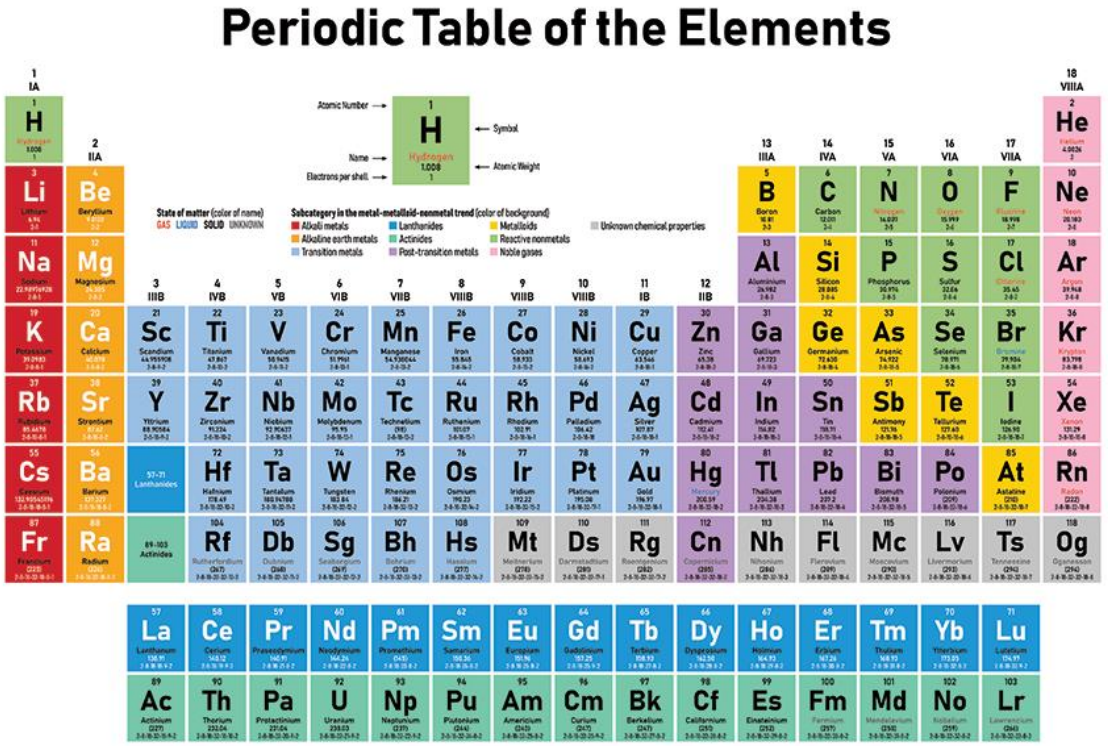
a	b	c
0	0	0
0	1	0
1	0	0
1	1	1
A	B	C

Truth Table for OR gate

d	e	f
0	0	0
0	1	1
1	0	1
1	1	1
D	E	F

製作芯片的材料

- Silicon (Si)
- is a semiconductor
  - an excellent conductor
  - an insulator of electricity, by the introduction of minor amounts of impurities

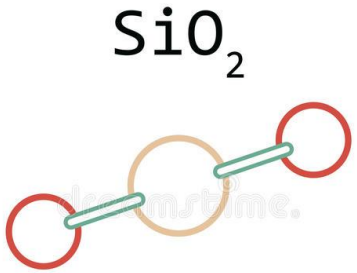


我們在哪裡可以找到矽？

- Sand composed of silicon dioxide
- the starting point for making a processor

製作芯片的材料

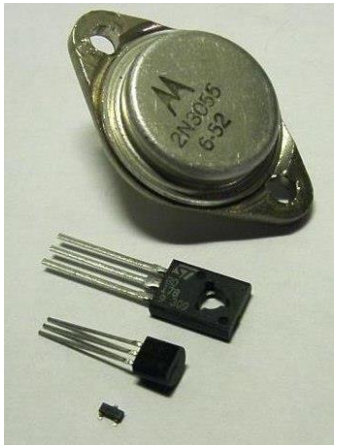
- Metal oxide semiconductor (MOS) structure is obtained by growing
  - a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of polycrystalline silicon



Silicon dioxide

電晶體

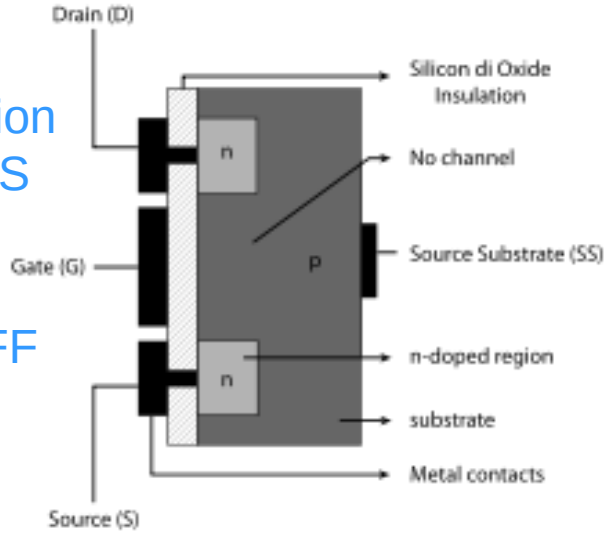
- 1947 by American physicists John Bardeen and Walter Brattain, William Shockley at Bell Labs.
- shared 1956 Nobel Prize in Physics



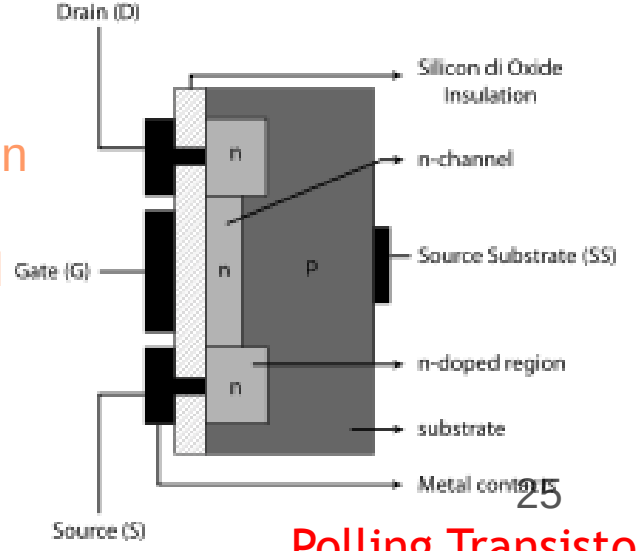
關於二氧化矽

- Silicon dioxide is
  - a dielectric material,
  - equivalent to a planar capacitor
  - with one of the electrodes replaced by a semiconductor
- A voltage is applied across a MOS structure
  - modifies the distribution of charges in the semiconductor

Cross section of an NMOS without channel formed: OFF state



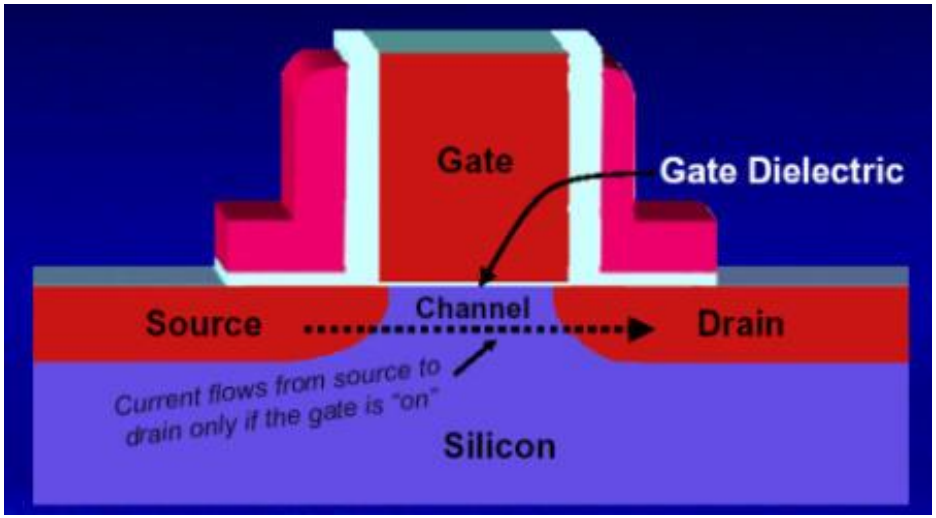
Cross section of an NMOS with channel formed: ON state

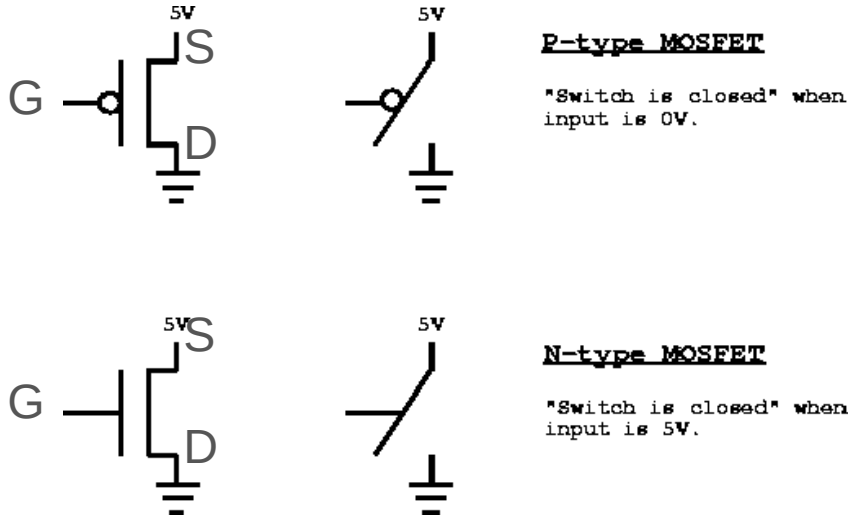


Polling Transistor

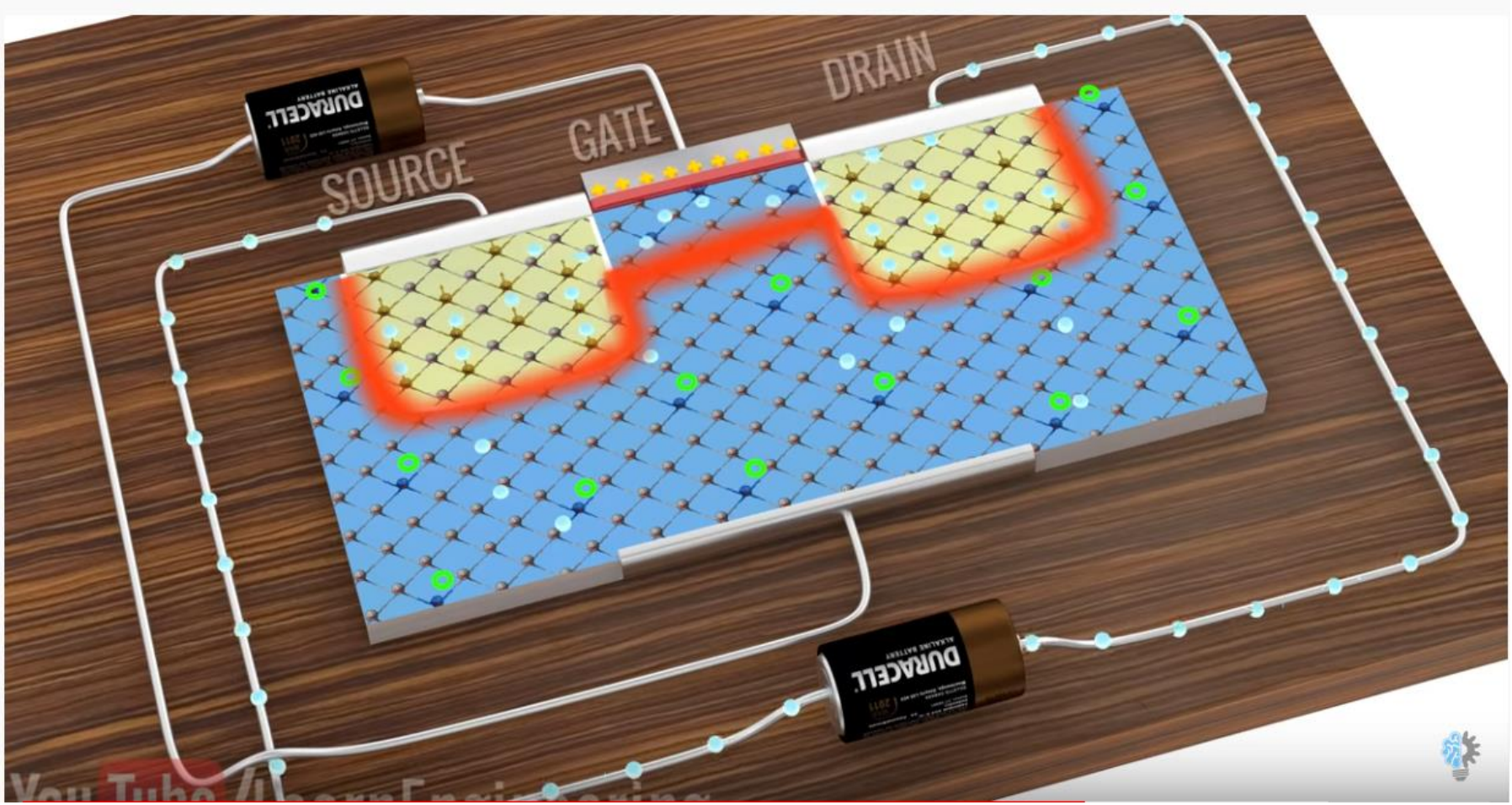
CMOS技術

- Current technology to create digital circuitry : CMOS (*complementary metal-oxide-semiconductor*)
- **CMOS** = **N-MOSFET** (n-type) + **P-MOSFET** (p-type)
- G=Gate, S=Source, D=Drain





Transistor 晶體管介紹視頻

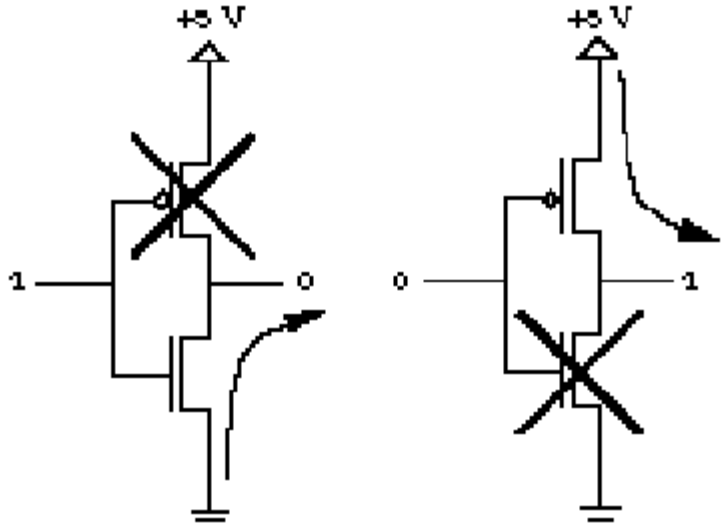


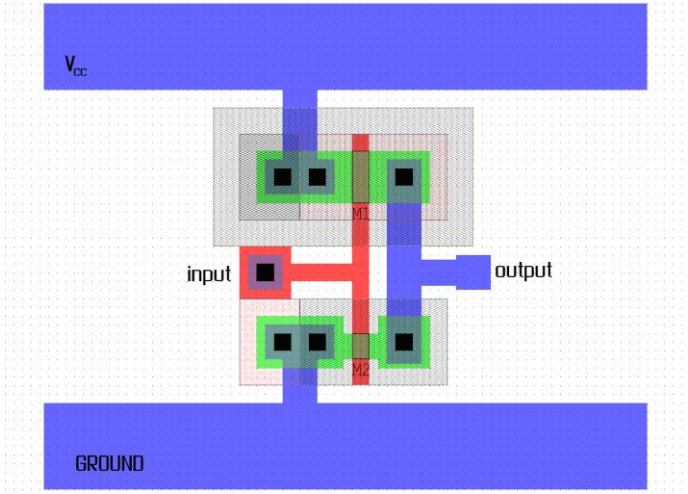
Ref: https://www.youtube.com/watch?v=stM8dgcY1CA

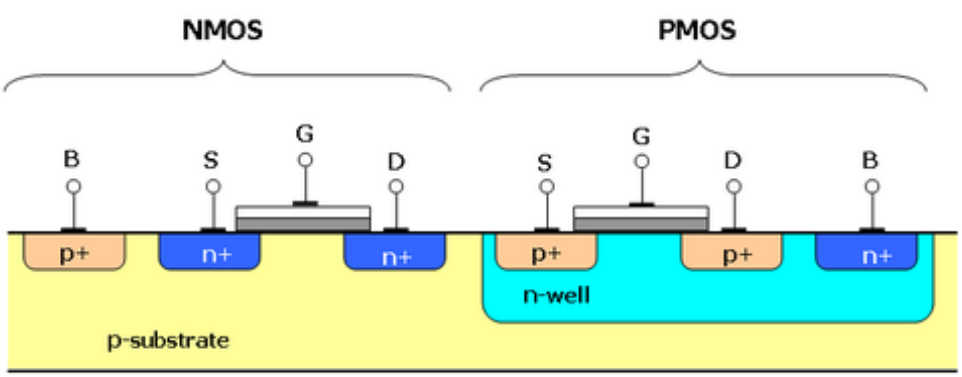
CMOS technology - Example

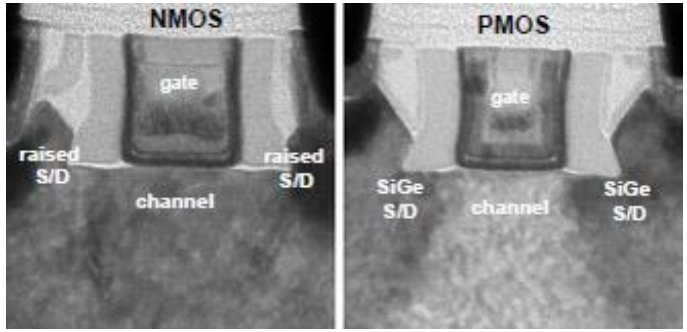
Polling Transistor

CMOS Inverter





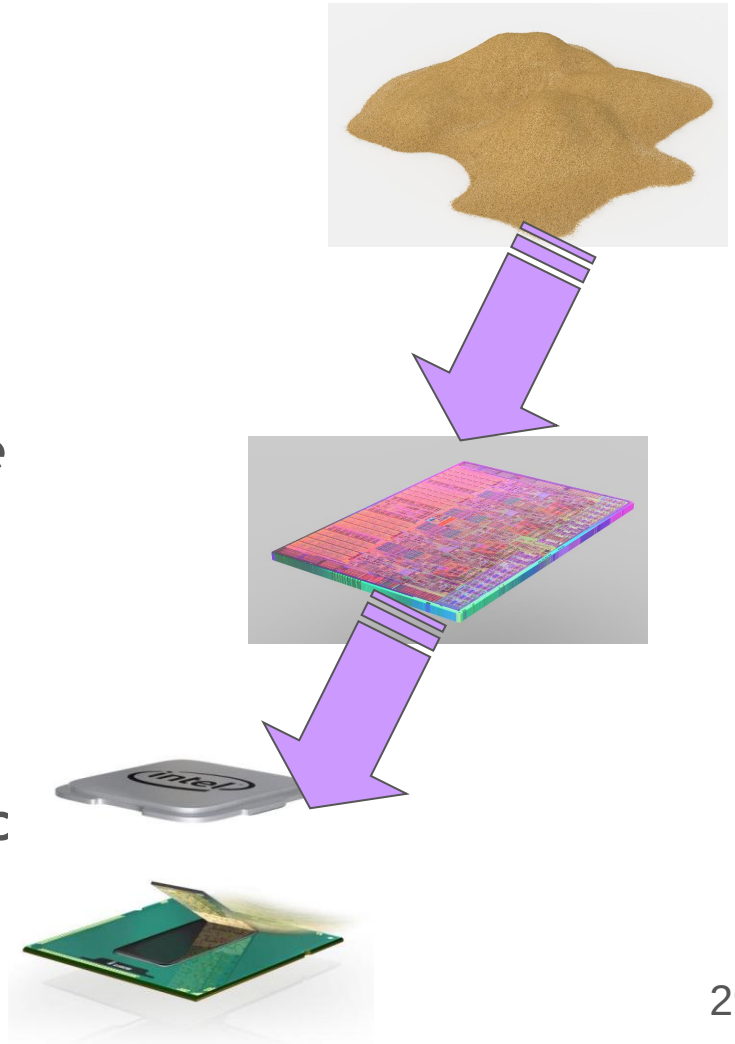




Cross section of two transistors in a CMOS gate, in an N-well CMOS process

製造芯片

- Sand / Ingot
- Ingot / Wafer
- Photo Lithography
- Ion Implantation
- Etching
- Temporary Gate Formation
- “Gate-Last” High-k/Metal Gate Formation
- Metal Deposition
- Metal Layers
- Wafer Sort / Singulation
- Packaging
- Class Testing / Completed Proc



芯片製造

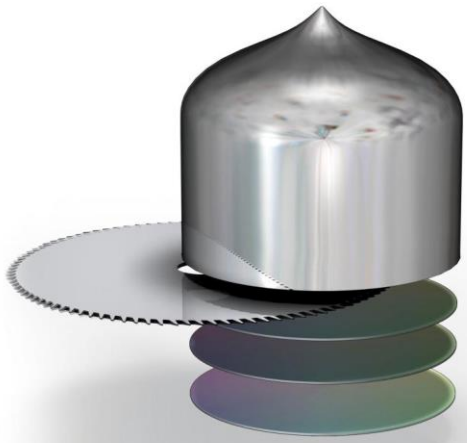
Sand / Ingot (錠, 鑄塊)

Sand -
Silicon is the second most abundant element in the earth's crust

Melted Silicon -
Sand is melted and allowed to cool down into a solid which is a single, continuous and unbroken crystal lattice in the shape of a cylinder

Monocrystalline Silicon Ingot

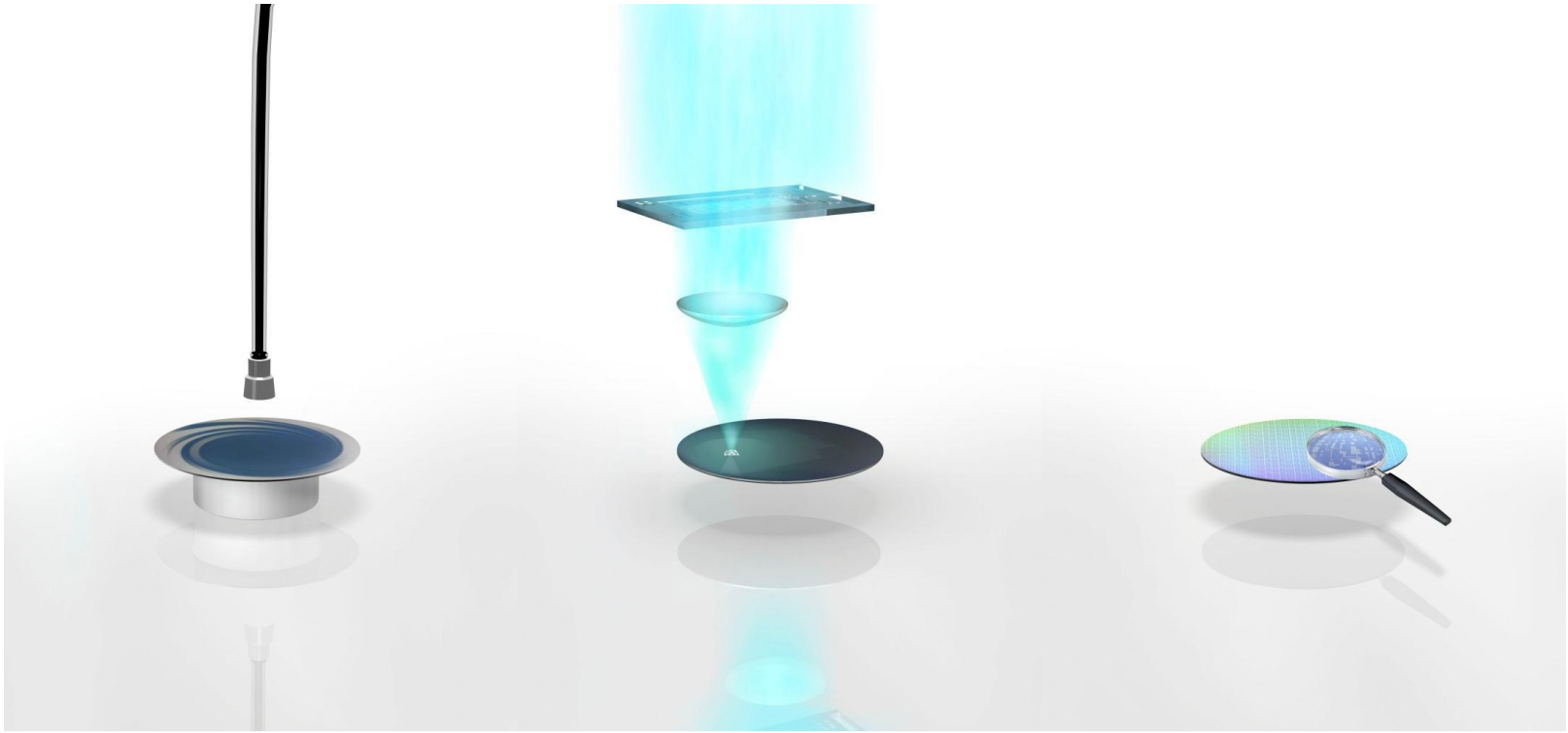
Ingot / Wafer (薄片；圓片；晶片)



Ingot Slicing -
The ingot is cut into individual silicon discs called wafers

Wafer -
The wafers are polished until they have flawless, mirror-smooth surfaces.

Photo Lithography (平版印刷術)



Applying Photoresist **-** Photolithography is the process by which a specific pattern is imprinted on the wafer.

Exposure - The photoresist is hardened, and portions of it are exposed to ultra violet (UV) light, making it soluble.

Resist Development - The soluble photoresist is removed by a chemical process,

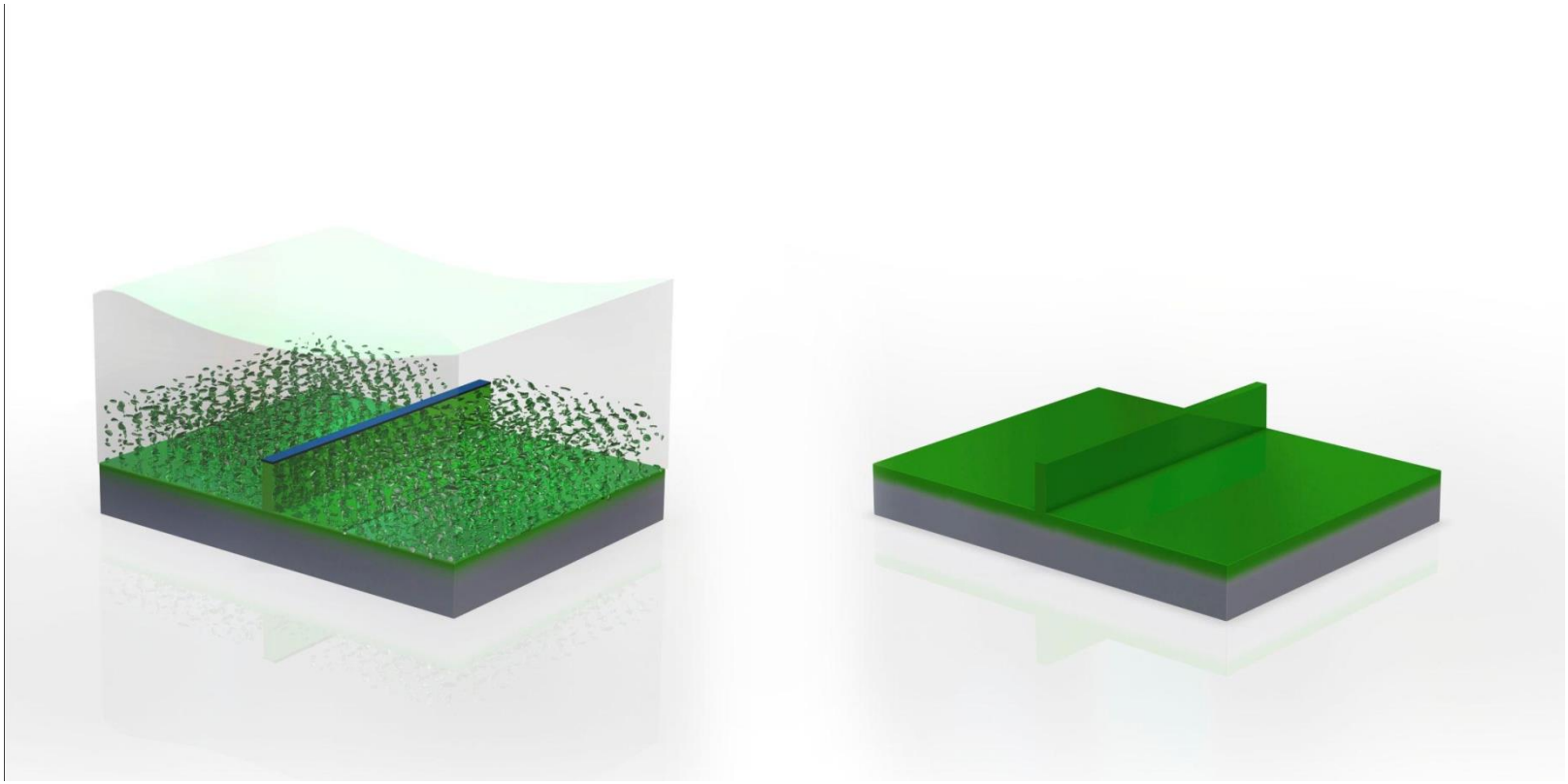
Ion Implantation (植入術)

Ion Implantation -
The wafer with patterned photoresist is bombarded with a beam of ions

Removing Photoresist -
After ion implantation, the photoresist is removed and the resulting wafer has a pattern of doped regions in which transistors will be formed.

Begin Transistor Formation -
a tiny part of the wafer, where a single transistor will be formed.

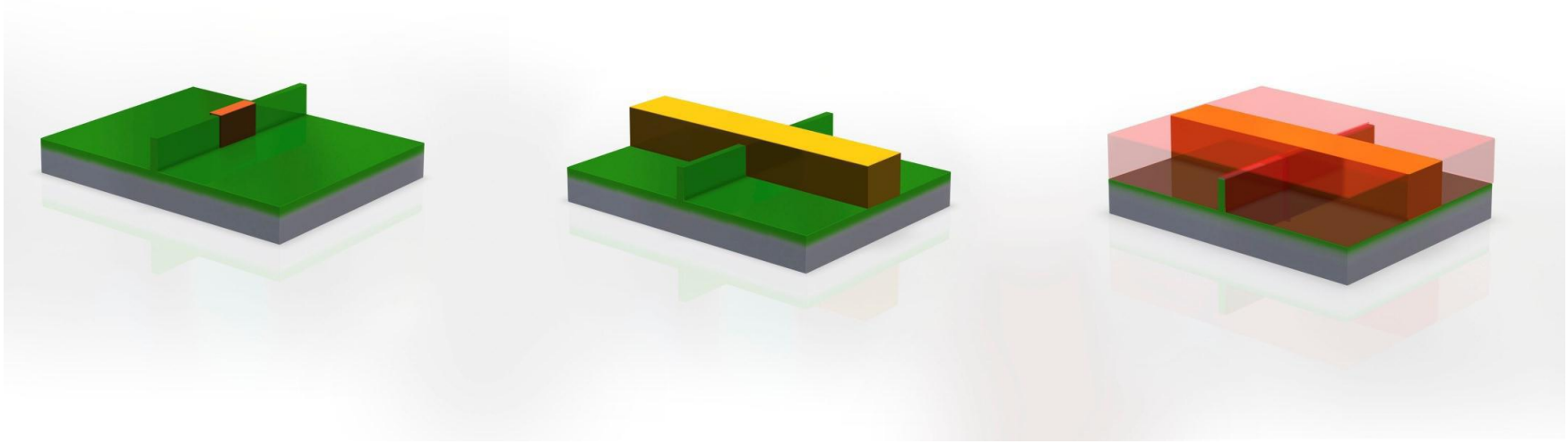
Etching (蝕刻術)



Etch -
Remove unwanted silicon

Removing Photoresist -
The hard mask is chemically removed

形成邏輯門 Logic Gate

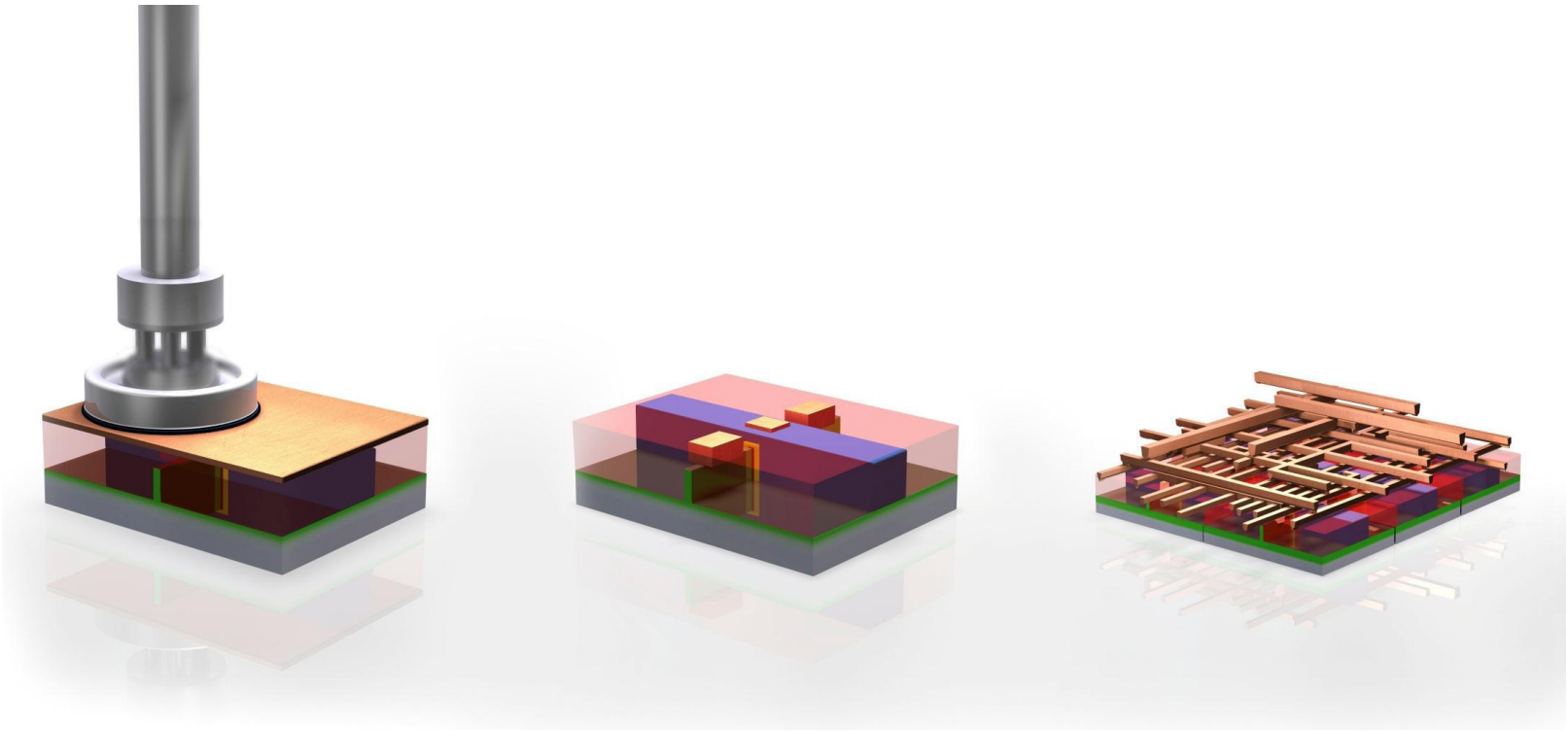


Silicon Dioxide Gate Dielectric -
the transistor are covered with photoresist and a thin silicon dioxide layer (red)

Polysilicon Gate Electrode -
temporary layer of polycrystalline silicon (yellow) is created

Insulator -
a silicon dioxide layer is created over the entire wafer

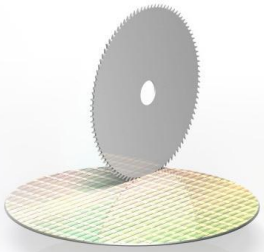
Metal Layers 金屬層



Polishing -
The excess material is mechanically polished away

Metal Layers -
Multiple metal layers are created to interconnect (wires) all the transistors on the chip in a specific configuration.

Wafer Sort / 單數化

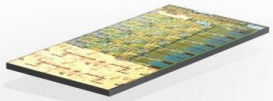


Wafer Sort -
This portion of a ready wafer is being put through a test.

Wafer Slicing

Selecting Die for Packaging

Packaging (包裝術)



Individual Die

Packaging -
The package substrate, the die and the heat spreader are put together to form a completed processor.

Processor

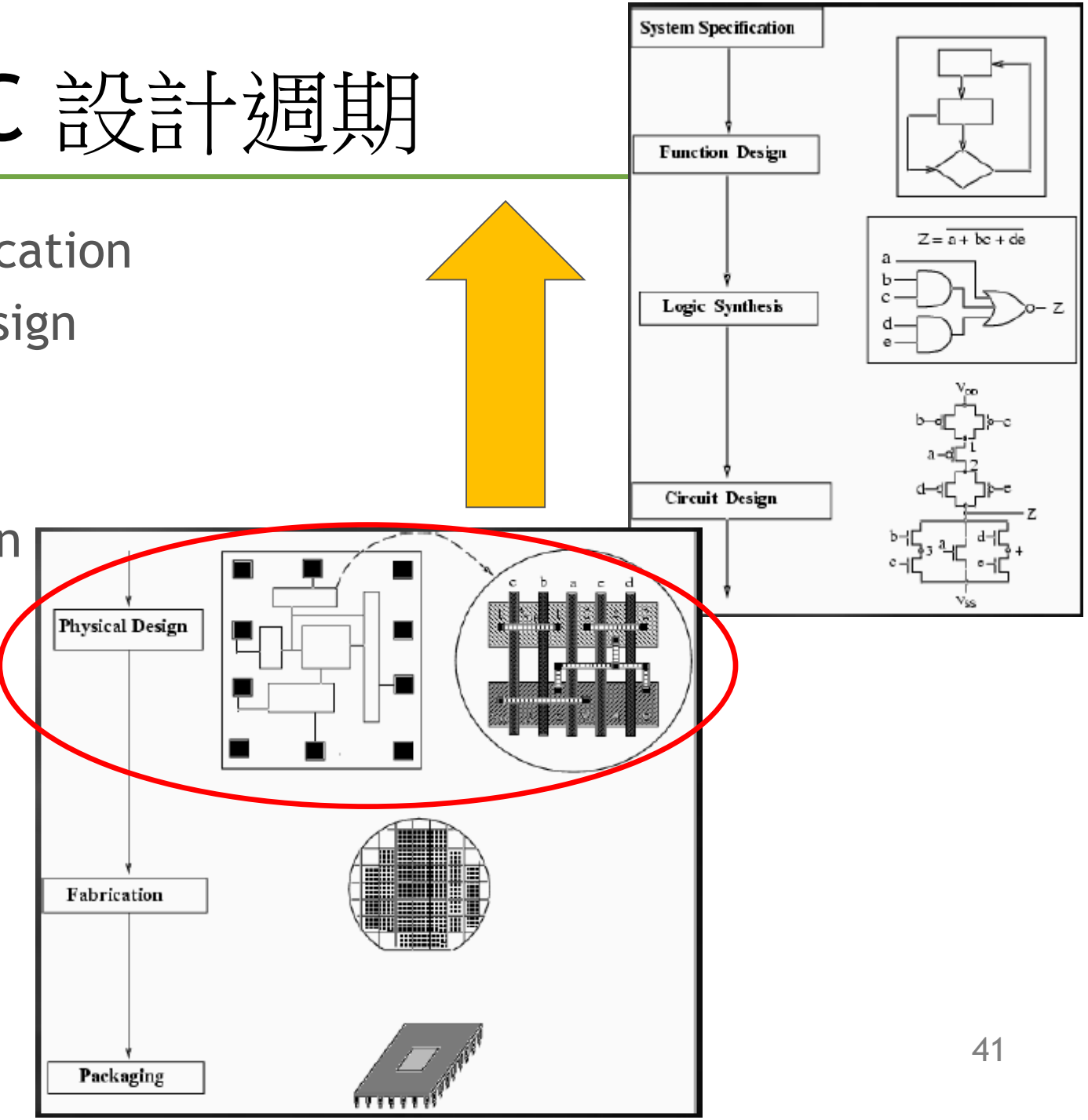
Class Testing / 測試中

Class Testing -
During this final test the processor is thoroughly tested for functionality, performance and power.

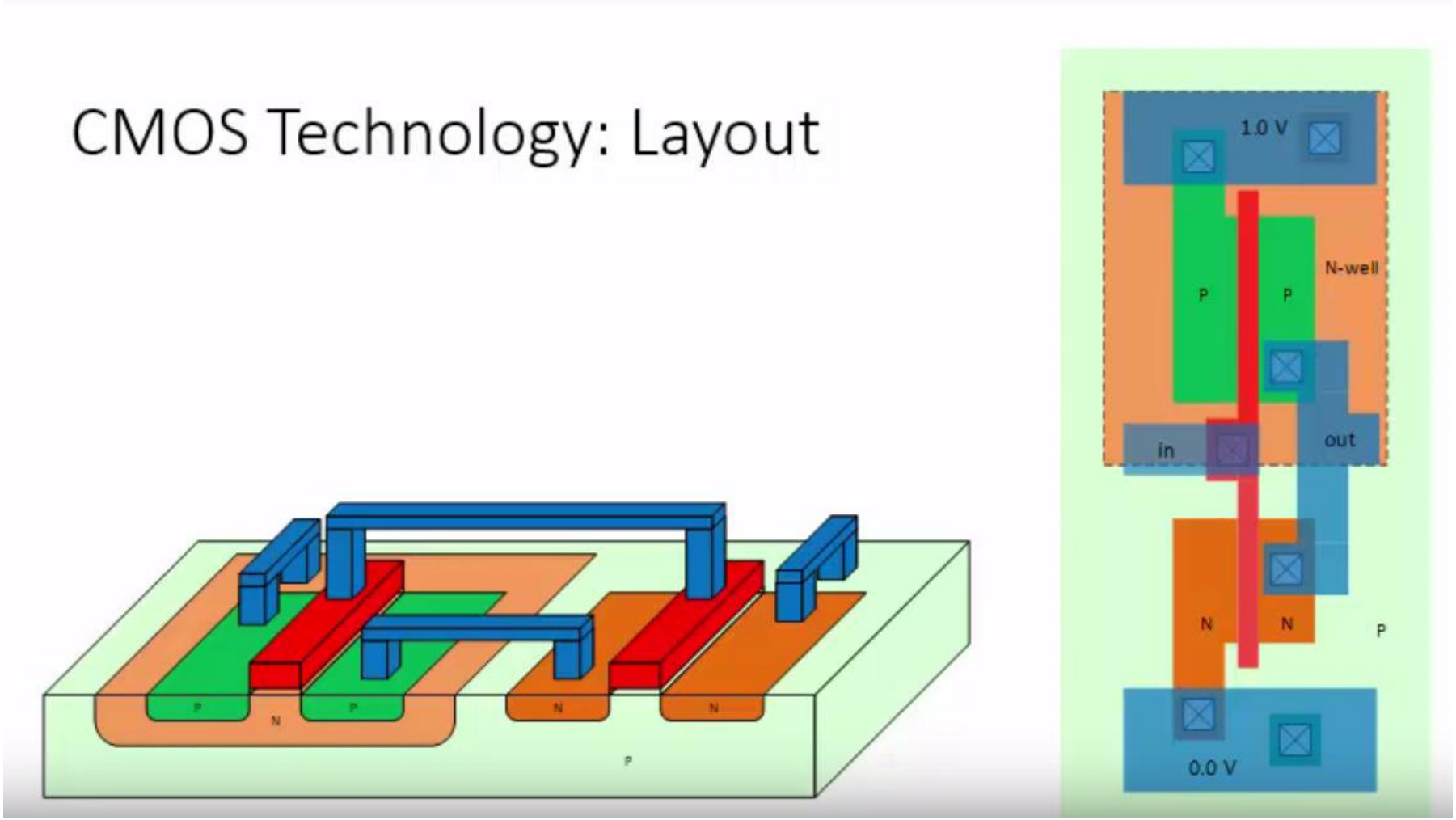
Binning -
Based on the test result of class testing, processors with equal capabilities are binned together in trays, ready for shipment to customers

IC 設計週期

- Design Specification
- Functional Design
- Logic Design
- Circuit Design
- Physical Design
- Fabrication
- Packaging
- IC delivery



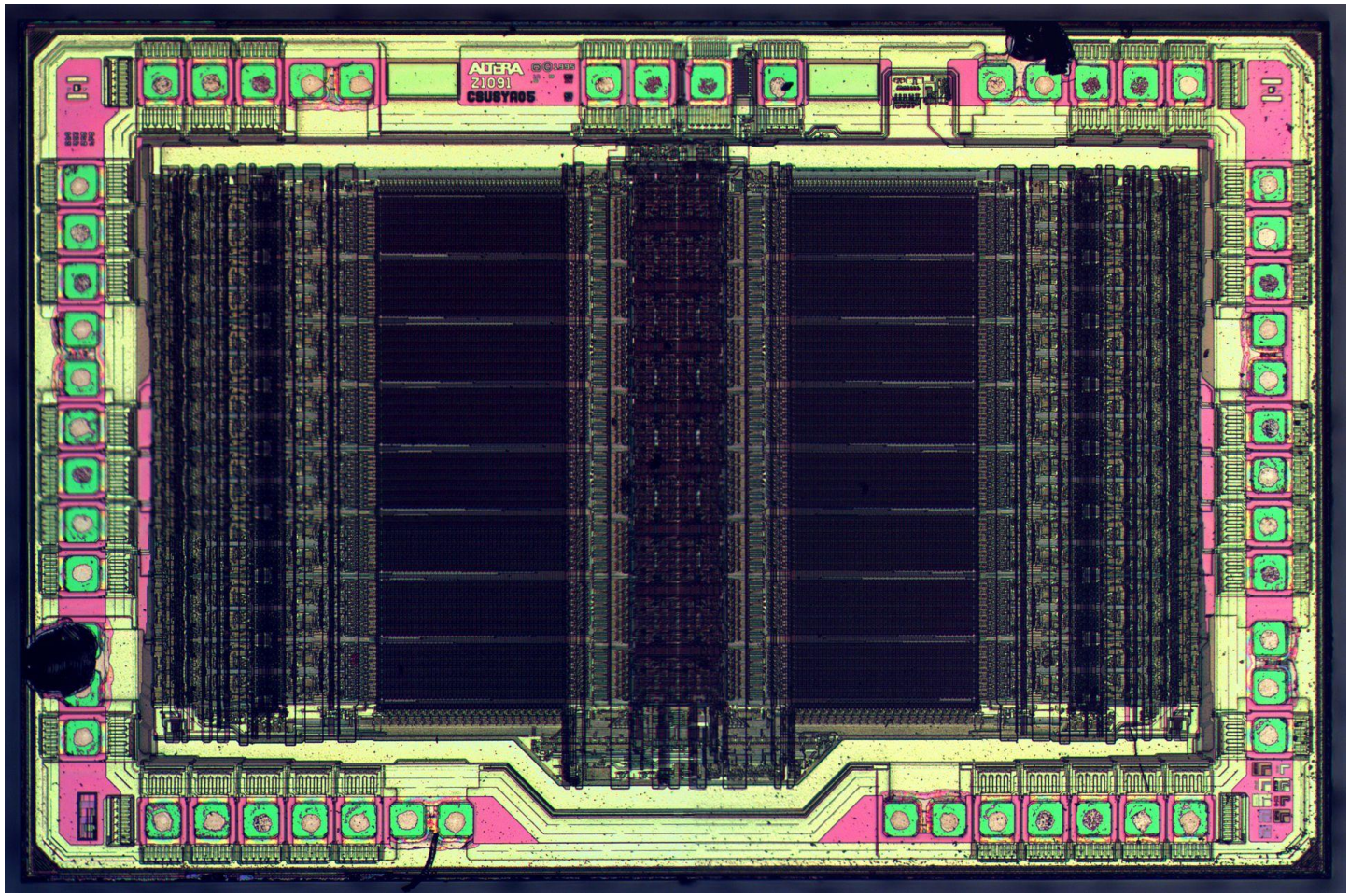
芯片佈局



Ref: https://www.youtube.com/watch?v=oSrUsM0hoPs

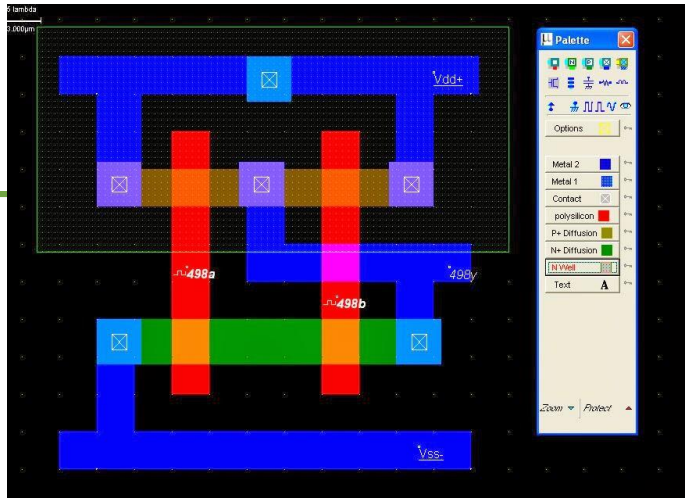
芯片佈局

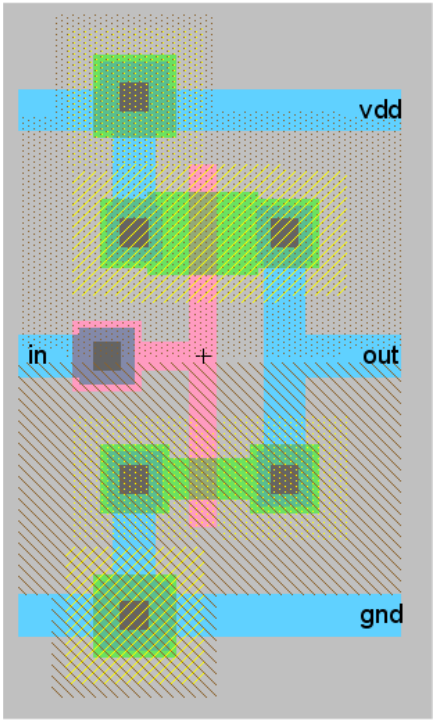
- Complex Programmable Logic Devices (CPLDs):
  - Come in sizes ranging from 500 to 16,000 gates.

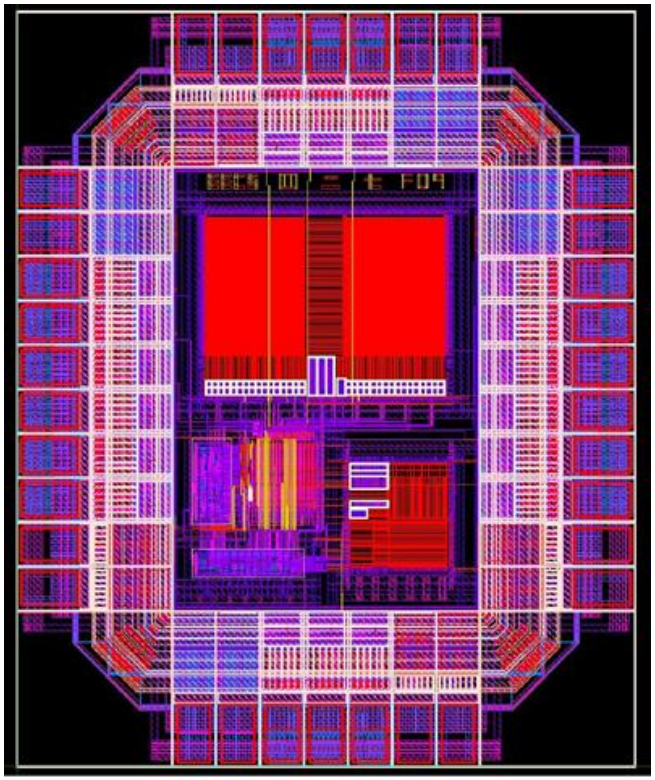


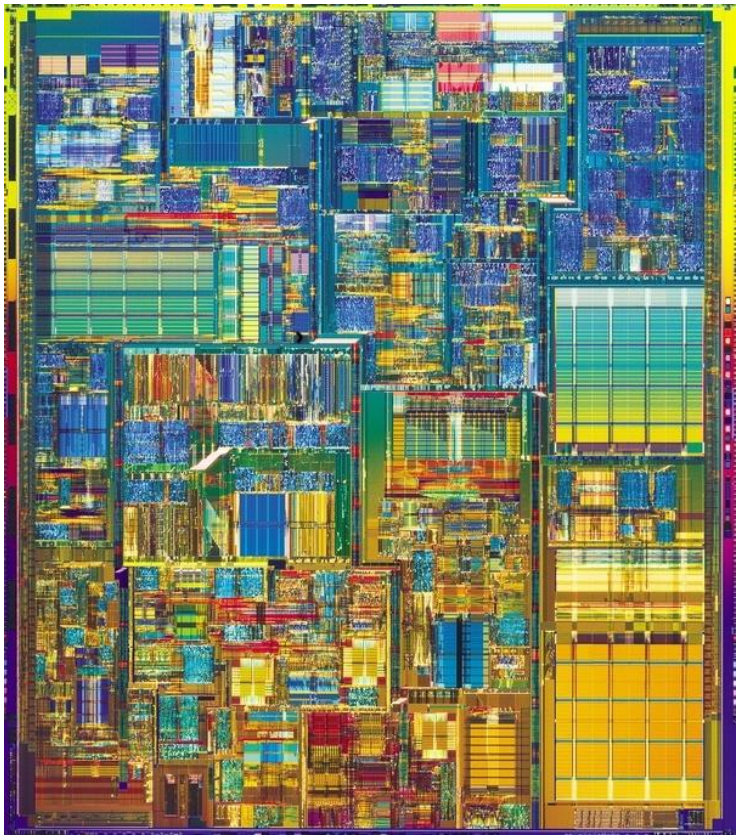
集成電路佈局

- Automatic Layout Generation
- Layout Engineers

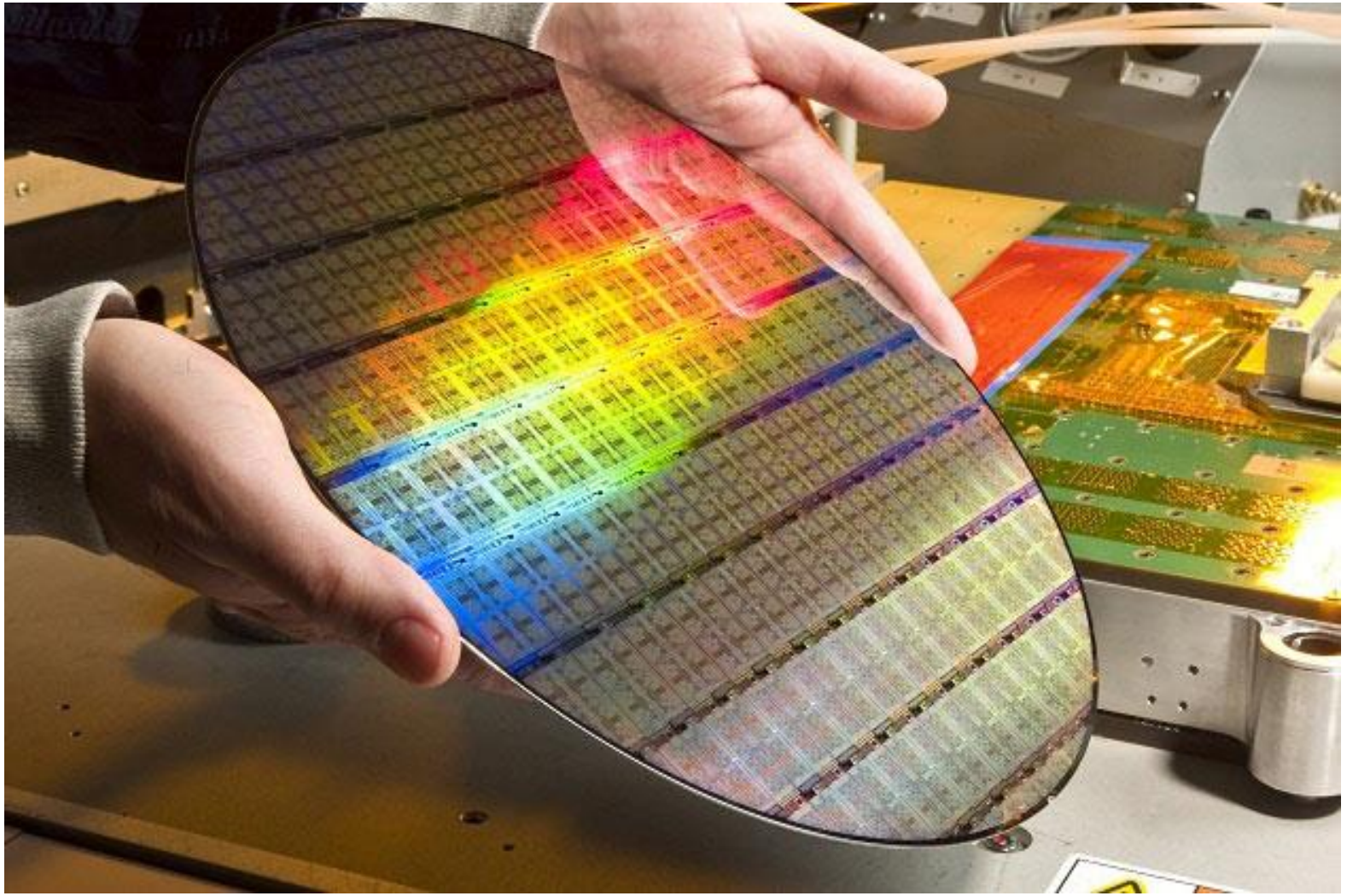




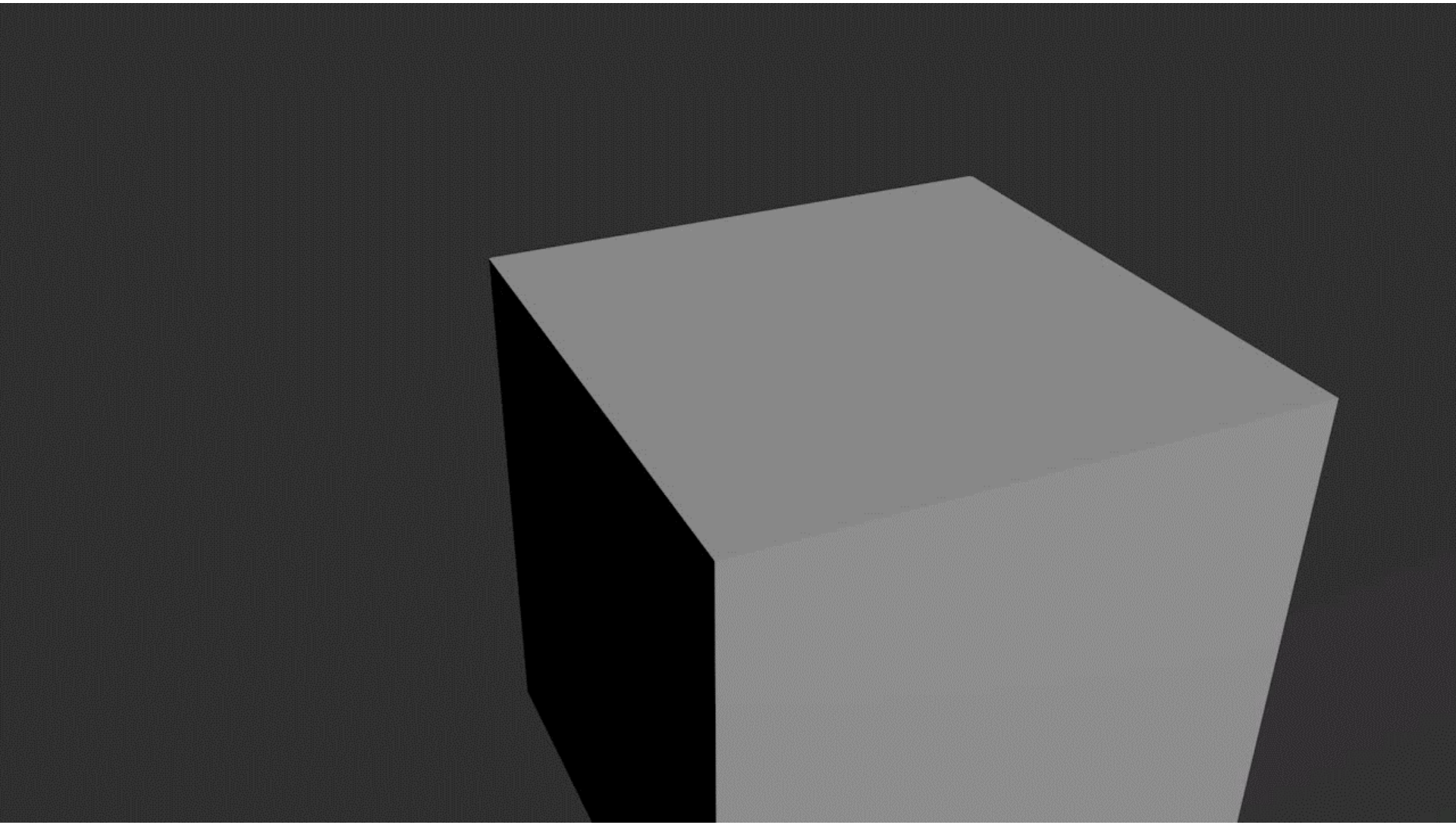




TSMC 台積電工藝技術



納米 one billionth of a meter



- 1×10^{-9} m

1 nanometer

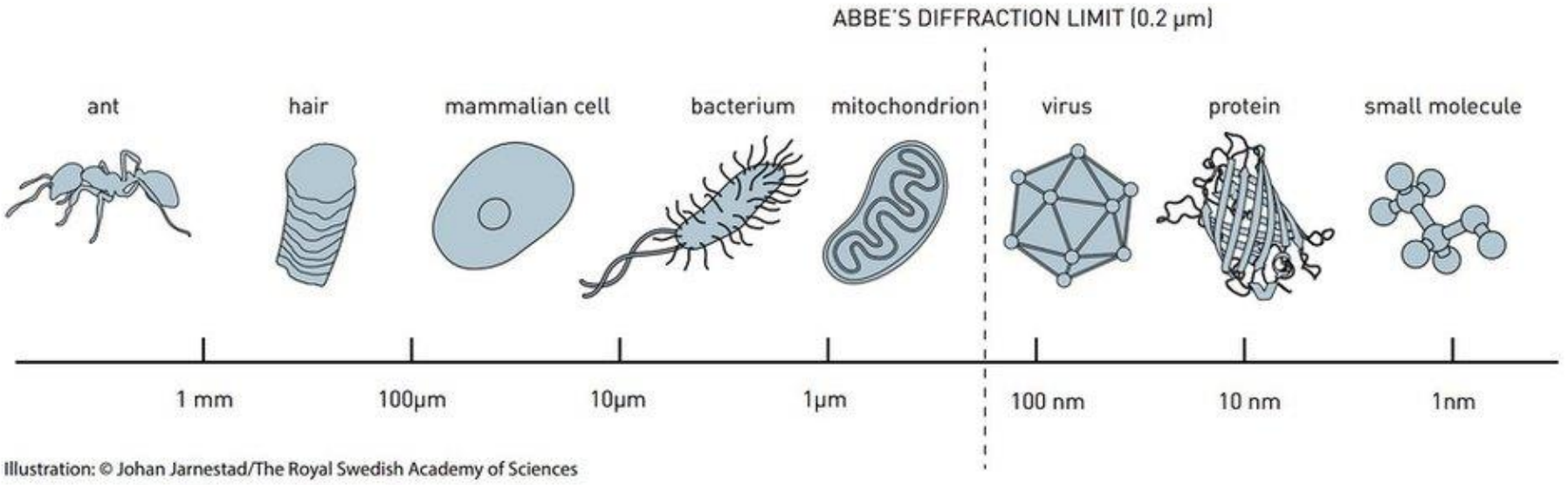
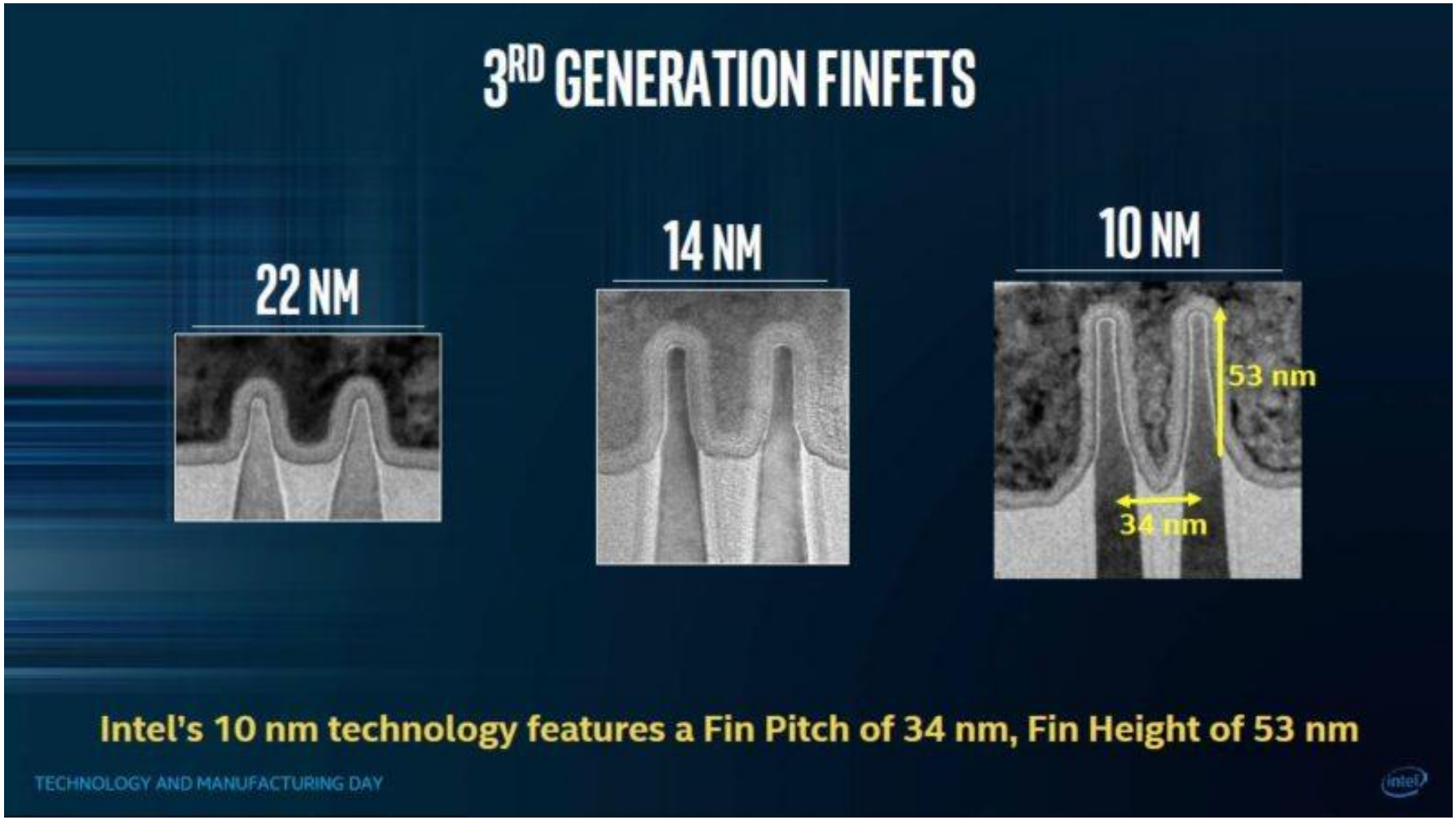
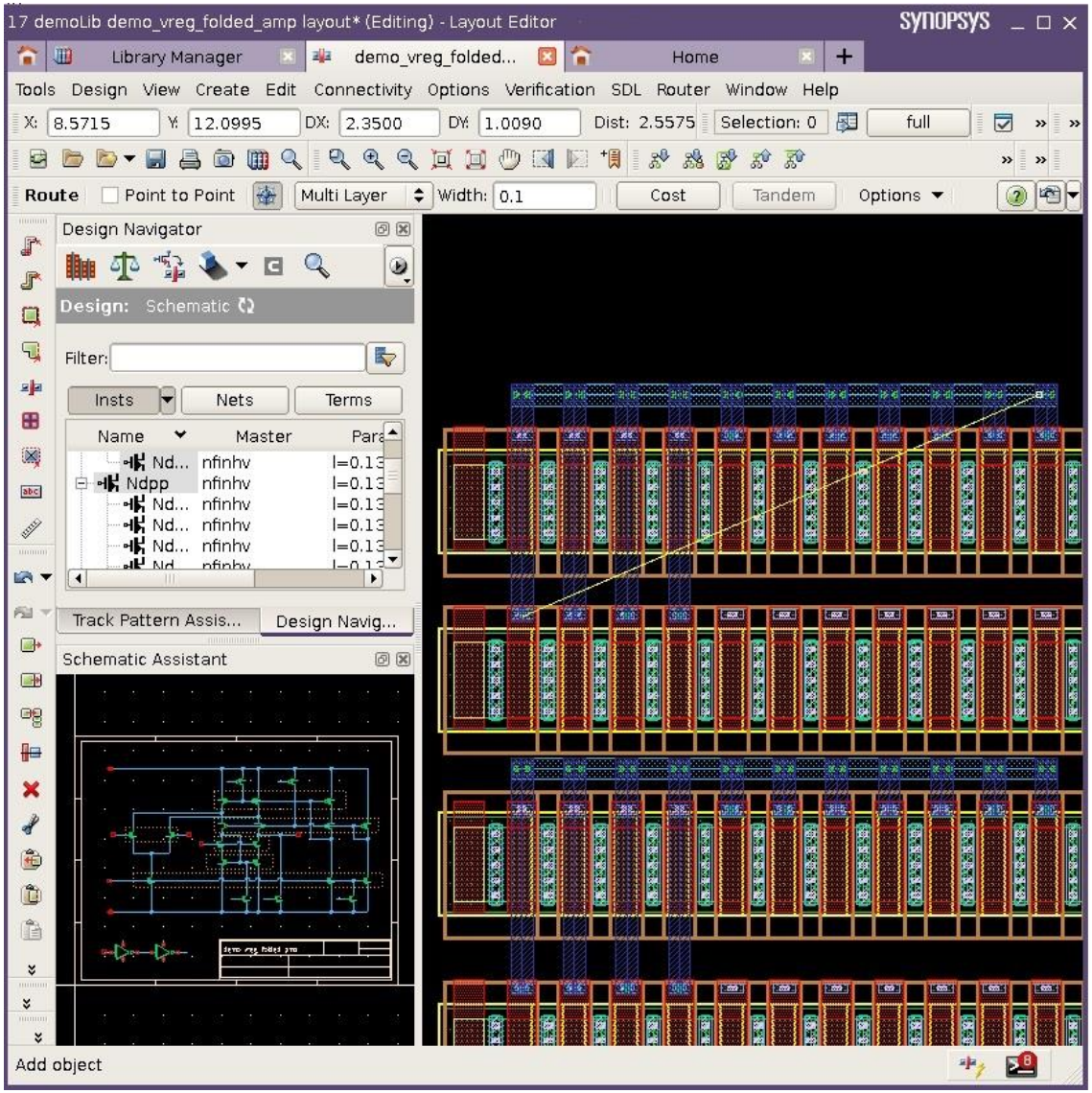


Illustration: © Johan Jarnestad/The Royal Swedish Academy of Sciences

22nm vs. 10nm vs. 7nm



Complexity: 電子設計自動化（EDA）



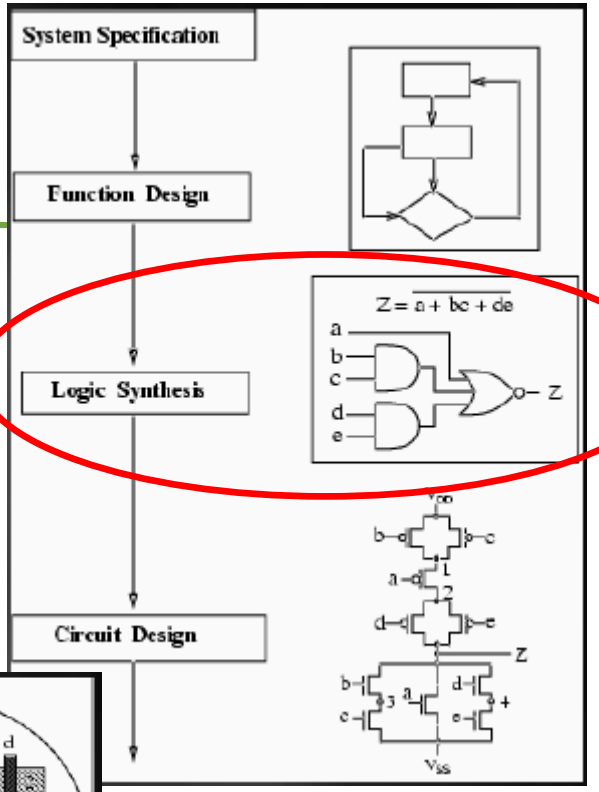
Synopsys, Inc.

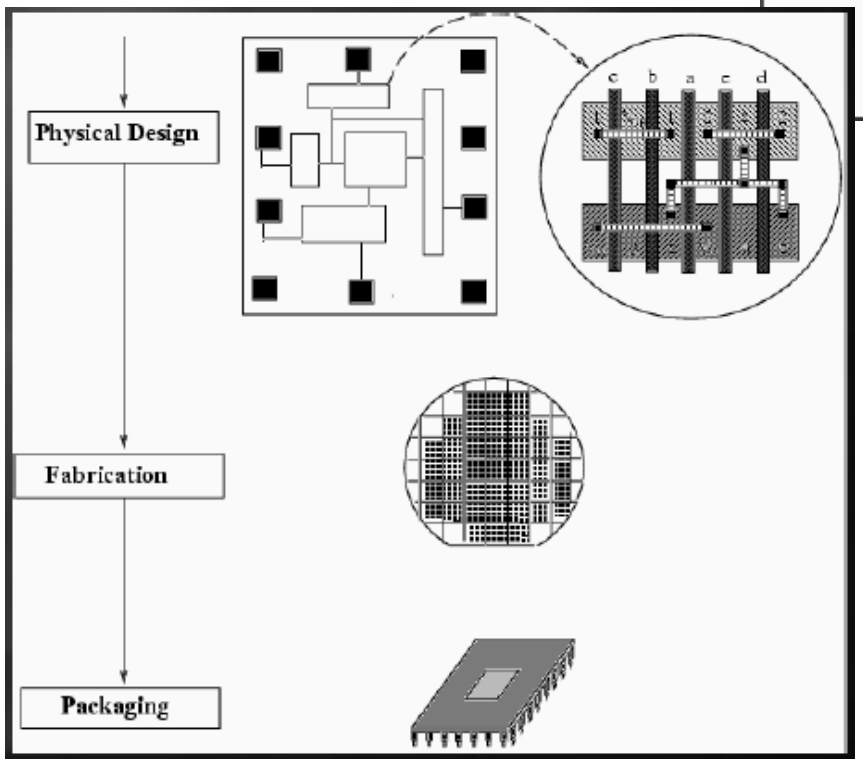
SYNOPSYS®

Type	Public
Traded as	NASDAQ: SNPS NASDAQ-100 component S&P 500 component
ISIN	US8716071076
Industry	Integrated circuit Self-driving car Software as a service Software Testing Internet of Things
Predecessor	C Level Design
Founded	1986 in Research Triangle Park, North Carolina.
Founder	David Gregory Aart de Geus
Headquarters	Mountain View, California, U.S.
Key people	Aart J. de Geus (Founder, Chairman & co-CEO) Chi-Foon Chan (President & co-CEO)
Revenue	▲ US$3.3 billion (2019)[1]
Net income	▲ US$625 million (2019)[1]
Number of employees	13,000[2]

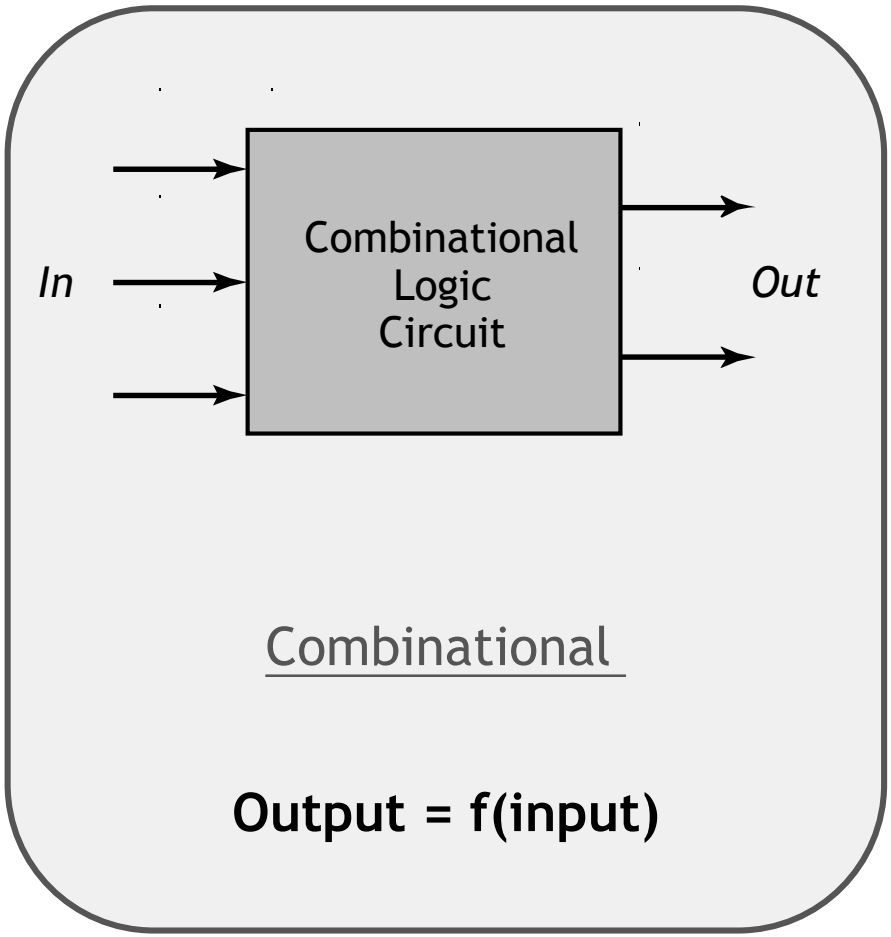
芯片設計週期

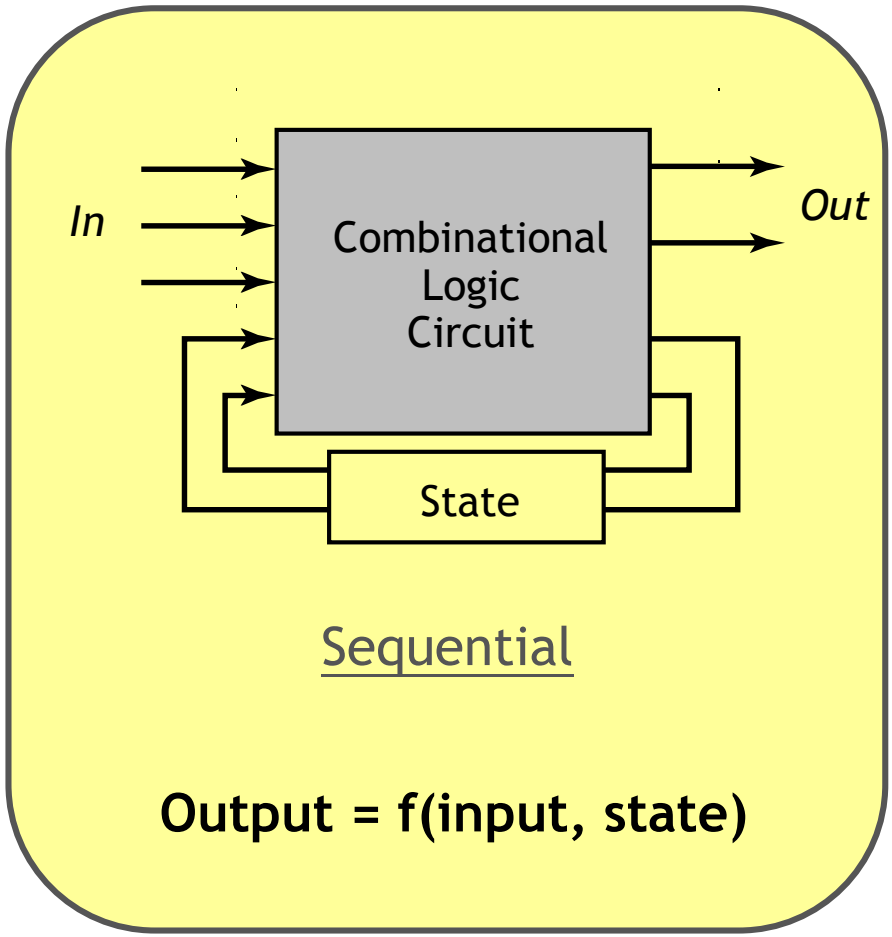
- Design Specification
- Functional Design
- Logic Design
- Circuit Design
- Physical Design
- Fabrication
- Packaging
- IC delivery





組合邏輯 與 順序邏輯


In
Combinational
Logic
Circuit
Out
Combinational
Output = f(input)

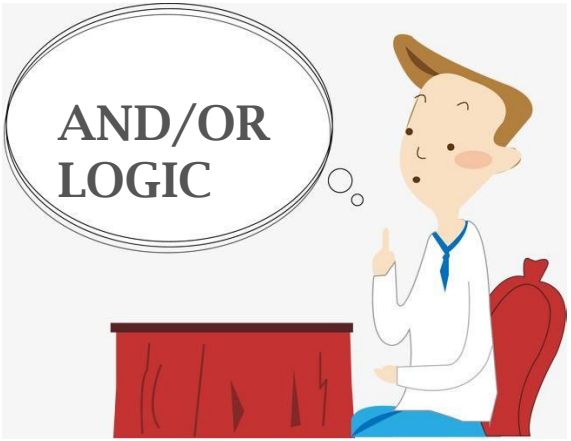

In
Combinational
Logic
Circuit
Out
State
Sequential
Output = f(input, state)

硬件描述語言格式和語法

- A Way to Describe our IC in a human readable format

```
ENTITY and_gate IS
PORT (    a, b    :IN BIT;
          y       :OUT BIT);
END and_gate;
ARCHITECTURE ckt OF and_gate IS
BEGIN
        y <= a AND b;
END ckt;
```

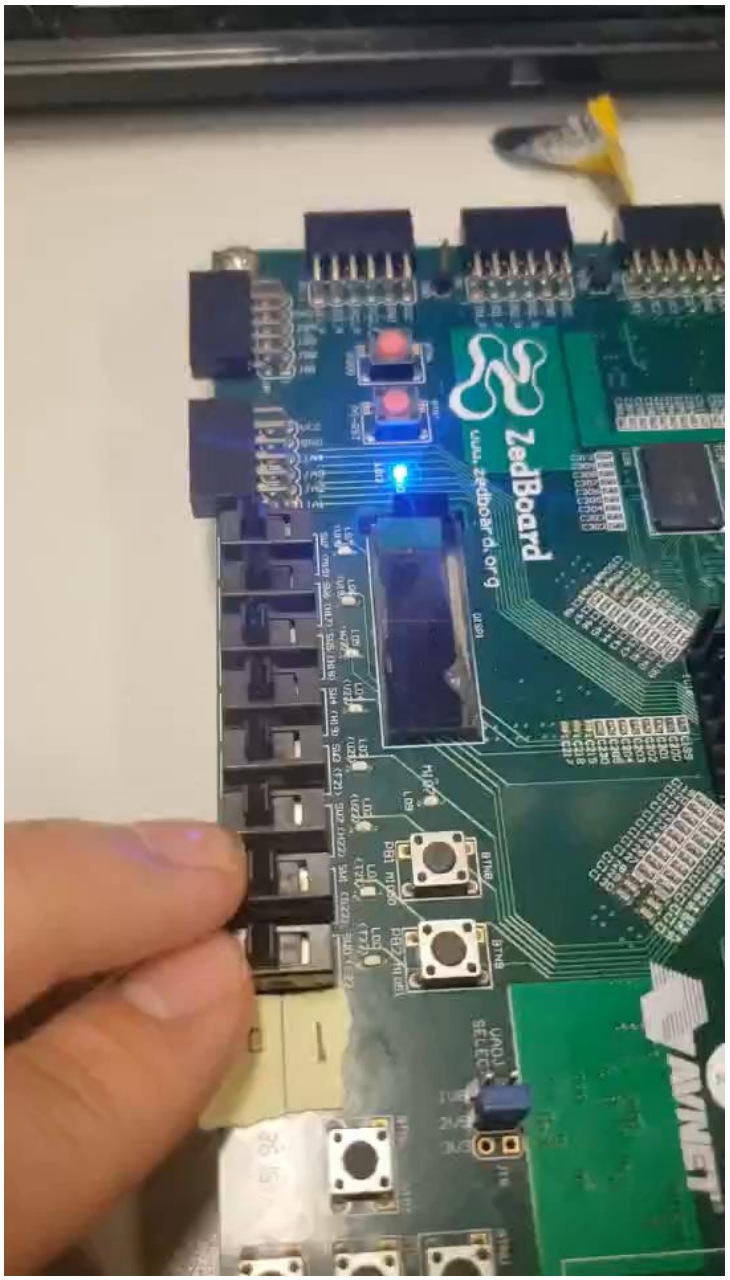
簡單的VHDL設計




```
2   LIBRARY IEEE;
3   USE IEEE.STD_LOGIC_1164.ALL;
4   ENTITY and2 IS
5       PORT(a,b:IN STD_LOGIC;
6            d,e:IN STD_LOGIC;
7            c:OUT STD_LOGIC;
8            f:OUT STD_LOGIC);
9   END and2;
10  ARCHITECTURE and2_behavior OF and2 IS
11  BEGIN
12      c<= a AND b;
13      f<= d OR e;
14  END and2_behavior;
```

F
E
D

C
B
A



Polling Logic

芯片設計週期

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- Physical Design
- Fabrication
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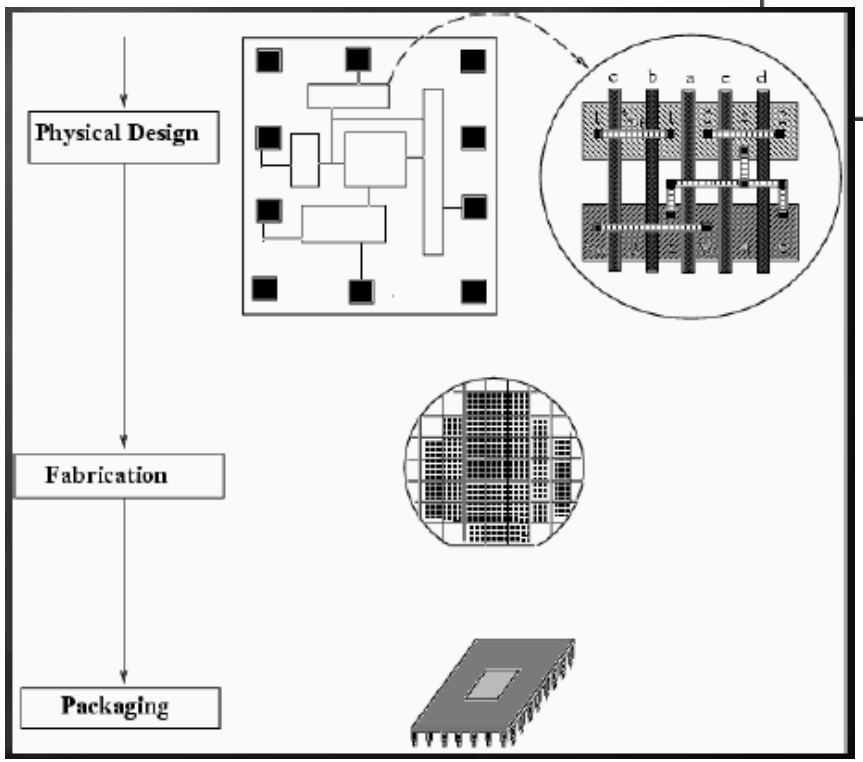
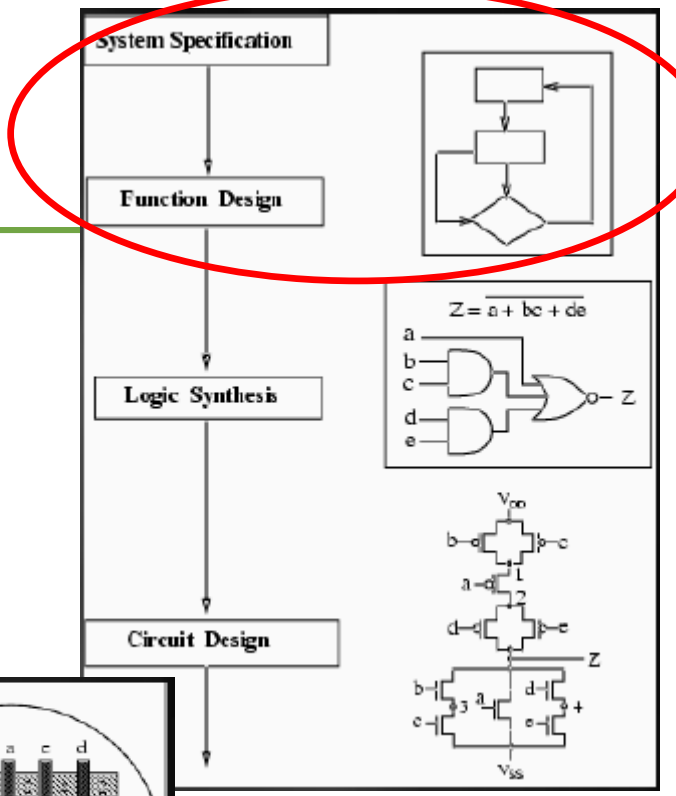
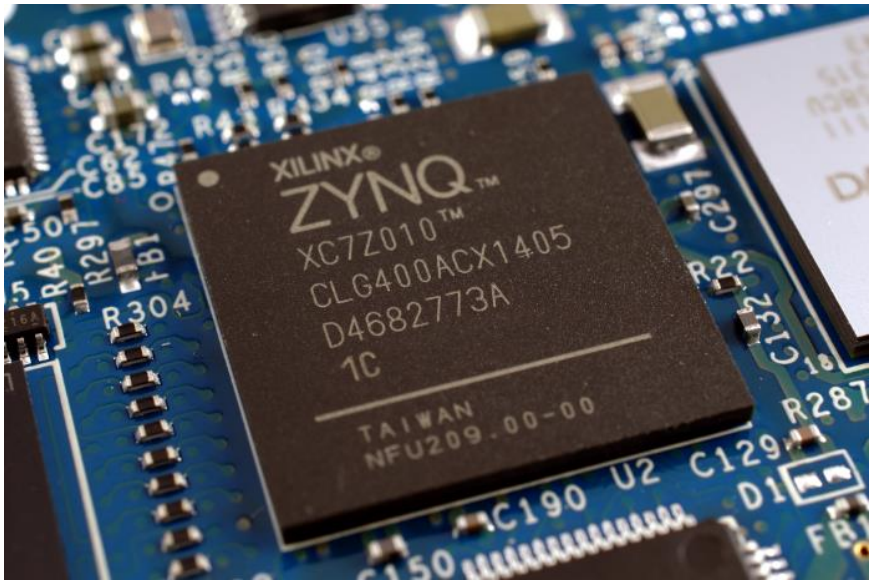
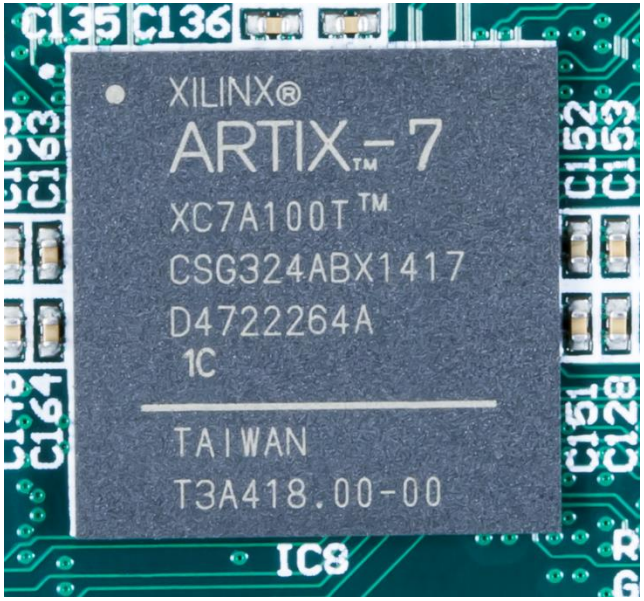




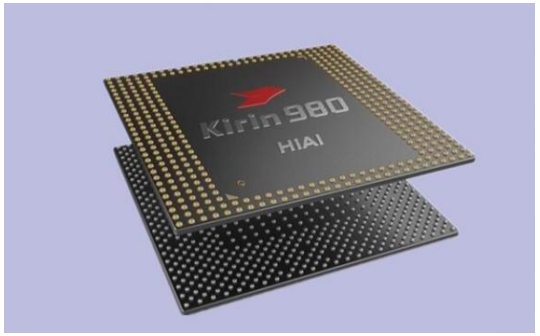
集成電路


intel
Stratix 10


XILINX
ZYNQ
XC7Z010
CLG400ACX1405
D4682773A
1C
TAIWAN
NFU209.00-00


XILINX
ARTIX-7
XC7A100T
CSG324ABX1417
D4722264A
1C
TAIWAN
T3A418.00-00
IC8


ALTERA
Stratix IV
EP4SGX230KF40C3ES
H AAAA80849A
KOREA


Kirin 980
HiAi

中央處理器 微架構

From Program to Instructions

Your Program

```
int a, b, c;
a = 3;
b = 4;
c = a + b;
```

translate

Assembly Code

ARM

```
mov r1, #3
mov r2, #4
add r3, r1,
r2
```

Intel

```
mov eax, 3
mov ebx, 4
add eax, ebx
mov ecx, eax
```

translate

Machine Instructions

ARM

```
03 10 a0 e3
04 20 a0 e3
02 30 81 e0
```

Intel

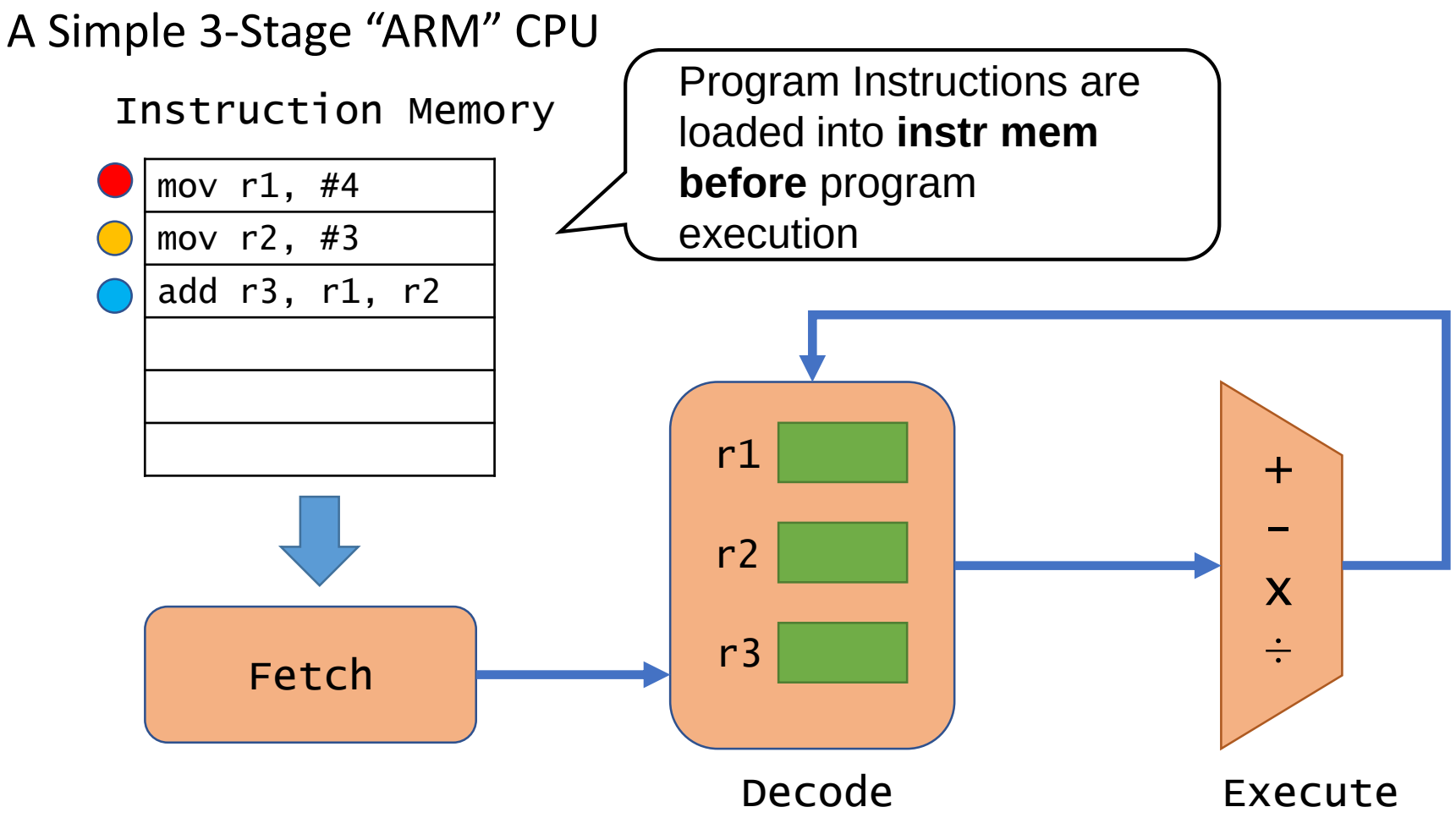
```
b8 03 00 00 00
bb 04 00 00 00
01 d8
89 c1
```

CPU can only understand **machine instructions** !!

Compilers do this job for you

Different CPU Microarchitecture
Different Set of Instructions

中央處理器是如何工作的？



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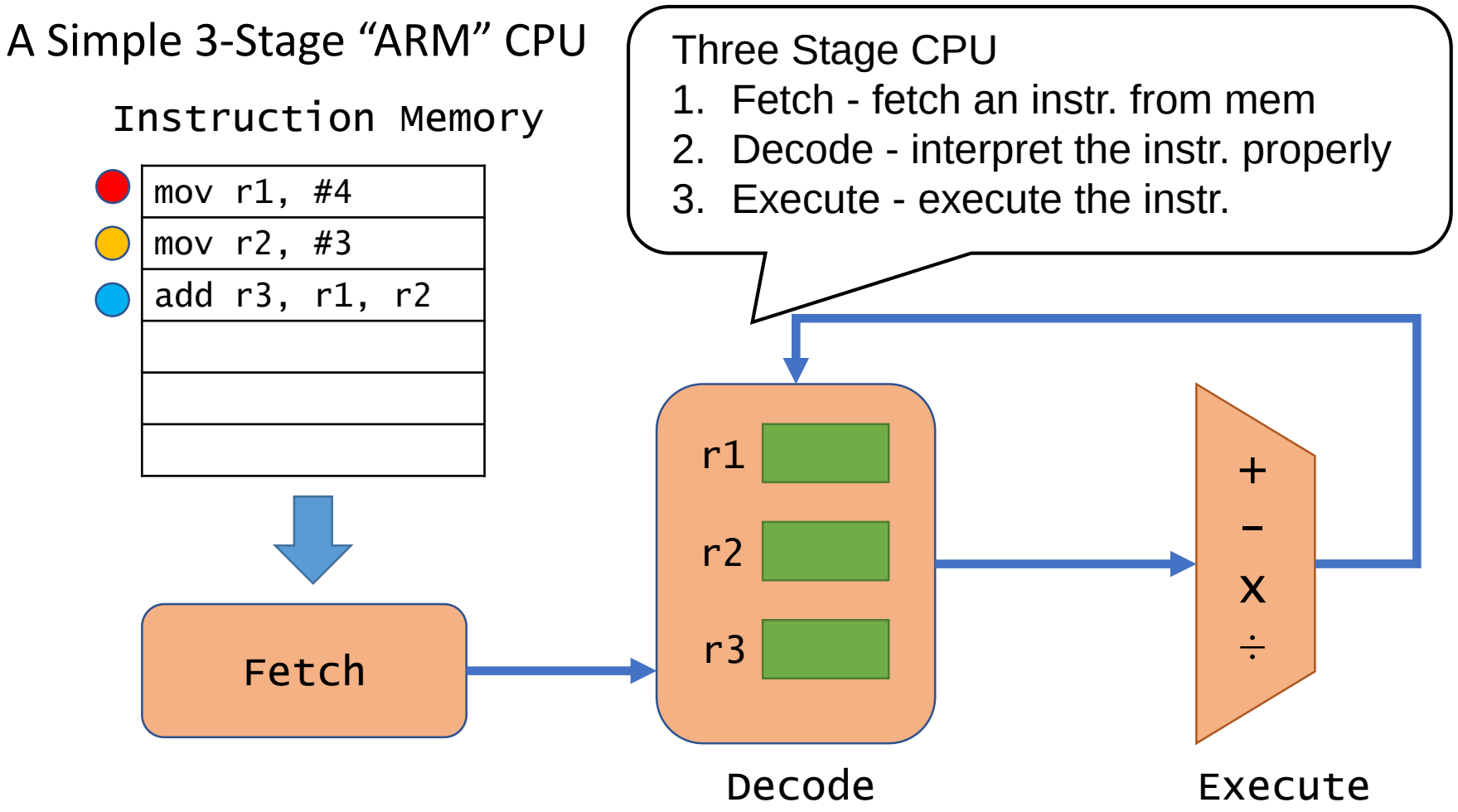
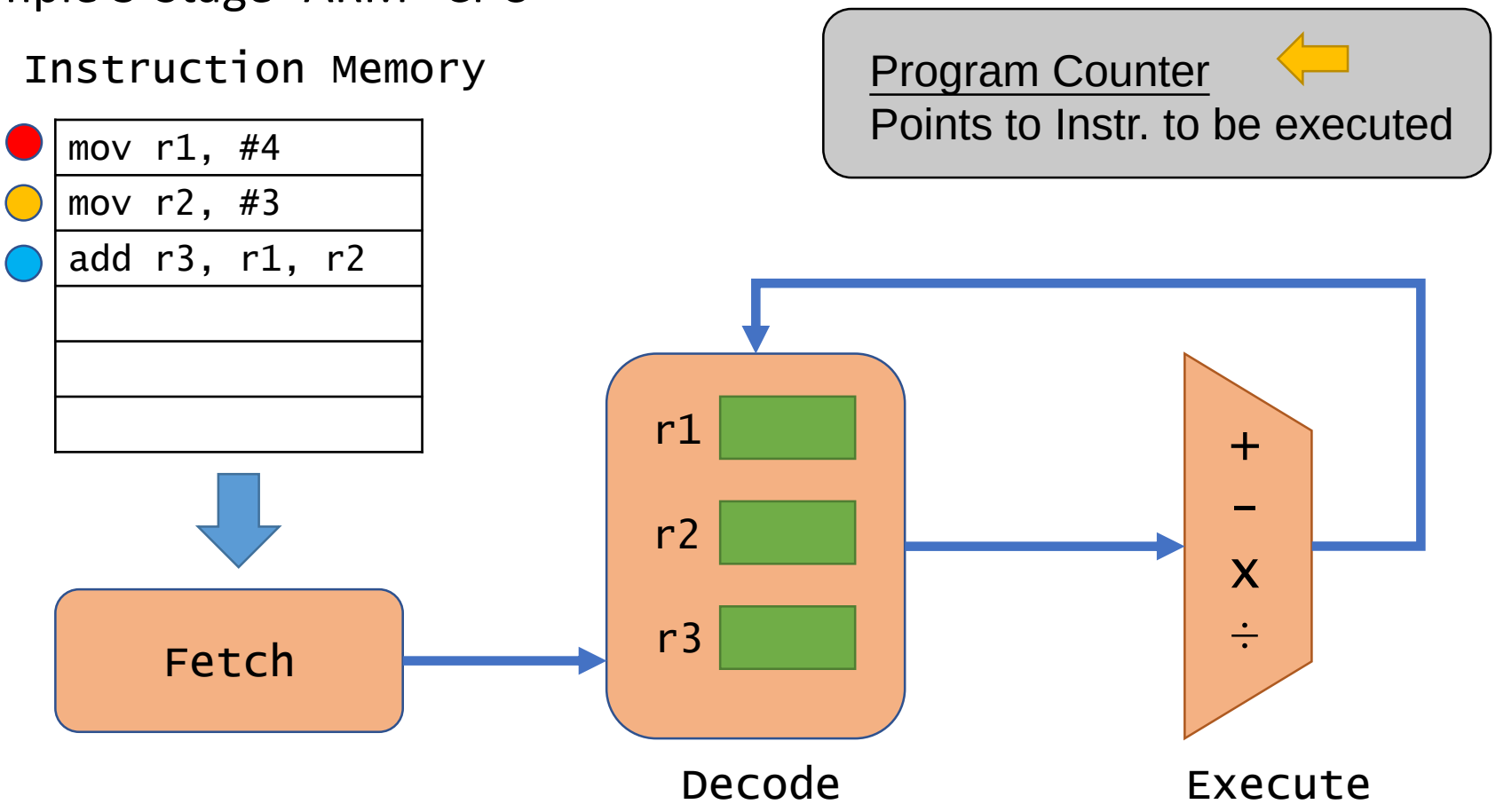


中央處理器是如何工作的？

A Simple 3-Stage “ARM” CPU



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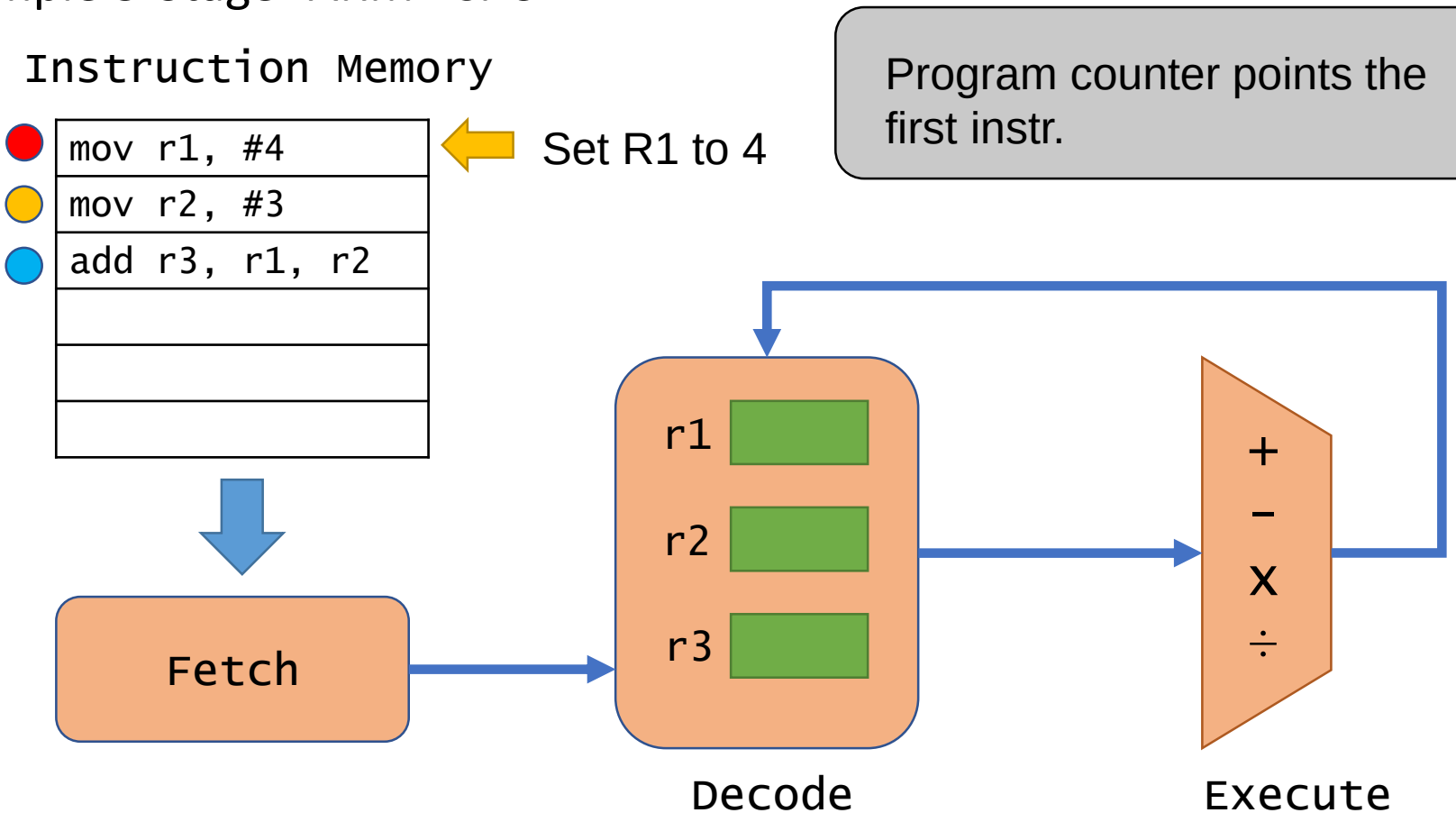

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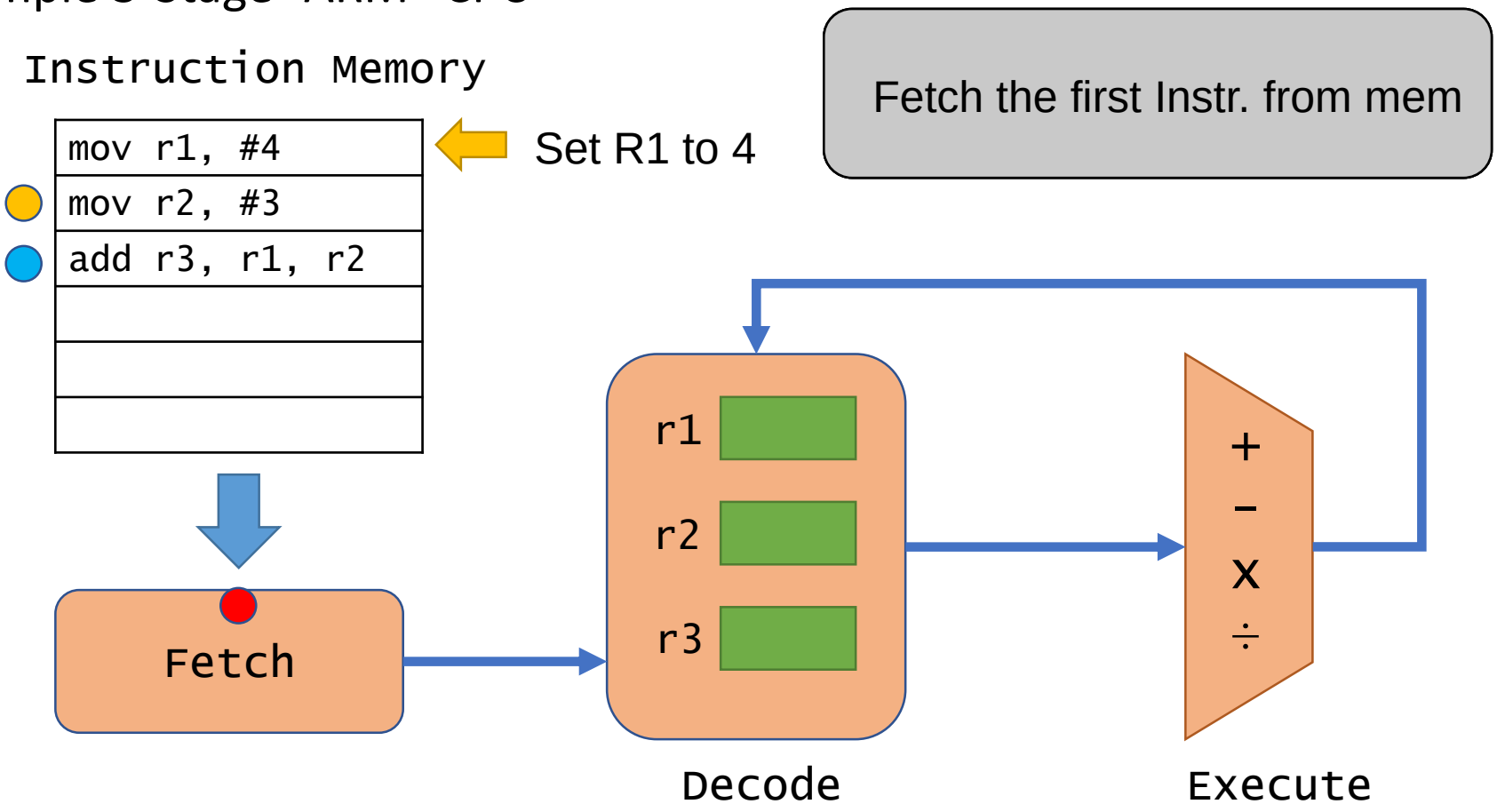

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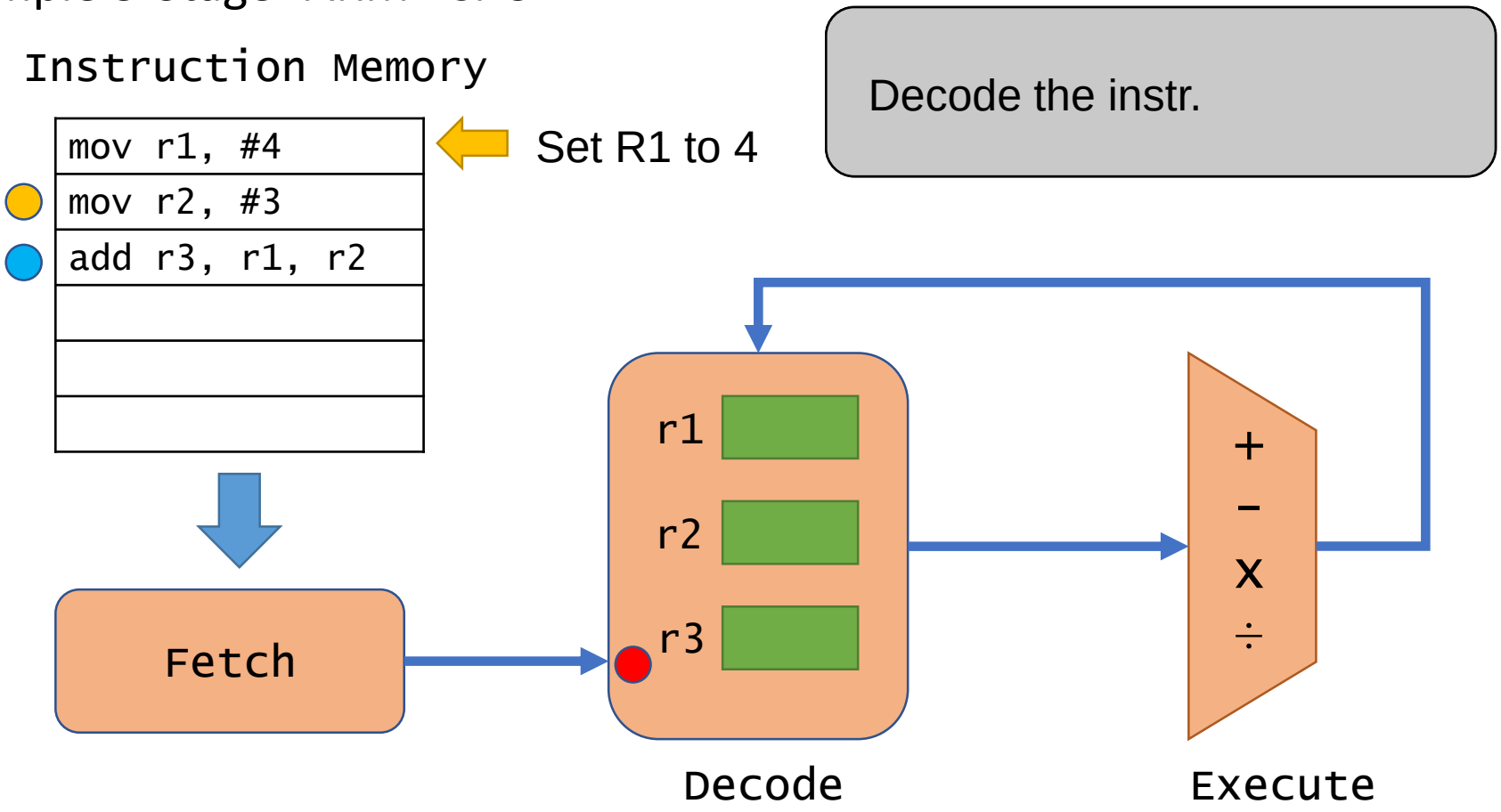

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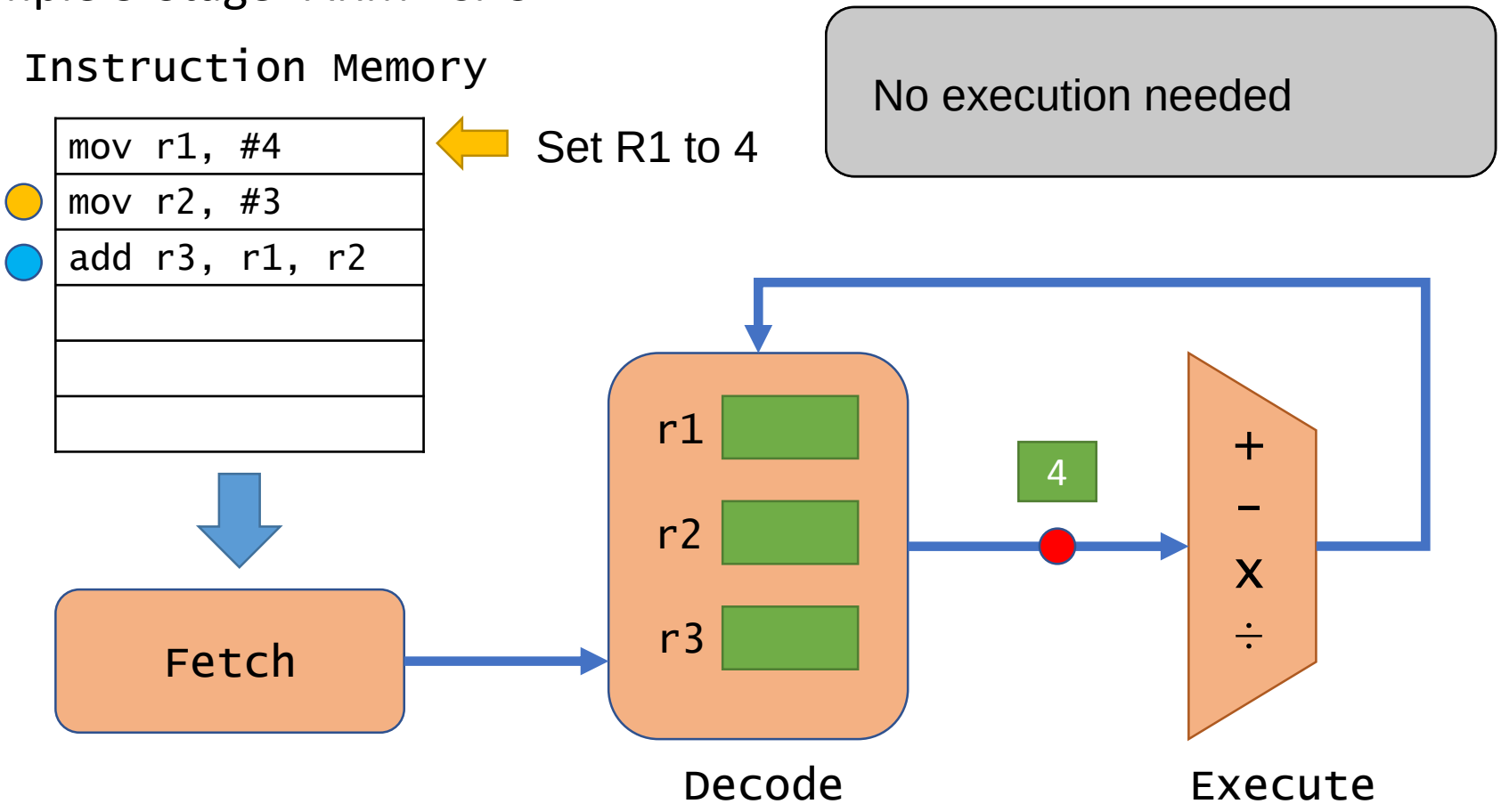

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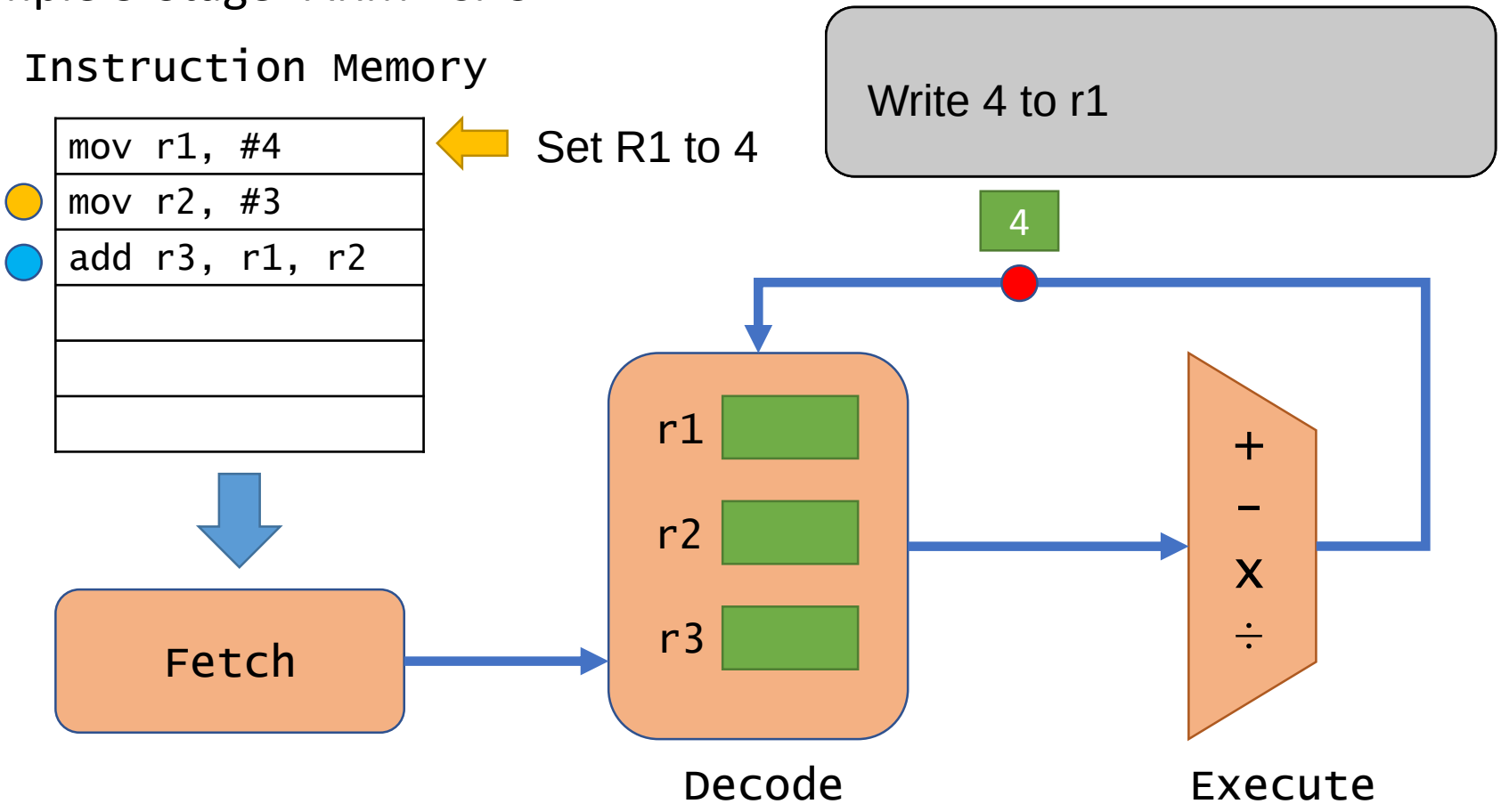

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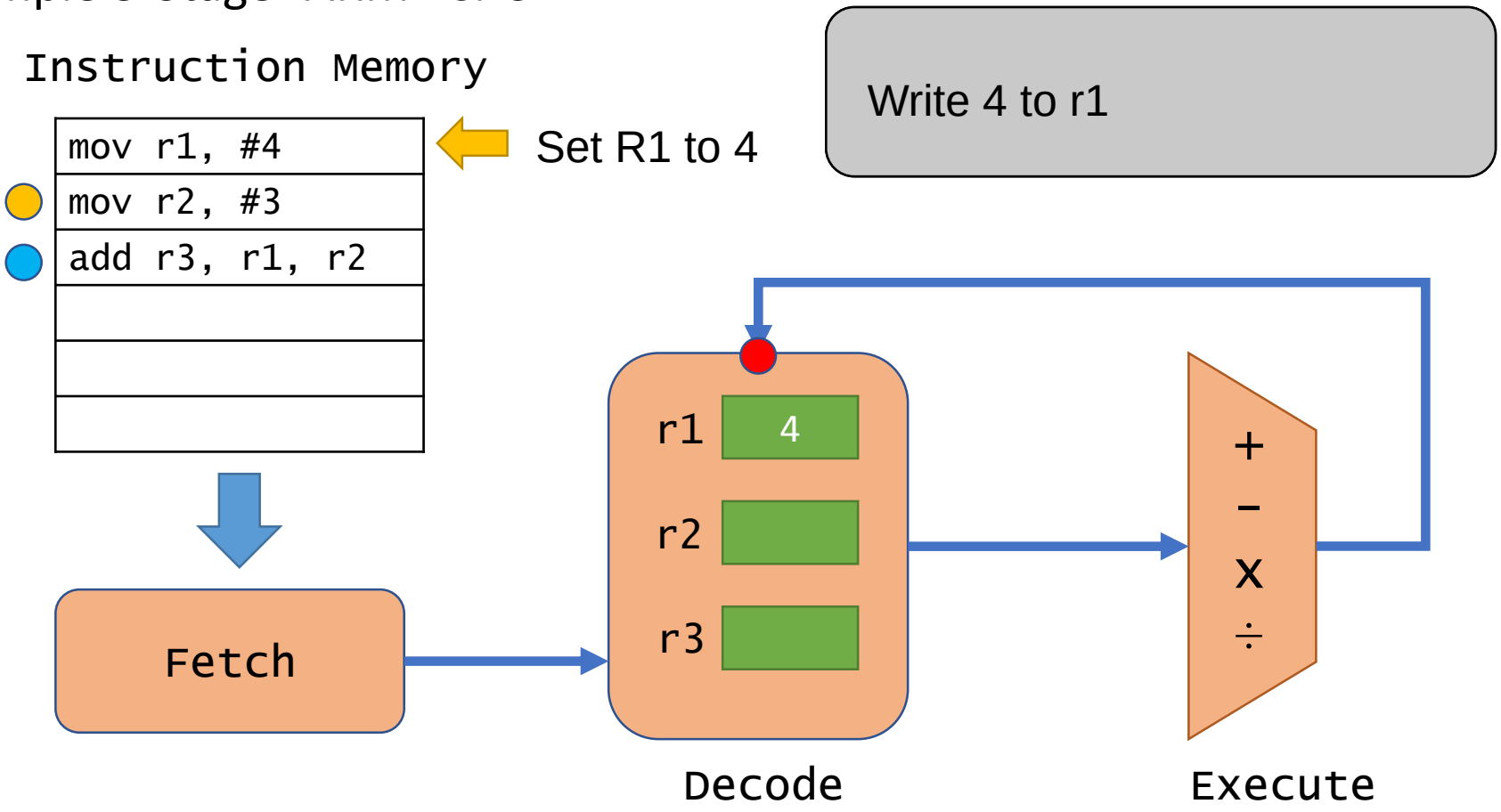

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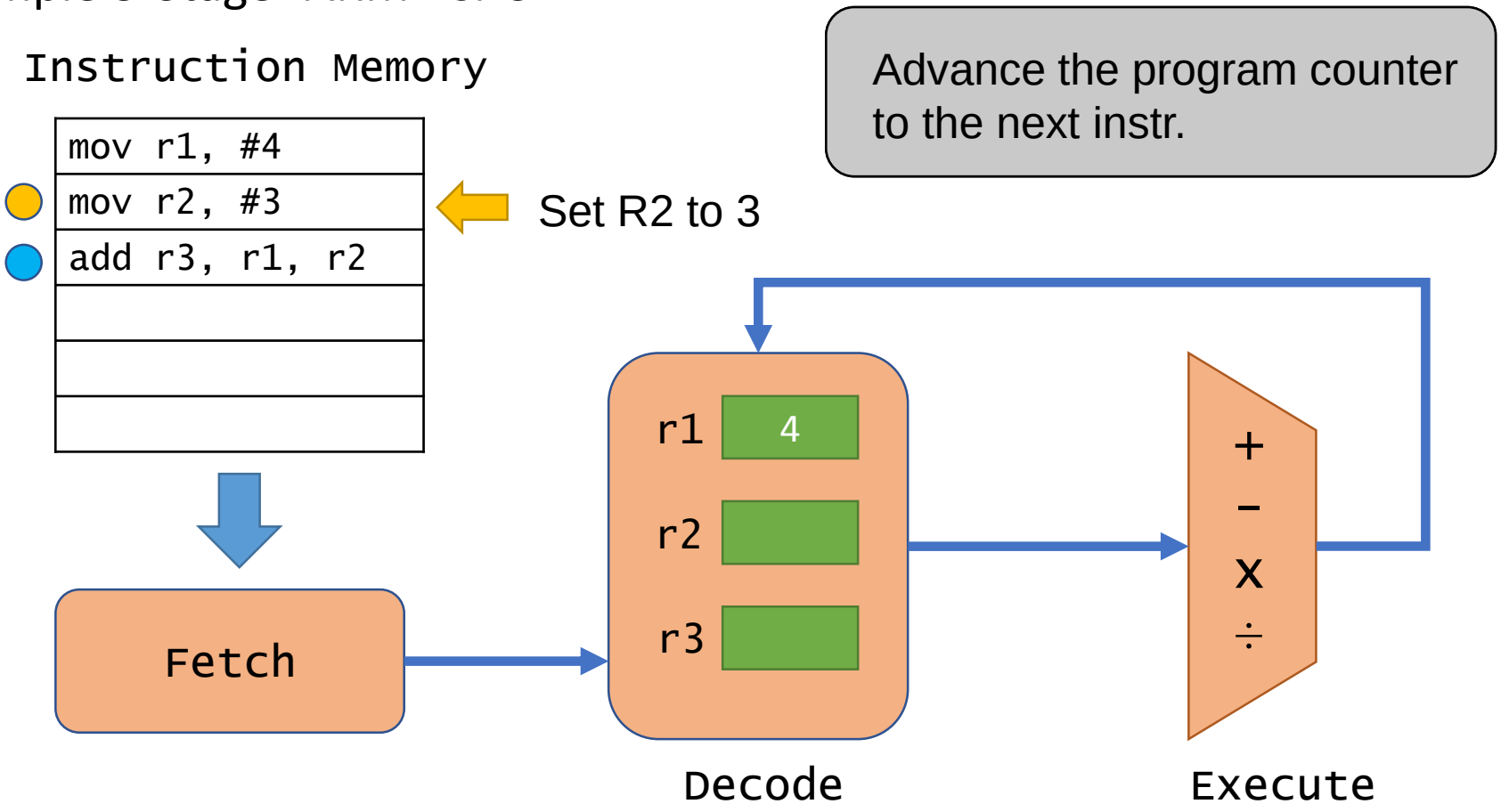

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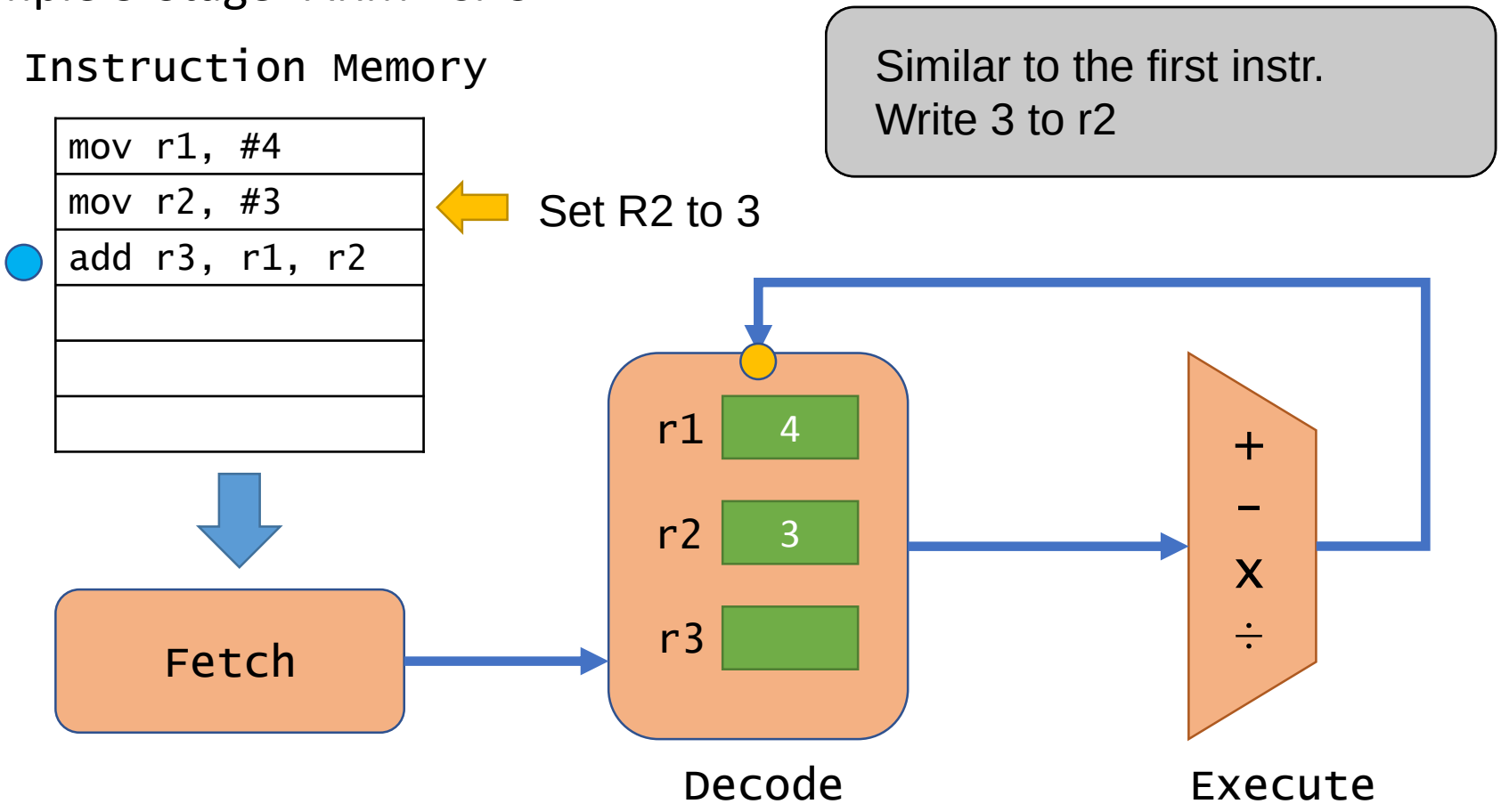

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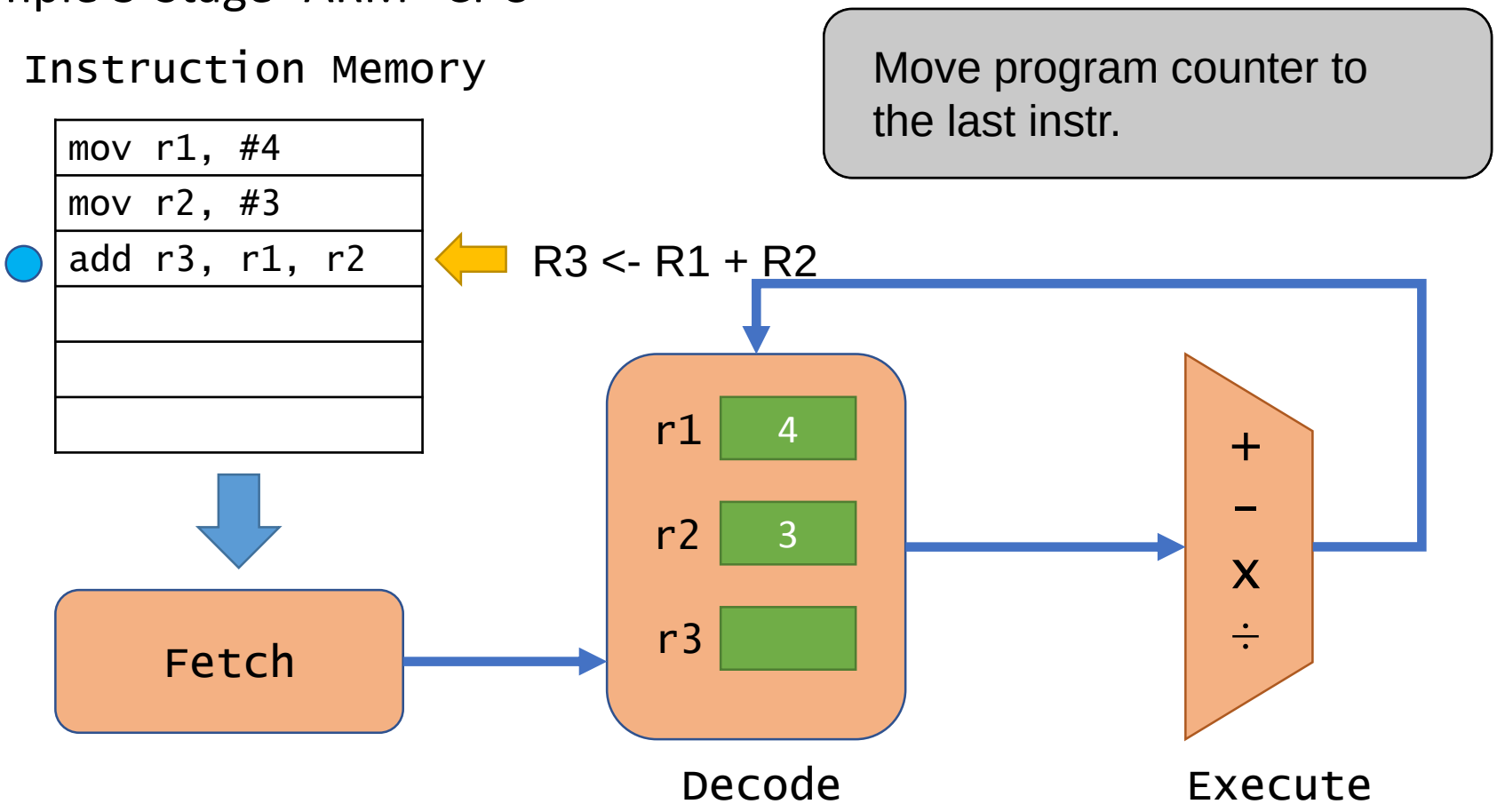

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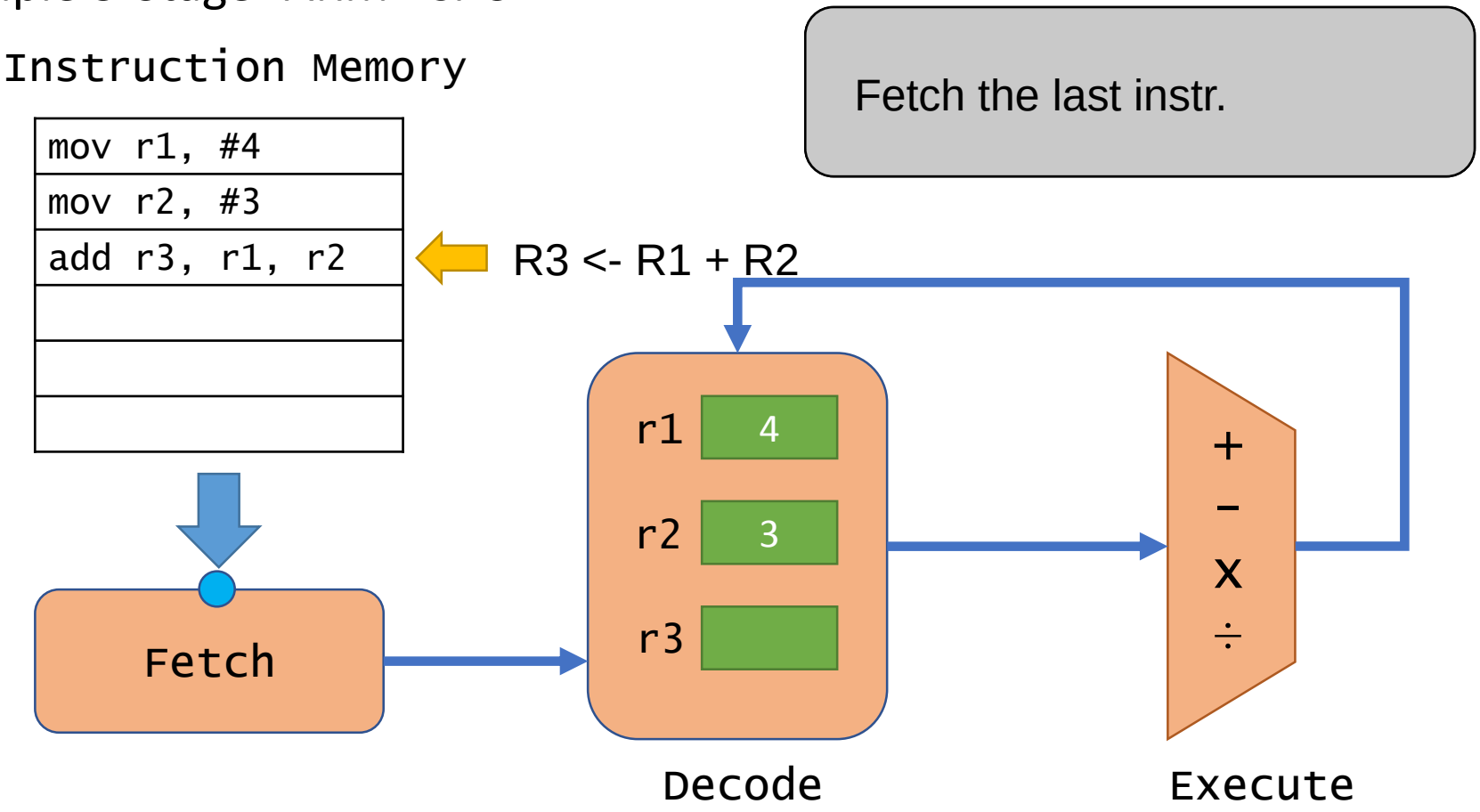

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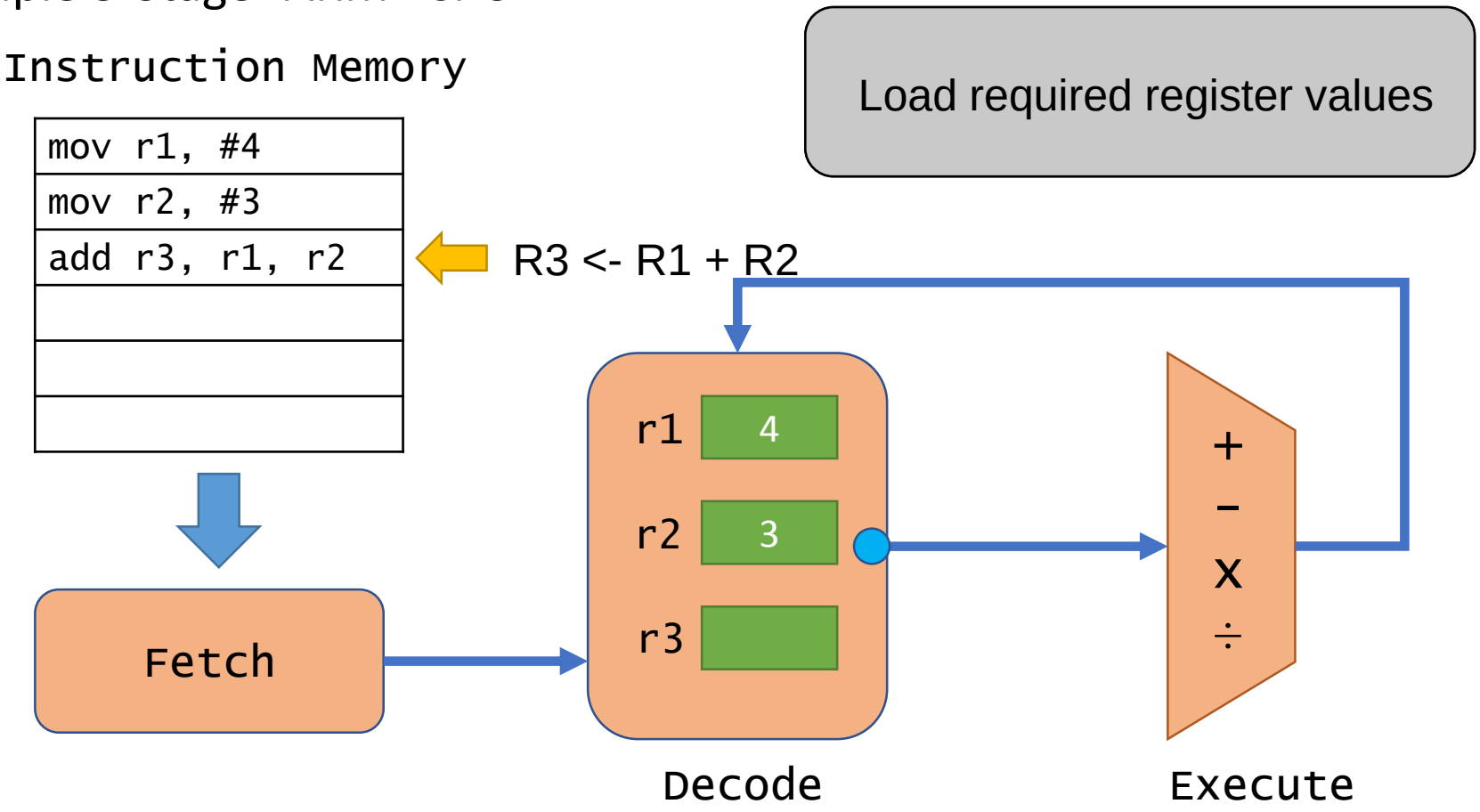

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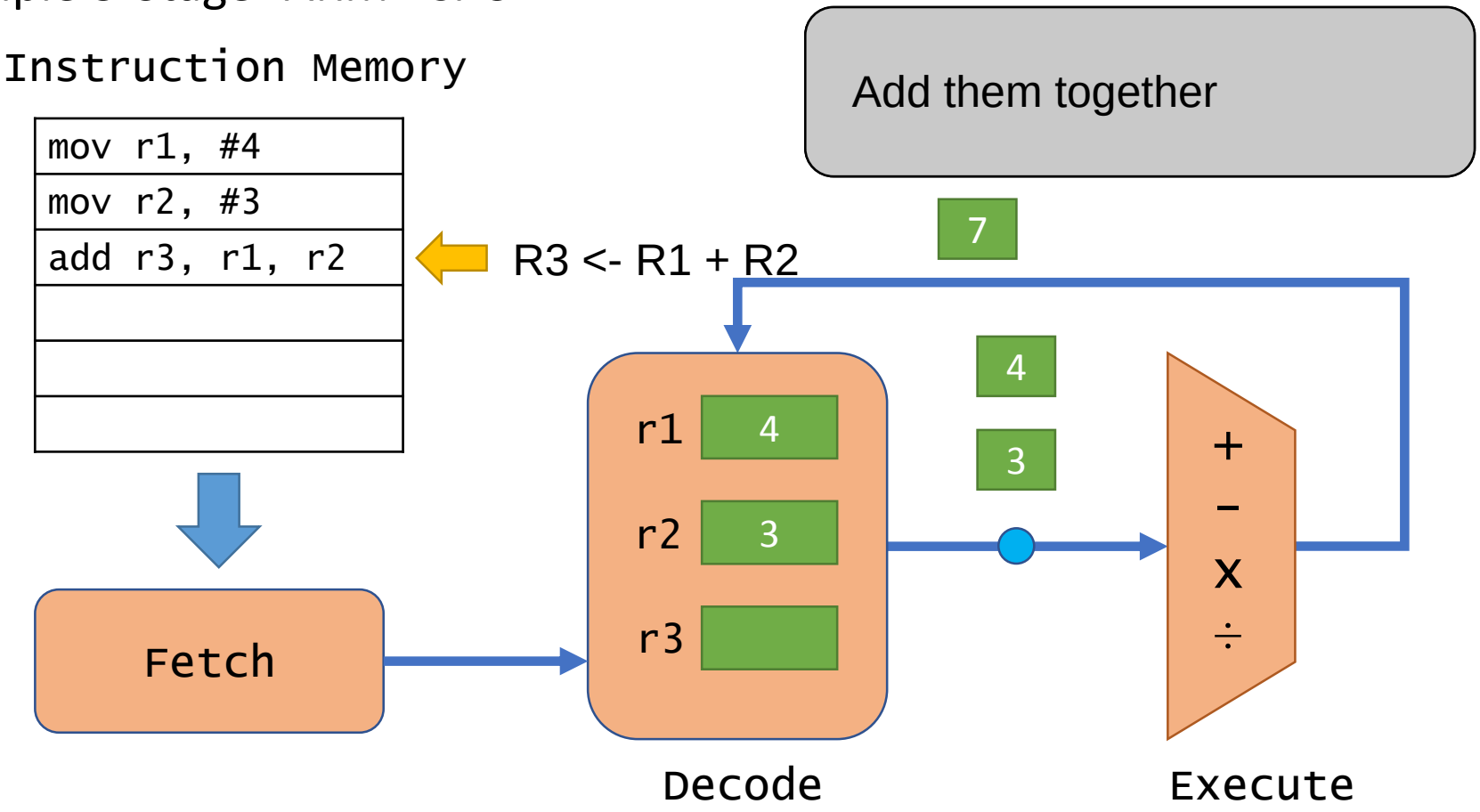

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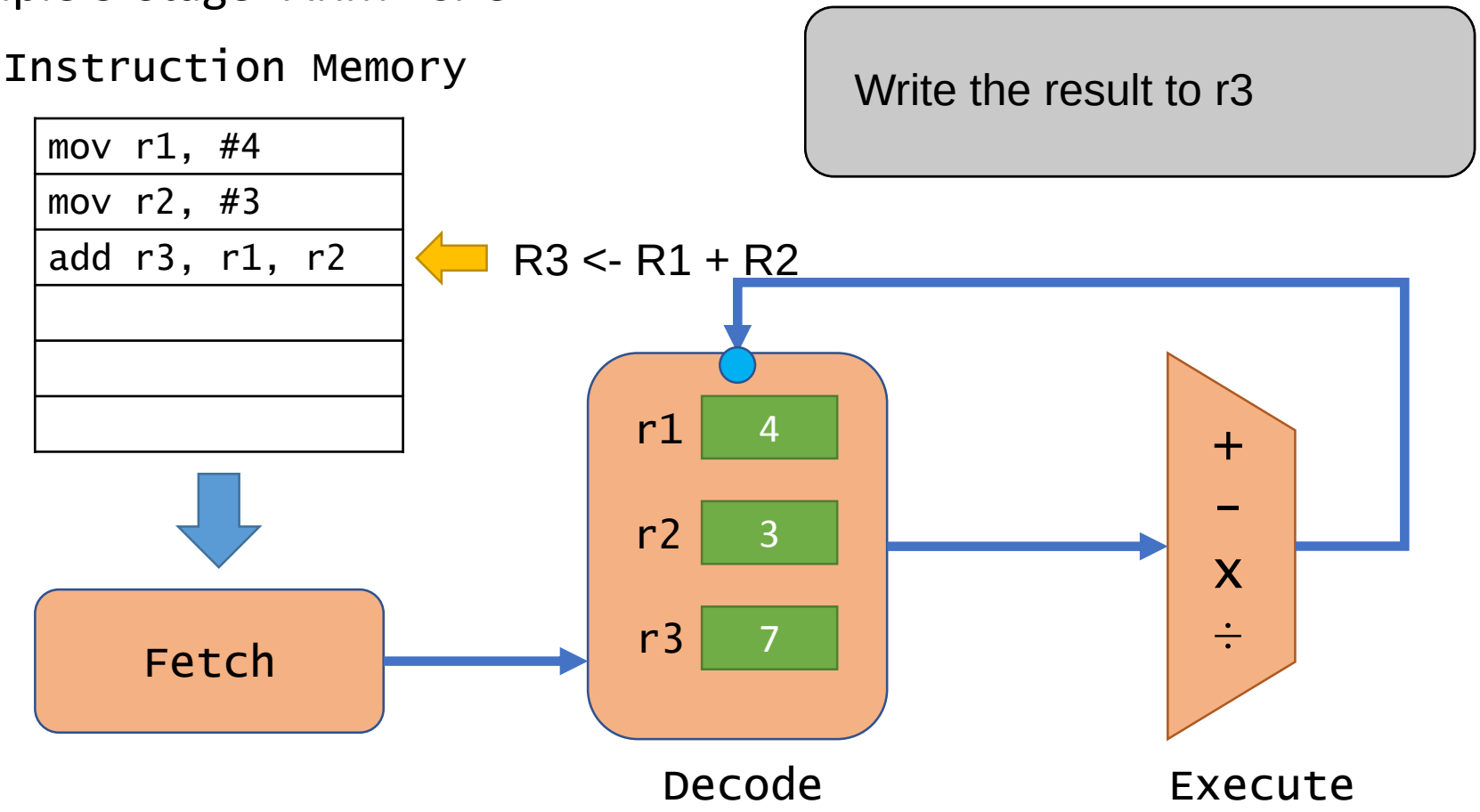
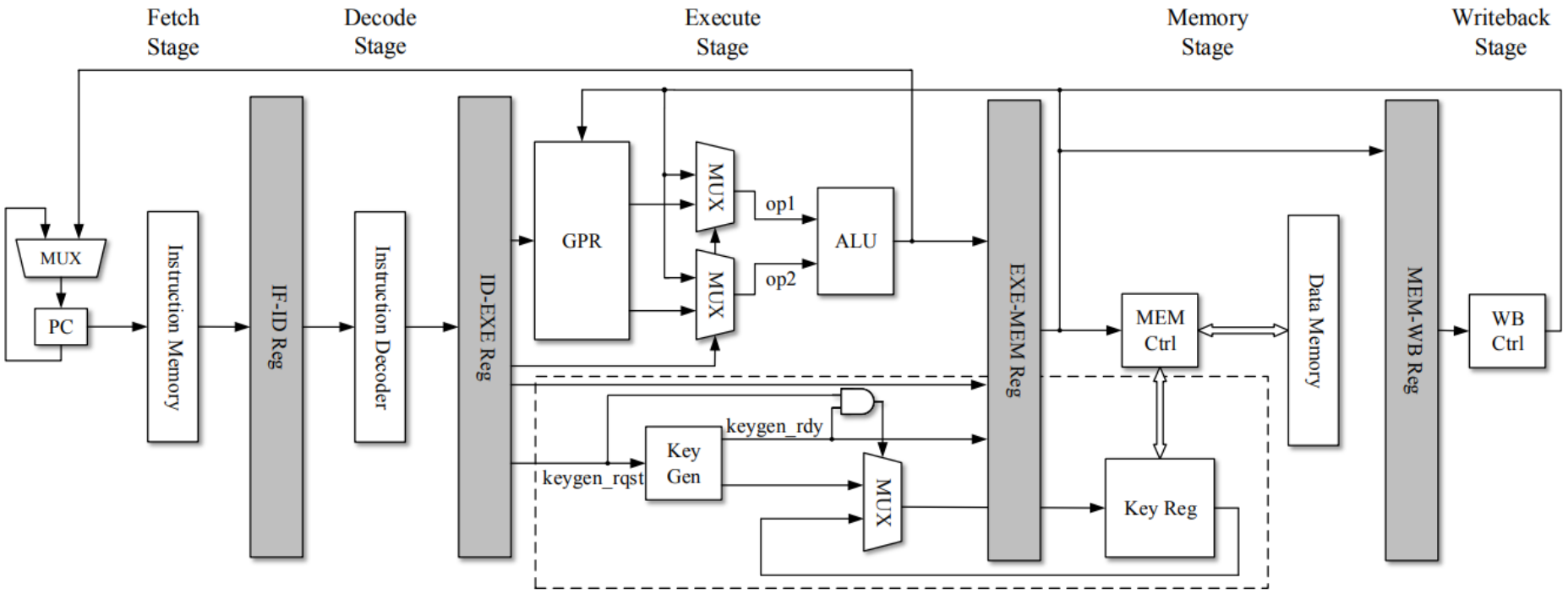


中央處理器 微架構

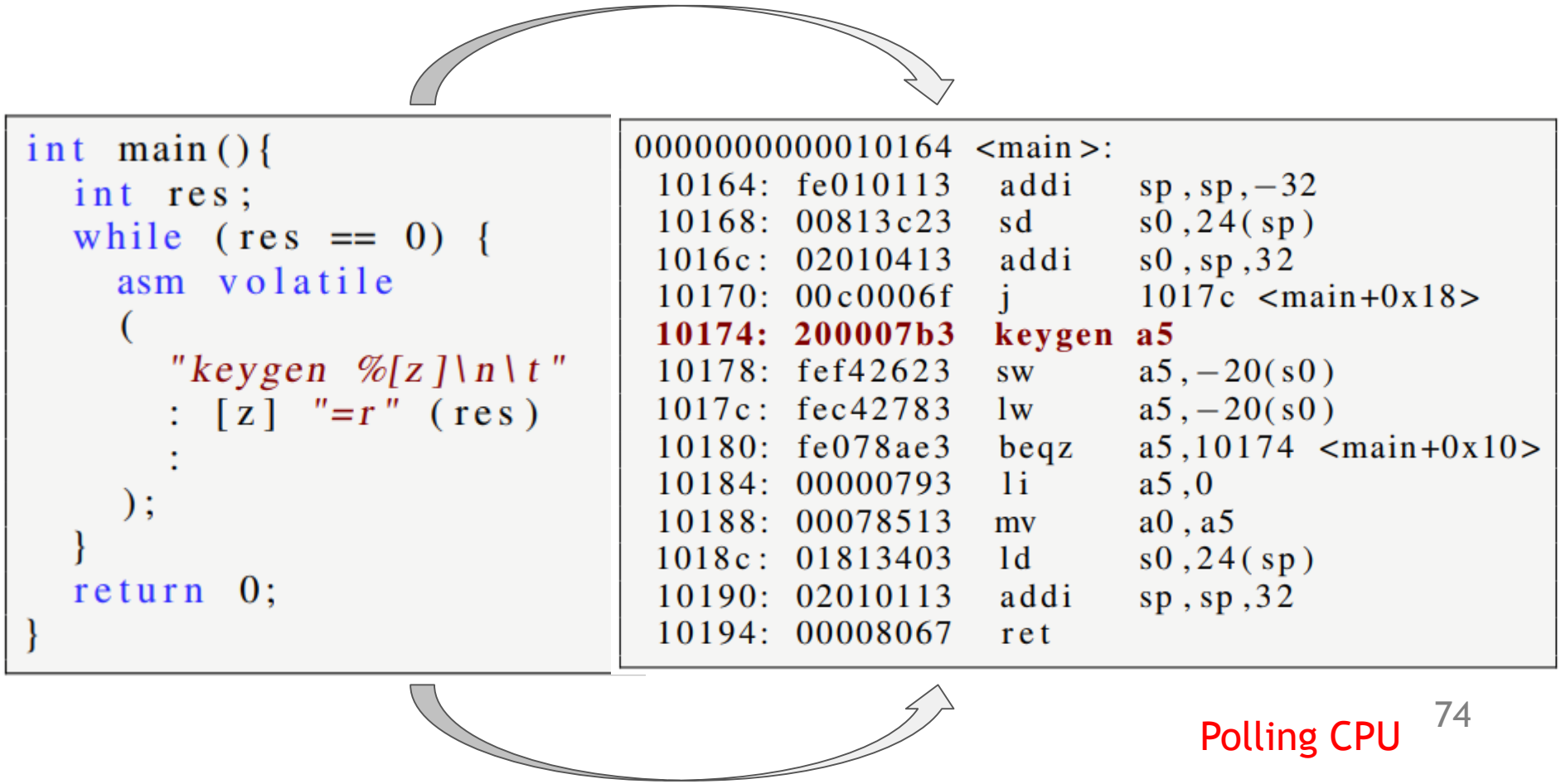
- Machine Code running on this architecture
- Compile a high-level language to machine code



Research work at CityU – Secure AIoT Microprocessor

高級語言 到 機器代碼

- Compiler will handle the translation for you.

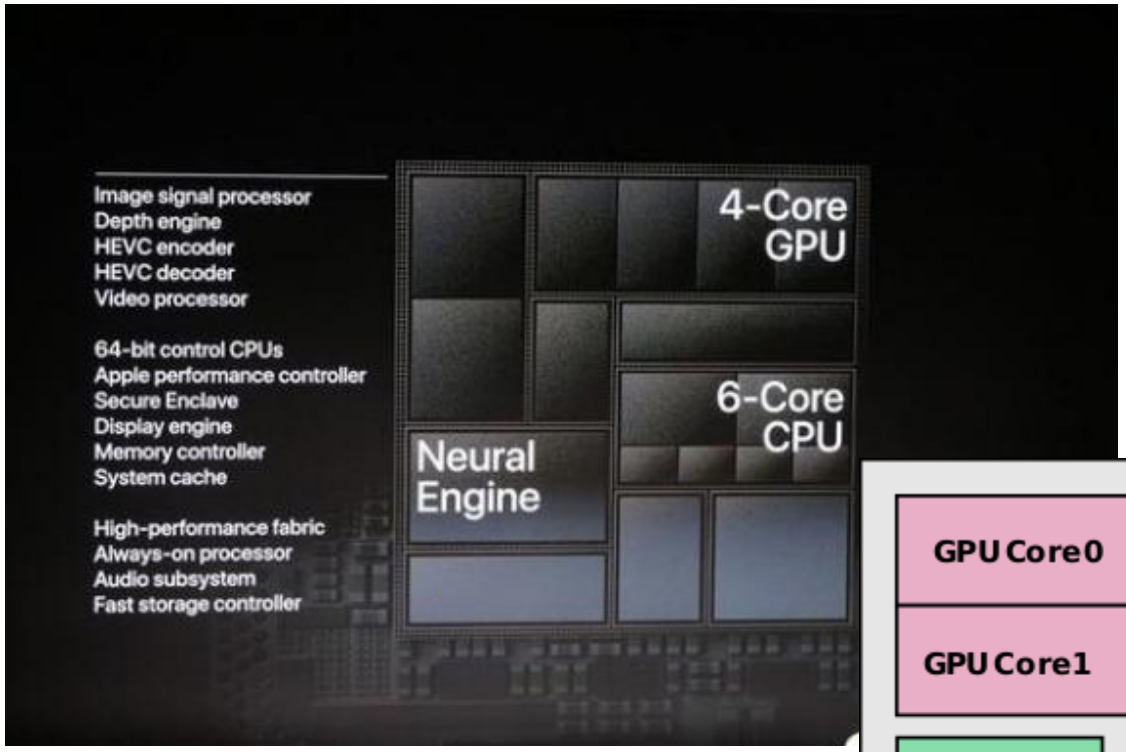


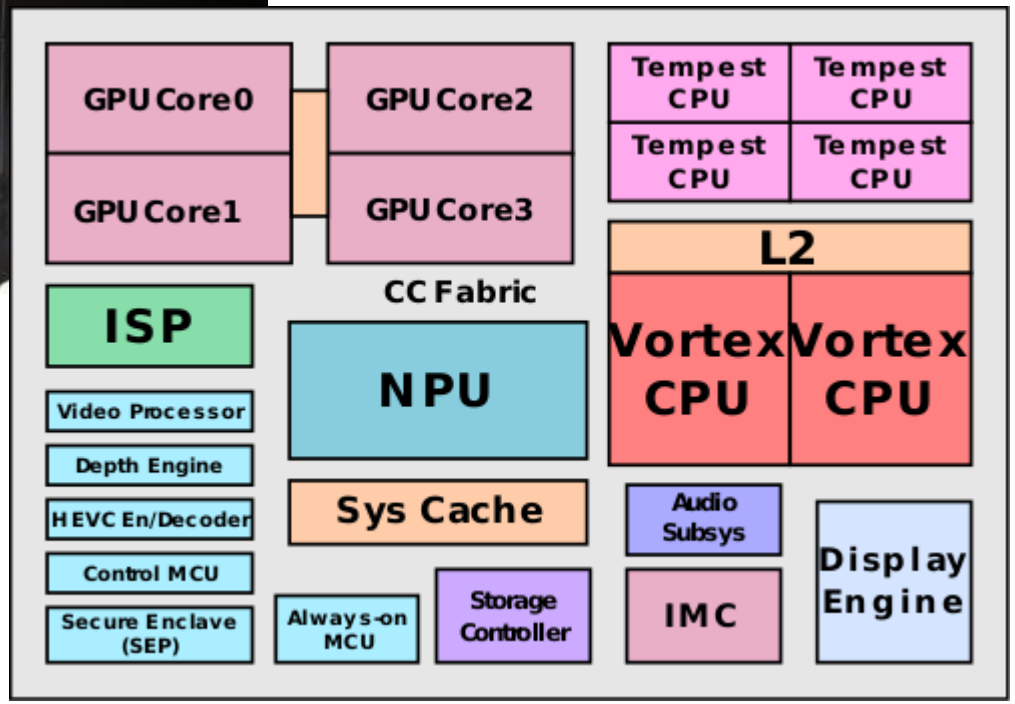
```
int main(){
  int res;
  while (res == 0) {
    asm volatile
    (
      "keygen %[z]\n\t"
      : [z] "=r" (res)
      :
    );
  }
  return 0;
}
```

```
0000000000010164 <main>:
 10164: fe010113   addi    sp,sp,-32
 10168: 00813c23   sd      s0,24(sp)
 1016c: 02010413   addi    s0,sp,32
 10170: 00c0006f   j       1017c <main+0x18>
 10174: 200007b3   keygen  a5
 10178: fef42623   sw      a5,-20(s0)
 1017c: fec42783   lw      a5,-20(s0)
 10180: fe078ae3   beqz    a5,10174 <main+0x10>
 10184: 00000793   li      a5,0
 10188: 00078513   mv      a0,a5
 1018c: 01813403   ld      s0,24(sp)
 10190: 02010113   addi    sp,sp,32
 10194: 00008067   ret
```

Polling CPU

Apple A12 - 7nm





華為和 Apple 核心處理器

Kirin 980

General Info

Designer	HiSilicon, ARM Holdings
Manufacturer	TSMC
Model Number	980
Market	Mobile
Introduction	August 31, 2018 (announced) August 31, 2018 (launched)

General Specs

Family	Kirin
Frequency	2,600 MHz, 1,920 MHz, 1,800 MHz

Microarchitecture

ISA	ARMv8 (ARM)
Microarchitecture	Cortex-A76, Cortex-A55
Core Name	Cortex-A76, Cortex-A55
Process	7 nm
Transistors	6,900,000,000
Technology	CMOS
Word Size	64 bit
Cores	8
Threads	8

A12 Bionic

General Info

Designer	Apple
Manufacturer	TSMC
Model Number	A12 Bionic
Part Number	APL1W81
Market	Mobile, Embedded
Introduction	September 12, 2018 (announced) September 21, 2018 (launched)

General Specs

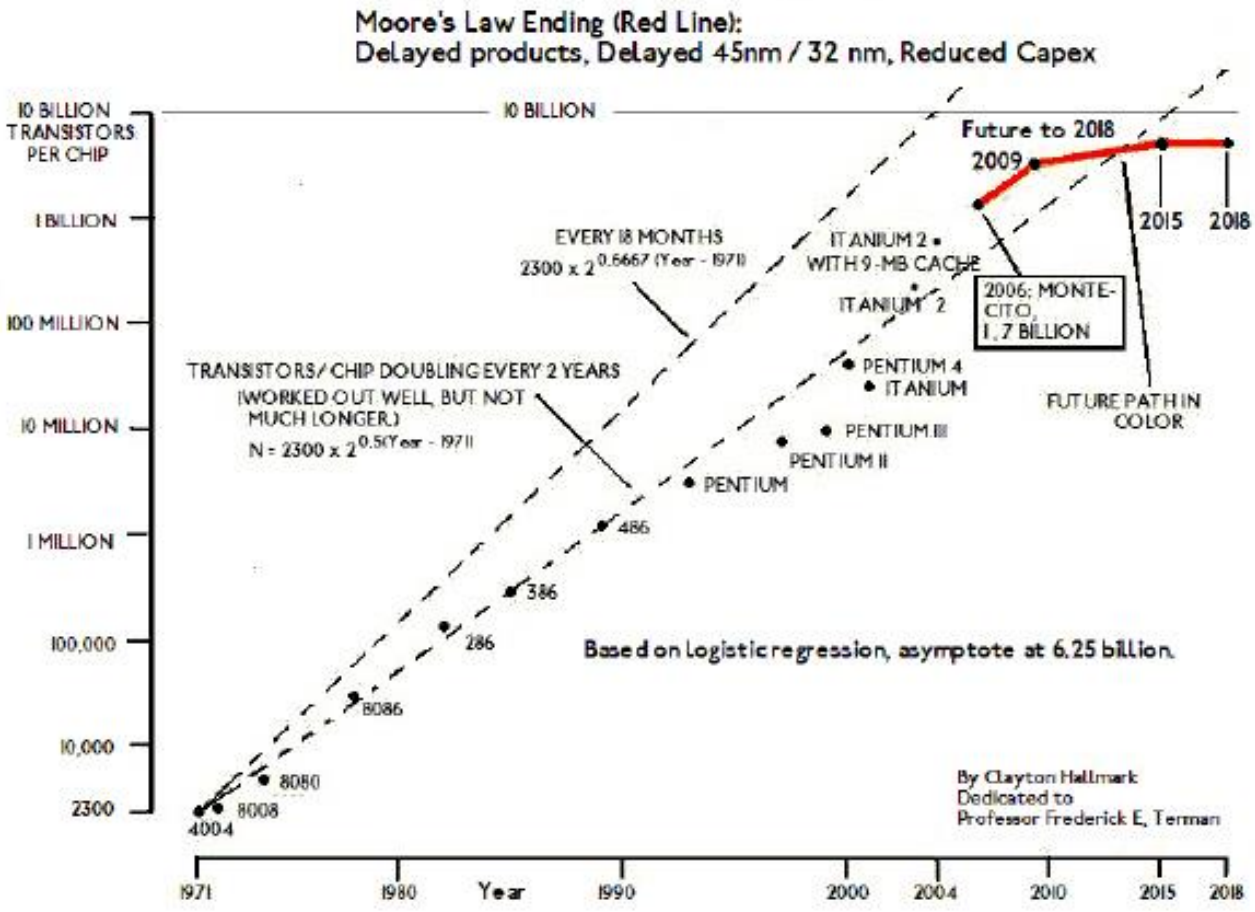
Family	Ax
Frequency	2,400 MHz

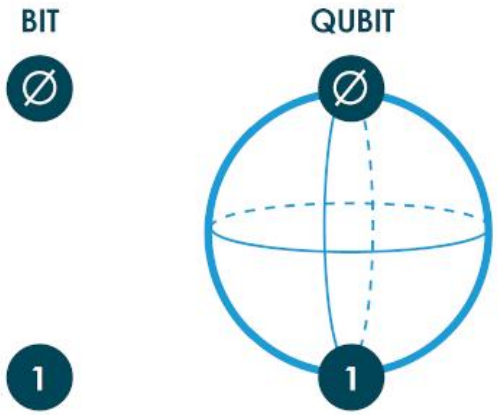
Microarchitecture

ISA	ARMv8.3 (ARM)
Microarchitecture	Vortex, Tempest
Core Name	Vortex, Tempest
Process	7 nm
Transistors	6,900,000,000
Technology	CMOS
Die	83.27 mm² 9.89 mm × 8.42 mm
Word Size	64 bit
Cores	6
Threads	6

芯片的未来

- Moore’s law – transistor size doubled every 2 years

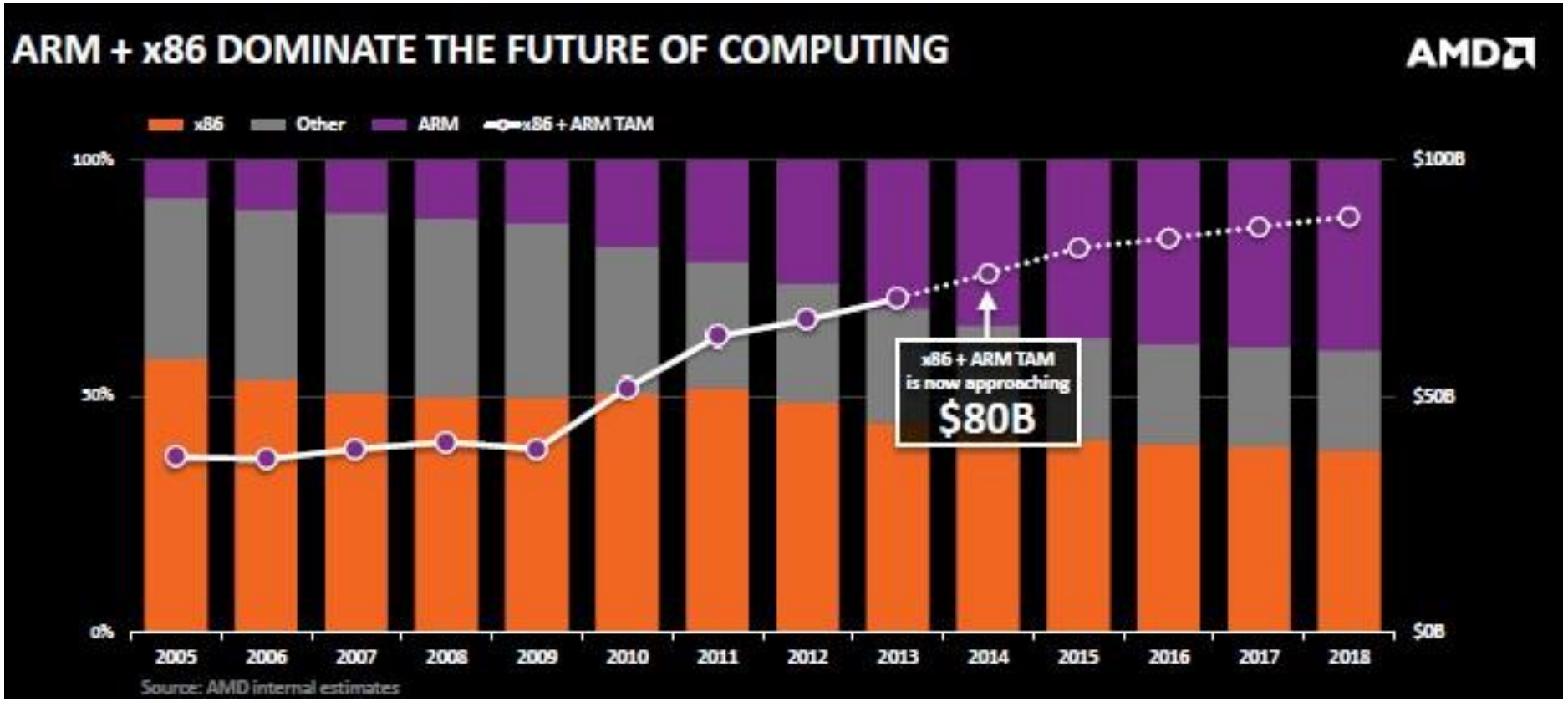




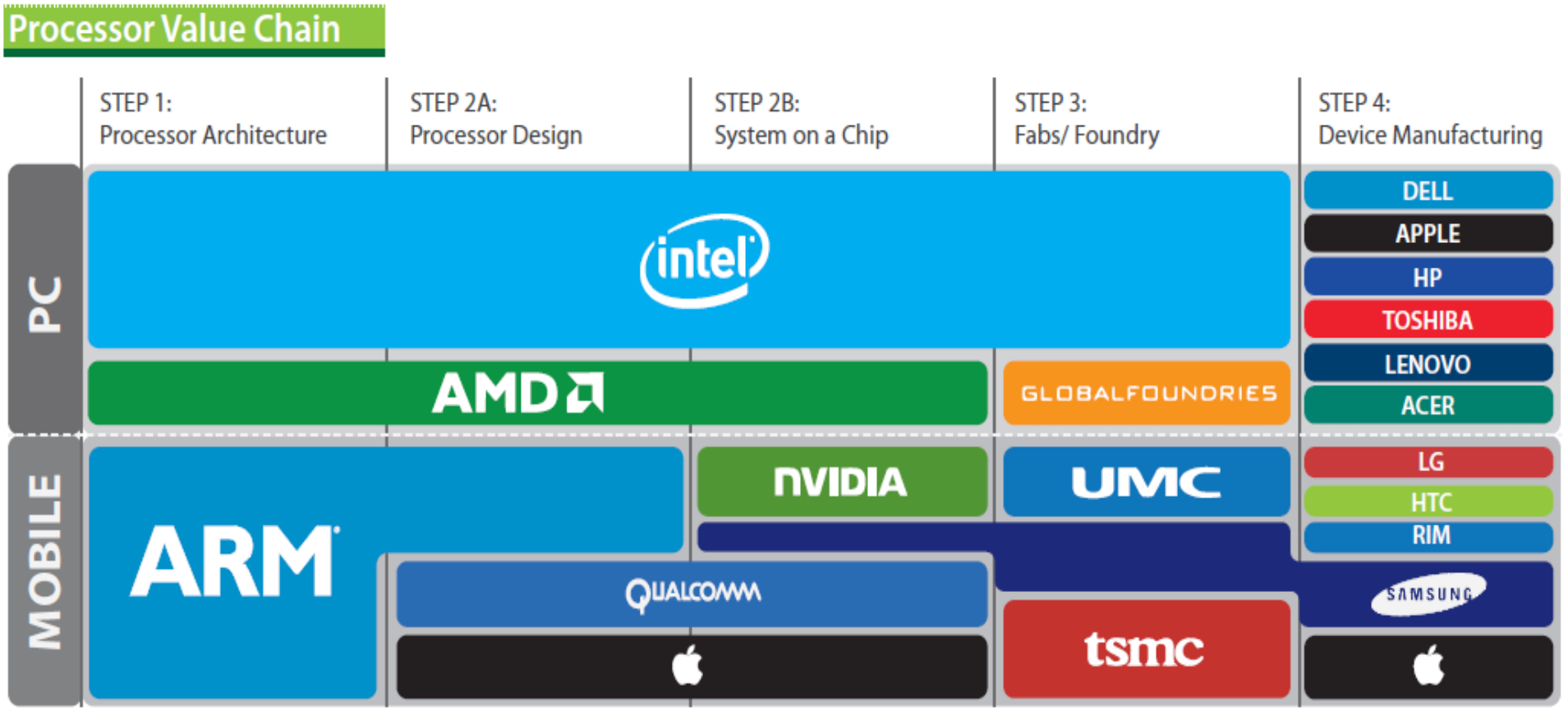
Quantum Computing

x86 vs. ARM

- Mobile computing market is continuously growing.

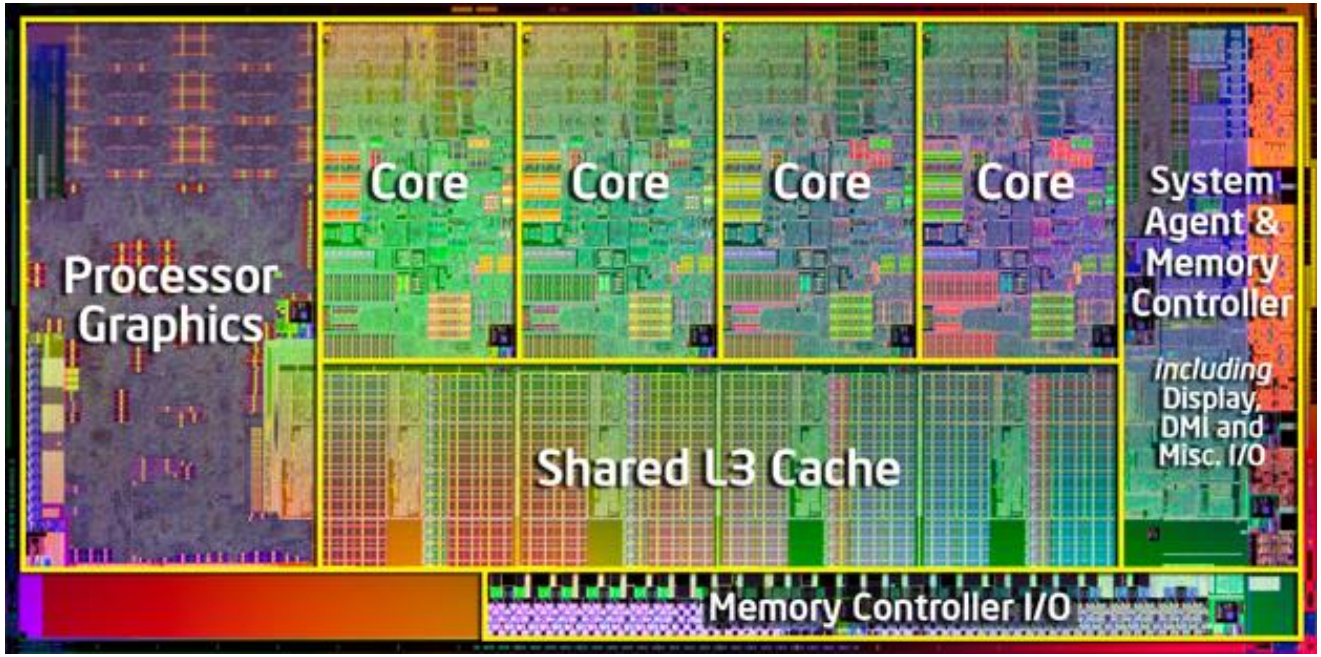


移動電腦市場 與 個人電腦市場



物理知識製作芯片

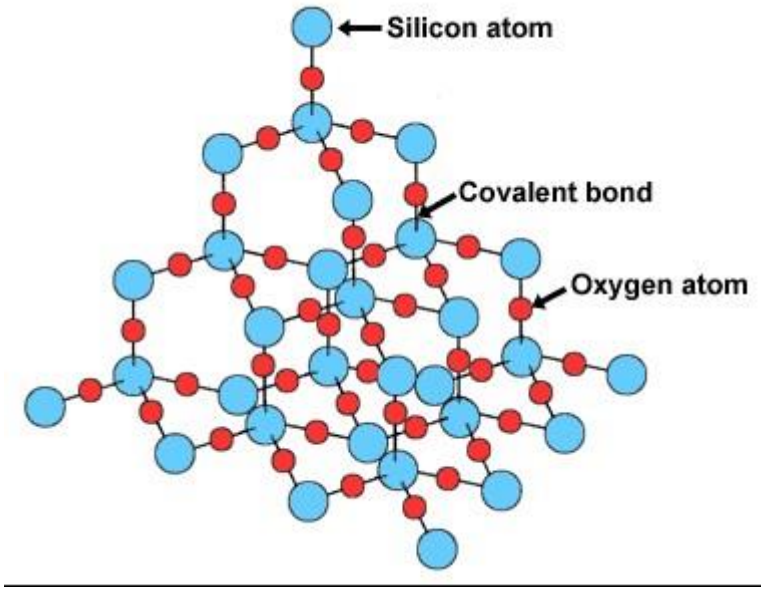
- Circuit design
  - Current, Voltage, Power, Resistance, Capacitance … (P = VI, $P=I^2R$ …)



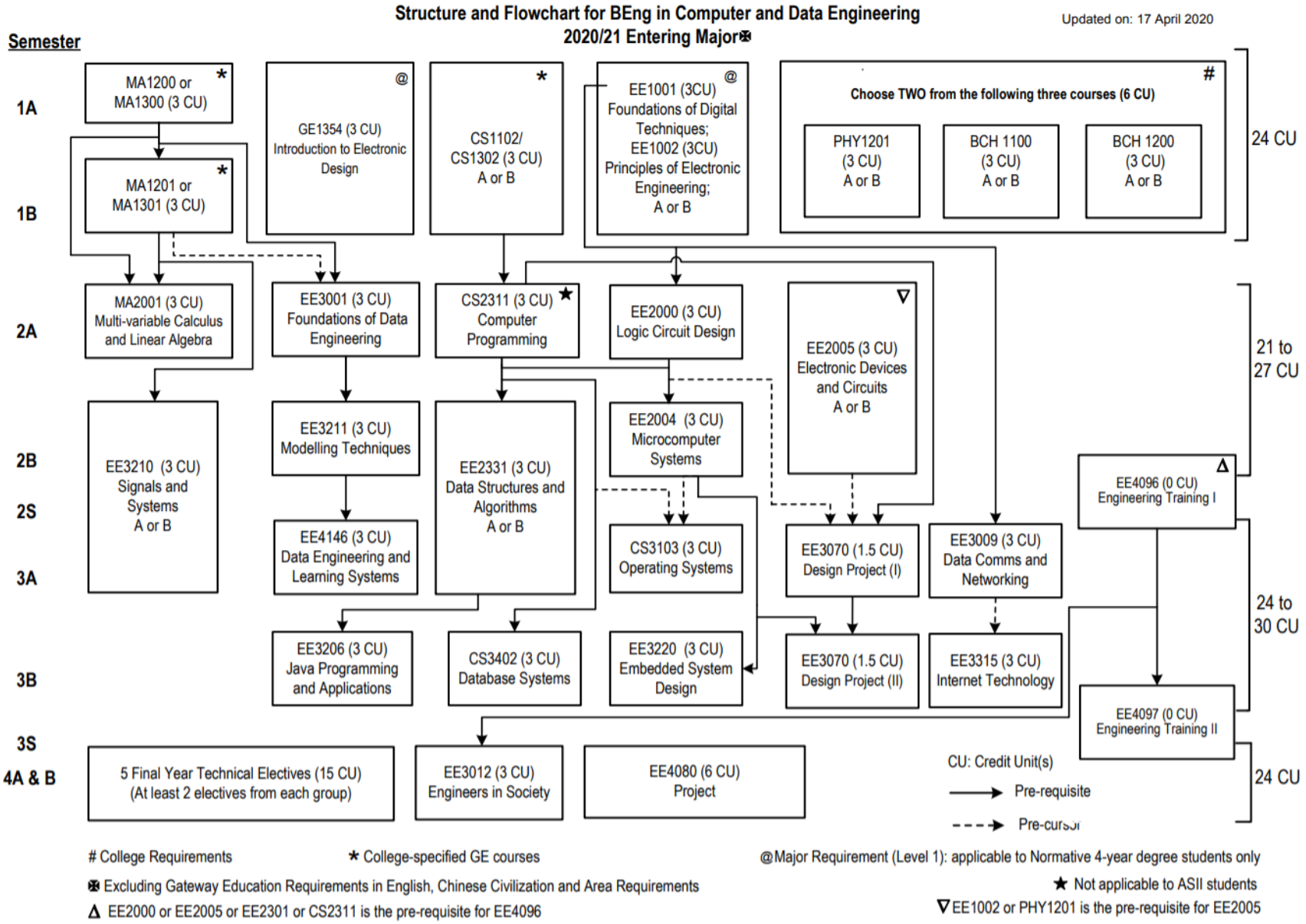
Layout Intel i7 CPU

化學知識製作芯片

- Silicon compounds (Silicon Oxide …)
- Find new materials to replace silicon ?
  - Smaller
  - Faster
  - Less power



工程科 大學教育


Structure and Flowchart for BEng in Computer and Data Engineering
2020/21 Entering Major✠
Updated on: 17 April 2020
Semester
1A
1B
2A
2B
2S
3A
3B
3S
4A & B
MA1200 or MA1300 (3 CU) *
MA1201 or MA1301 (3 CU) *
GE1354 (3 CU) Introduction to Electronic Design @
CS1102/ CS1302 (3 CU) A or B *
EE1001 (3CU) Foundations of Digital Techniques; EE1002 (3CU) Principles of Electronic Engineering; A or B @
Choose TWO from the following three courses (6 CU) #
PHY1201 (3 CU) A or B
BCH 1100 (3 CU) A or B
BCH 1200 (3 CU) A or B
24 CU
MA2001 (3 CU) Multi-variable Calculus and Linear Algebra
EE3001 (3 CU) Foundations of Data Engineering
CS2311 (3 CU) Computer Programming ★
EE2000 (3 CU) Logic Circuit Design
EE2005 (3 CU) Electronic Devices and Circuits A or B ∇
21 to 27 CU
EE3210 (3 CU) Signals and Systems A or B
EE3211 (3 CU) Modelling Techniques
EE2331 (3 CU) Data Structures and Algorithms A or B
EE2004 (3 CU) Microcomputer Systems
EE4096 (0 CU) Engineering Training I Δ
EE4146 (3 CU) Data Engineering and Learning Systems
CS3103 (3 CU) Operating Systems
EE3070 (1.5 CU) Design Project (I)
EE3009 (3 CU) Data Comms and Networking
24 to 30 CU
EE3206 (3 CU) Java Programming and Applications
CS3402 (3 CU) Database Systems
EE3220 (3 CU) Embedded System Design
EE3070 (1.5 CU) Design Project (II)
EE3315 (3 CU) Internet Technology
EE4097 (0 CU) Engineering Training II
5 Final Year Technical Electives (15 CU) (At least 2 electives from each group)
EE3012 (3 CU) Engineers in Society
EE4080 (6 CU) Project
24 CU
CU: Credit Unit(s)
Pre-requisite
Pre-cursor
College Requirements
* College-specified GE courses
@Major Requirement (Level 1): applicable to Normative 4-year degree students only
✠ Excluding Gateway Education Requirements in English, Chinese Civilization and Area Requirements
★ Not applicable to ASII students
Δ EE2000 or EE2005 or EE2301 or CS2311 is the pre-requisite for EE4096
∇EE1002 or PHY1201 is the pre-requisite for EE2005

HKSTP – Microelectronics Center

推動香港微電子 科技園公司辦FPGA電子開發加速器

星島日報

港聞 財經 地產 娛樂 中國 國際

【預算案】科技園將加建實驗室 改建元朗工業邨舊廠房為「微電子中心」

2020-02-26 18:32

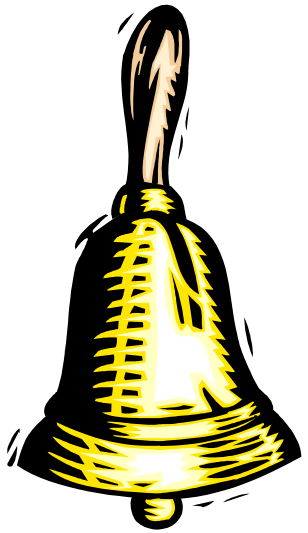
科技園。資料圖片

財政司司長陳茂波今日發布新一年度財政預算案，香港科技園公司表示歡迎，亦感謝政府增撥資源，持續支持香港的創科發展。

科技園公司表示，政府宣布的預留30億元，以推動科學園第二階段擴建計劃。科技園公司已委託顧問進行總體規劃研究探討發展方案，以加強香港的創科基建，推動創科生態圈的持續發展。根據科技園公司的初步建議，第二階段擴建計劃將在科學園內加建兩座實驗室附屬樓，以及位於平台的專門實驗室。

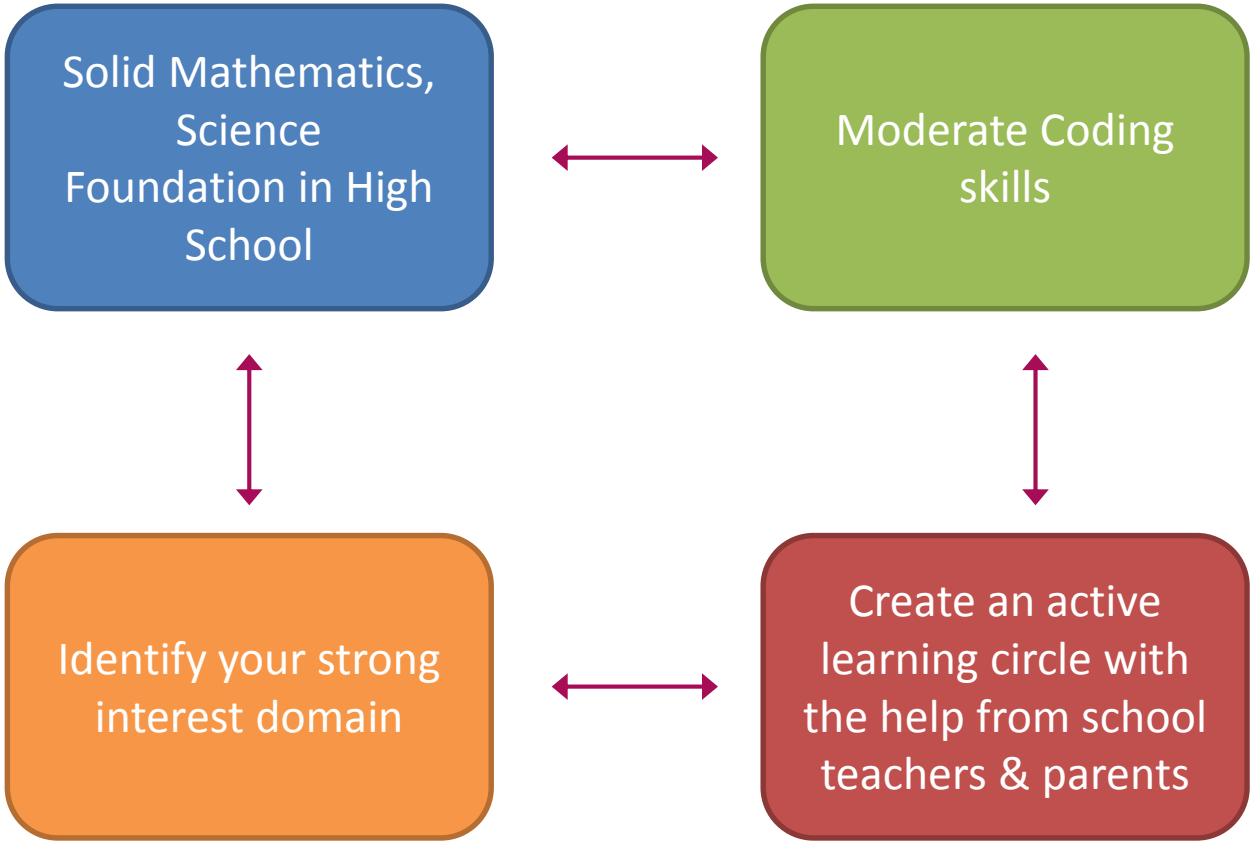
總結: 一切從「芯」開始

- Design Specification
- Functional Design
- Logic Design
- Circuit Design
- Physical Design
- Fabrication
- Packaging
- IC delivery



- Thank you very much for your listening.

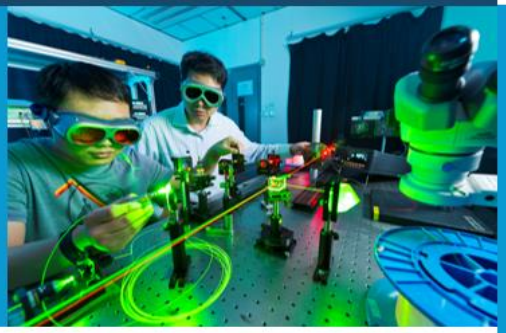
General Advice 給您的建議



Past workshops

How to adopt new tech in STEM?

5G Lab Visit



Product Design

Robotics Hardware Training

IoT Lab Training

CityU EE provides hardware and software complete training to support secondary school students.

Software Training For AI and coding

phone : +852 3442 7740 | www.ee.cityu.edu.hk

CityU
Department of Electrical Engineering
香港城市大學
City University of Hong Kong

Office of Education Development and Gateway Education
香港城市大學 City University of Hong Kong

Department of Electrical Engineering
香港城市大學 City University of Hong Kong

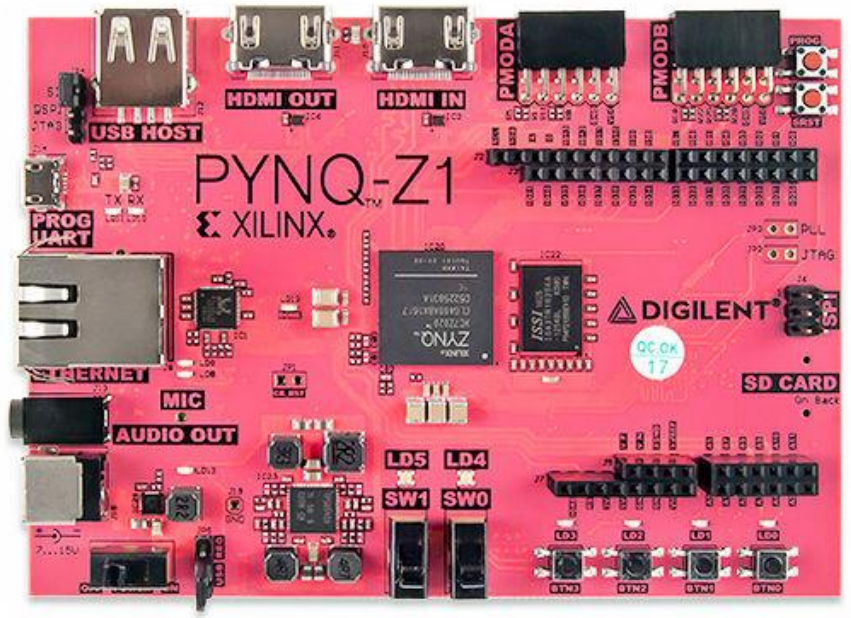
LEARNING CODING AND AI PROGRAM 2019

Learn to Code for AI !
Oct to Dec, every Sat (except exam period), 2pm-5pm

Briefing Session: 27/9 (Friday), 5pm, LT-11, Yeung

WORKSHOP CONTENT:

1. BASIC PYTHON
2. ADVANCED PYTHON
3. MACHINE LEARNING WITH PYTHON
4. DEEP LEARNING WITH PYTHON
5. HARDWARE ACCELERATION WITH PYTHON



REGISTER NOW!

STUDENTS FROM ALL MAJORS ARE WELCOMED!

Contact person: John Wong (Whatsapp: 6485 4147, Email: tljewong@cityu.edu.hk)
Remark: This program is supported by CityU Teaching & Learning Fund

Department of Electrical Engineering
香港城市大學 City University of Hong Kong

What's Next? 下一步是什麼？

JS1205 Department of Electrical Engineering

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

(Options: BEng Computer and Data Engineering, BEng Electronic and Electrical Engineering*, BEng Information Engineering)

Our Majors

- Common first year
- Students choose a major after one year of study
- Majors offered:
  - BEng in Computer and Data Engineering (CDE) 工學士(電子計算機及數據工程學)
  - BEng in Electronic and Electrical Engineering (EEE) 工學士(電子及電機工程學)*
  - BEng in Information Engineering (INFE) 工學士(資訊工程學)

* *Change of major title from "Electronic and Communication Engineering" to "Electronic and Electrical Engineering" is subject to approval of the University.*

Program Highlights

CDE - Computer Applications

- Digital Systems 數碼系統
- Computer and Embedded Systems 電腦及嵌入式系統
- Security Systems 保安系統
- Data Center and Cloud Computing 數據中心及雲端運算
- Big Data and Multimedia 大數據及多媒體科技

INFE - Computer Network and System

- Networking and Telecommunications 網絡與通訊
- Algorithms and Software 算法與軟件
- Cybersecurity and Forensics 網絡安全與鑑證
- Artificial Intelligence and Big Data 人工智能與大數據
- Signal and Image Processing 訊號與影像處理

EEE- Electronic and Electrical Systems

- Wireless Communications & Data Technology 無線通訊及大數據技術
- Terahertz & Optical Technologies 太赫茲及光學科技
- Photonics, Electronics and Sensors 光電子、電子及感應器
- Smart Control & Power Systems 智能管理及能源系統
- Bioelectronics and Bioinformatics 生物電子和生物信息技術

1) Principal Nomination Scheme

2) AI Workshop for High School Students

3) EE International students summer course

4) Face Recognition workshop for High School Students

5) Others upcoming

https://www.ee.cityu.edu.hk/home/

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

https://www.ee.cityu.edu.hk/home/doc/programme/CityU_EE-V3.0.pdf

CityU Department of Electrical Engineering 香港城市大學 City University of Hong Kong

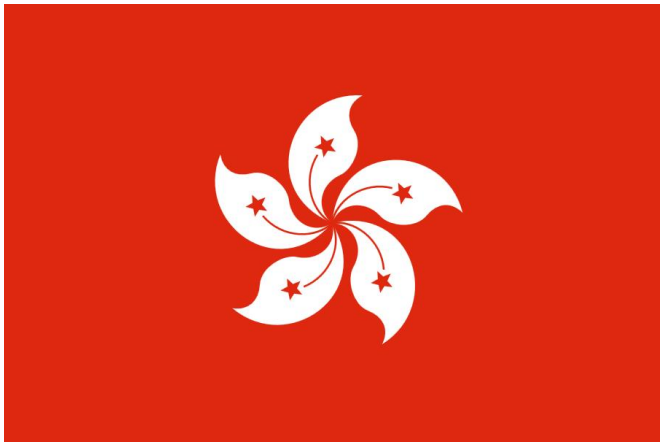
Acknowledgements 致謝

- CityU Provost Office, CityU-Learning Team
- Prof. Stella Pang – Head, Department of EE, CityU
- Yang Lyu, Vic Huang, PhD Student, Department of EE, CityU
- Kit Sit, PhD Student, Imperial College London, UK
- Clarissa Yung, UG Student, Edinburgh, UK

CityU Department of Electrical Engineering
香港城市大學 City University of Hong Kong

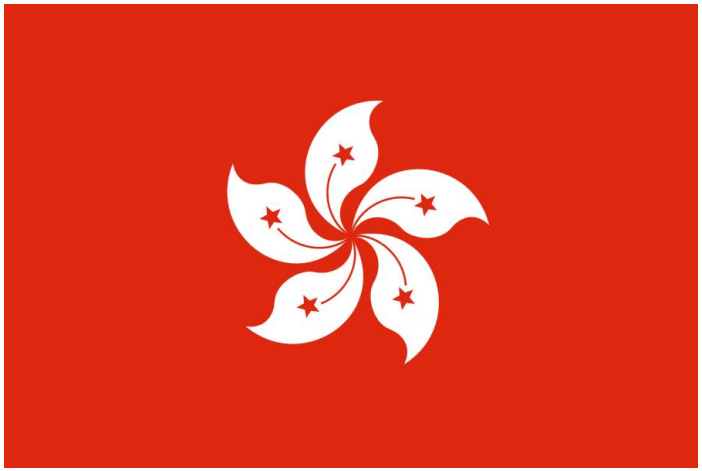
中學和高中教育

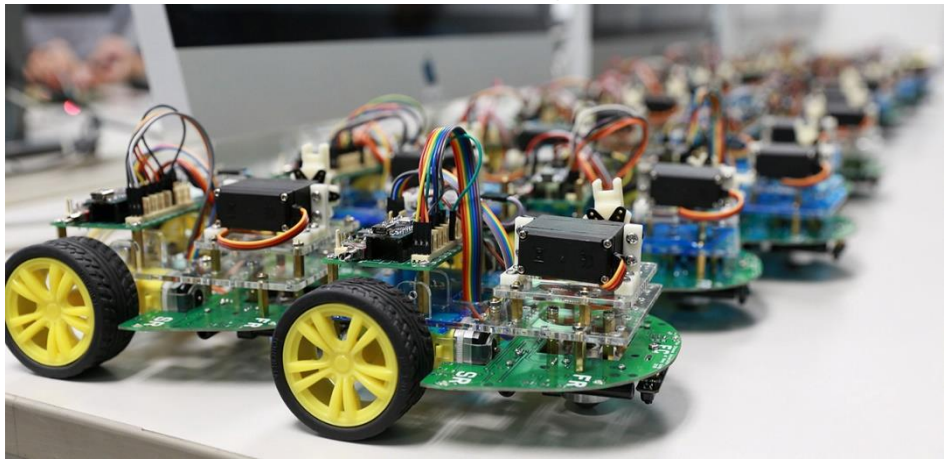
- HKCEE
  - Mathematics
  - Additional Mathematics
  - Physics, Chemistry, Biology
  - Computer Studies
- HKAL
  - Pure Mathematics
  - Applied Mathematics
  - Physics
  - Chemistry



大學工科教育

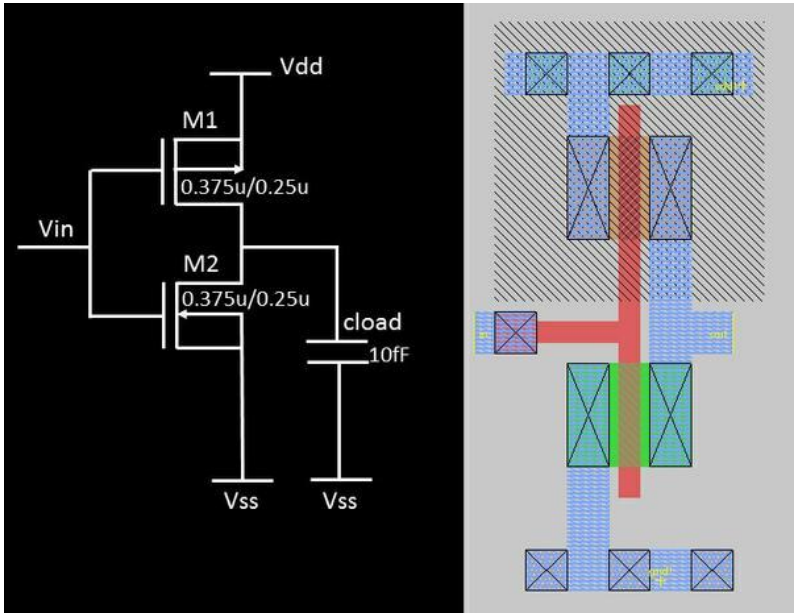
- BEng
  - Digital Logic (no VHDL)
  - System Design (VHDL)
  - FYP (published one paper in TENCON, South Korea)

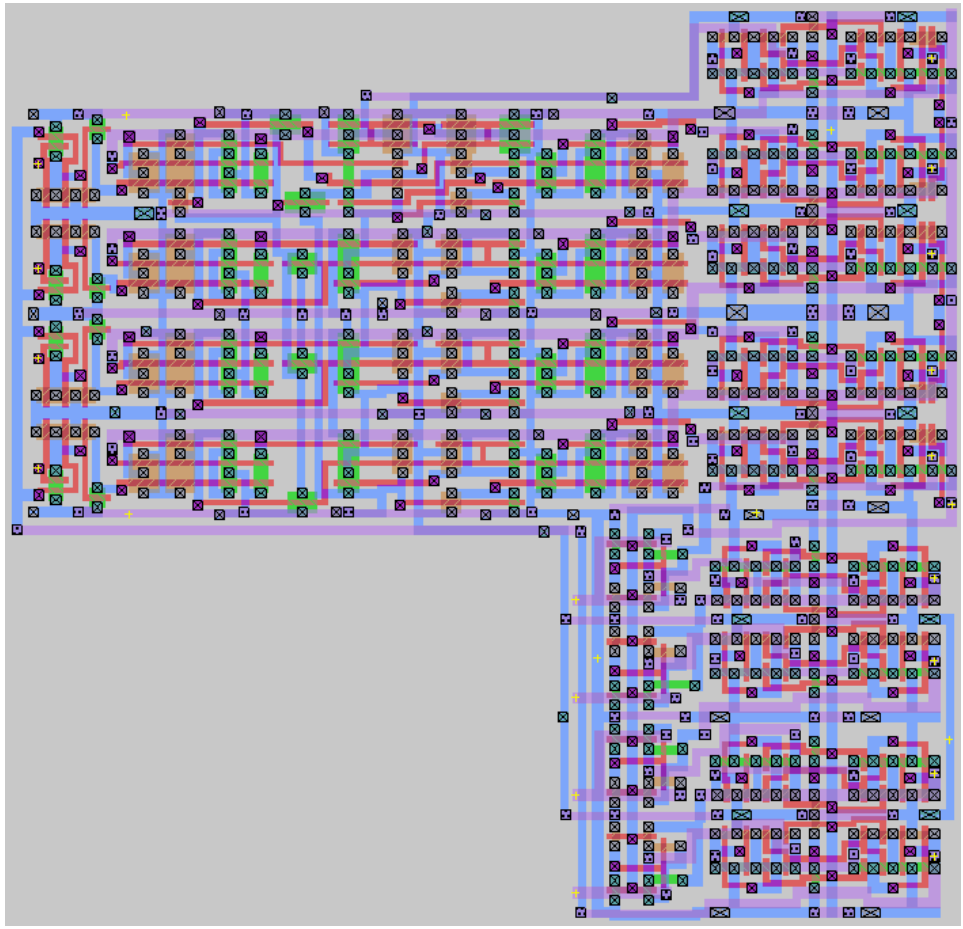




畢業設計論文

- Asynchronous Forth Processor – Layout the whole chip





從頭開始設計我的第一個處理器

- Fabricate my first Chip!
- IEEE TENCON is a flagship conference in Asia-Pacific.

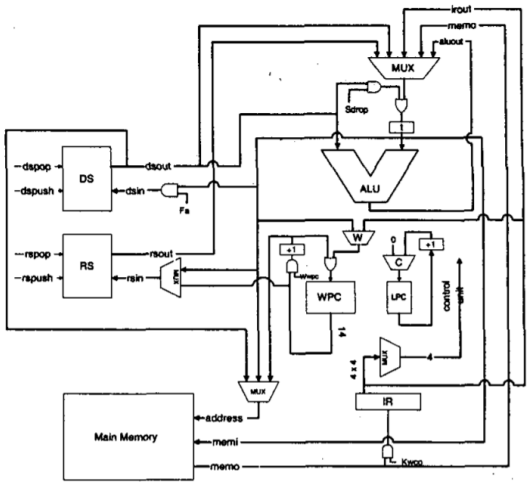


Figure 2: The datapath of MSL16A

1999 IEEE TENCON

MSL16A: An Asynchronous Forth Microprocessor

P.K. Tsang, C.C. Cheung, K.H. Leung, T.K Lee, P.H.W. Leong
Department of Computer Science and Engineering
The Chinese University of Hong Kong
{pktsang, ccheung2, khleung, tonylee, phwl}@cse.cuhk.edu.hk

Abstract

A 16-bit Forth microprocessor, MSL16 [7], was developed for embedded applications as the design offers good code density, easily developed software development tools, high performance, and small area. A delay-insensitive re-implementation of the processor has been developed to explore the potentials of asynchronous logic for low-power applications and to demonstrate the feasibility and practicability of using asynchronous circuits in embedded applications. This paper describes the asynchronous clone of MSL16. The implementation and performance evaluation of it is also presented. The design will be fabricated using AMI 1.2μ CMOS double layer metal process in 3Q99.

Recent research has demonstrated that asynchronous circuits techniques have matured and implementations of asynchronous processors have been reported [9, 15, 10, 12, 1, 11, 2, 14]. The asynchronous re-implementation of the microprocessor, called MSL16A , has been developed to investigate the potential advantages that asynchronous designs may enjoy, namely average-case performance instead of worst-case performance and low power consumption. MSL16A was also developed to demonstrate the feasibility and practicability of using asynchronous circuits in embedded applications.

The paper is organized as follows. Section 2 gives a brief description of the architecture of MSL16A. The design methodology and circuit style used in designing MSL16A, which were an original application of

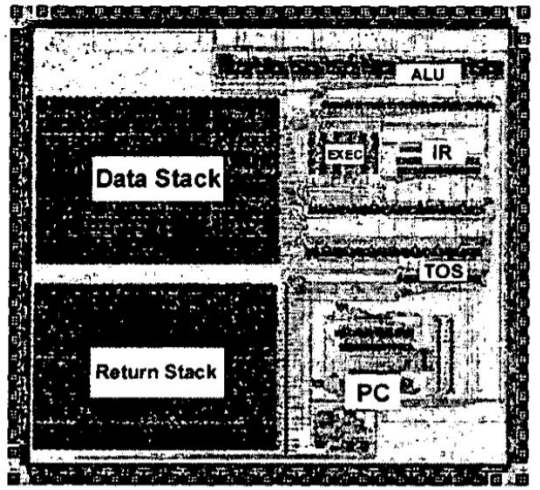
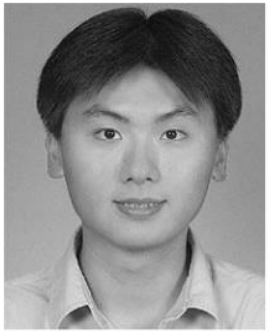


Figure 4: MSL16A chip image

哲學碩士（M.Phil）

- From a Layout engineer to become a **Computer Aided Designs (CAD) designer**
  - Circuit Partitioning
  - Switch-box designs



Chak-Chung Cheung received the B.Eng. and M.Phil. degree in computer engineering and computer science and engineering from The Chinese University of Hong Kong (CUHK), in 1999 and 2001, respectively.

In 2001, he worked as a System Administrator with the Center of Large-Scale Computation (CLC), Cluster Technology, Hong Kong. He is now an Instructor with the Deparment of Computer Science and Engineering, CUHK, and is responsible for the courses on Internet and Web Programming Technologies. His current research interests include optimization of logic and physical design automation of very large scale integration (VLSI) ASIC/FPGA designs and high-level synthesis of reconfigurable computing.

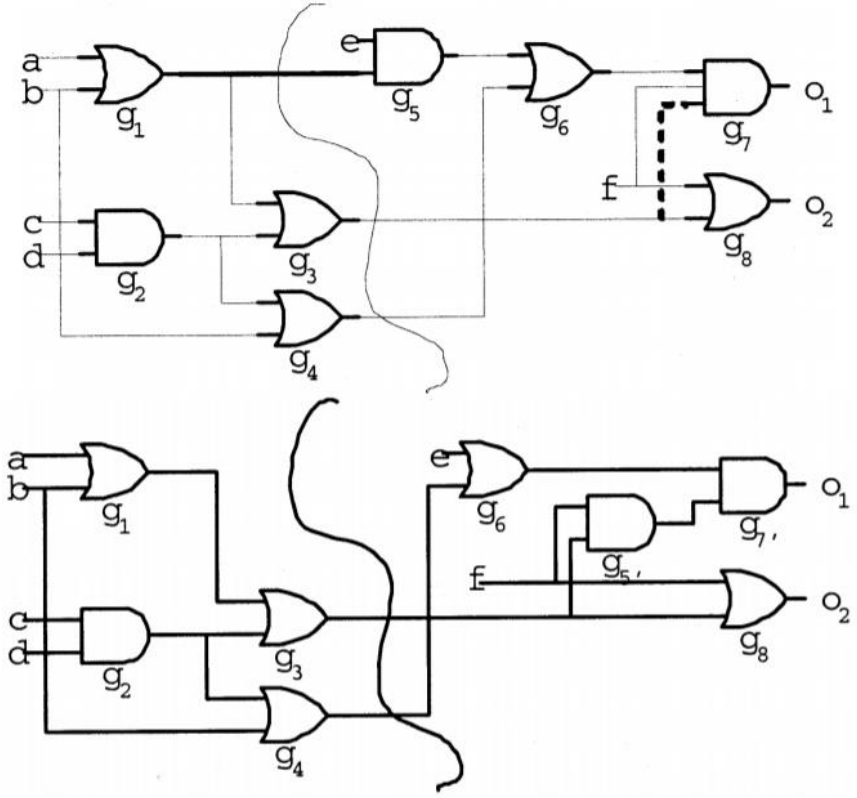
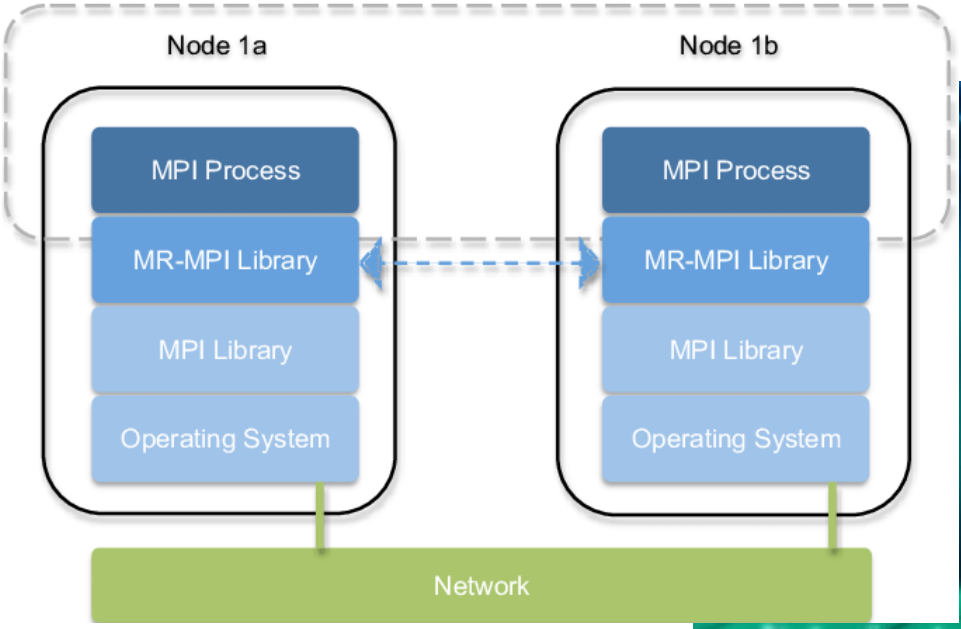


Fig. 1. Circuit partitioning by rewiring (cut net size improved from 3 to 2).

高性能計算公司

- Cluster Technology Limited
- Founding System Administrator
- HPC MPI Message Passing

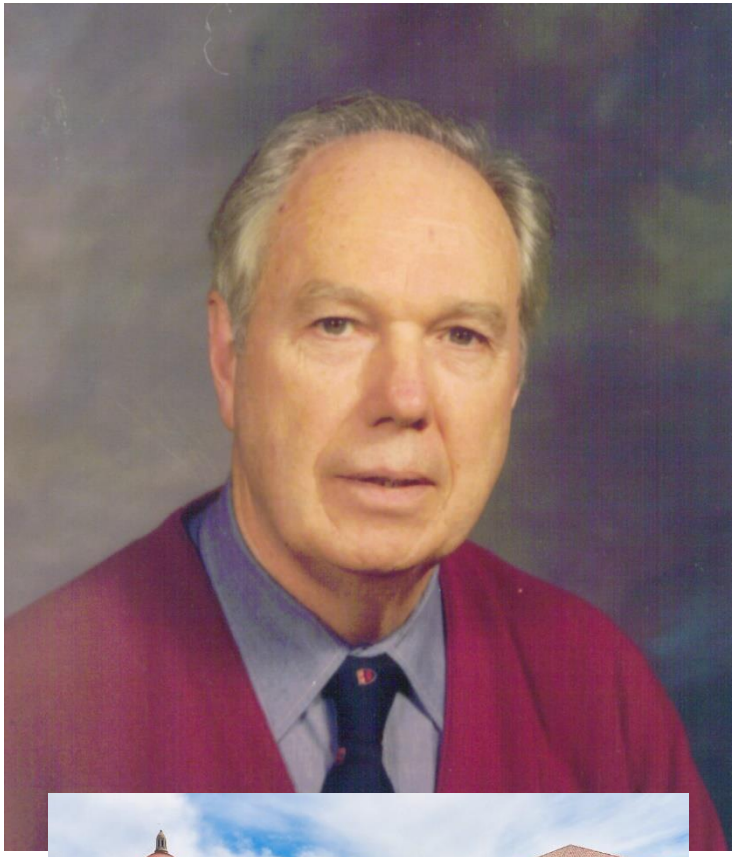
聯科集團
CLUSTERTECH

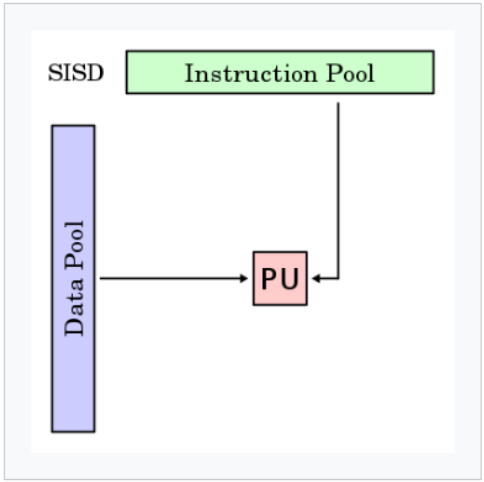


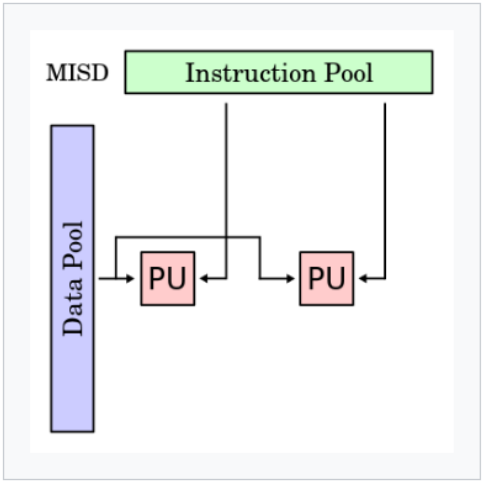
英國博士學位研究

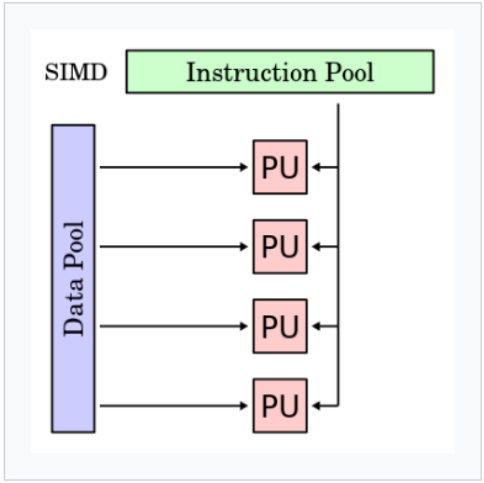
- Spent 3.5 years in London
- High-level designer
- Compiler design

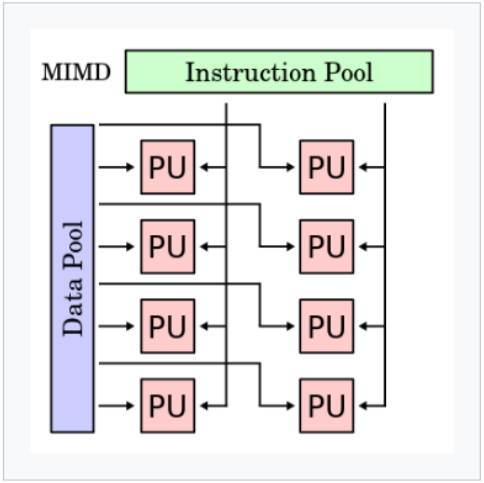
Prof. Michael Flynn - Stanford





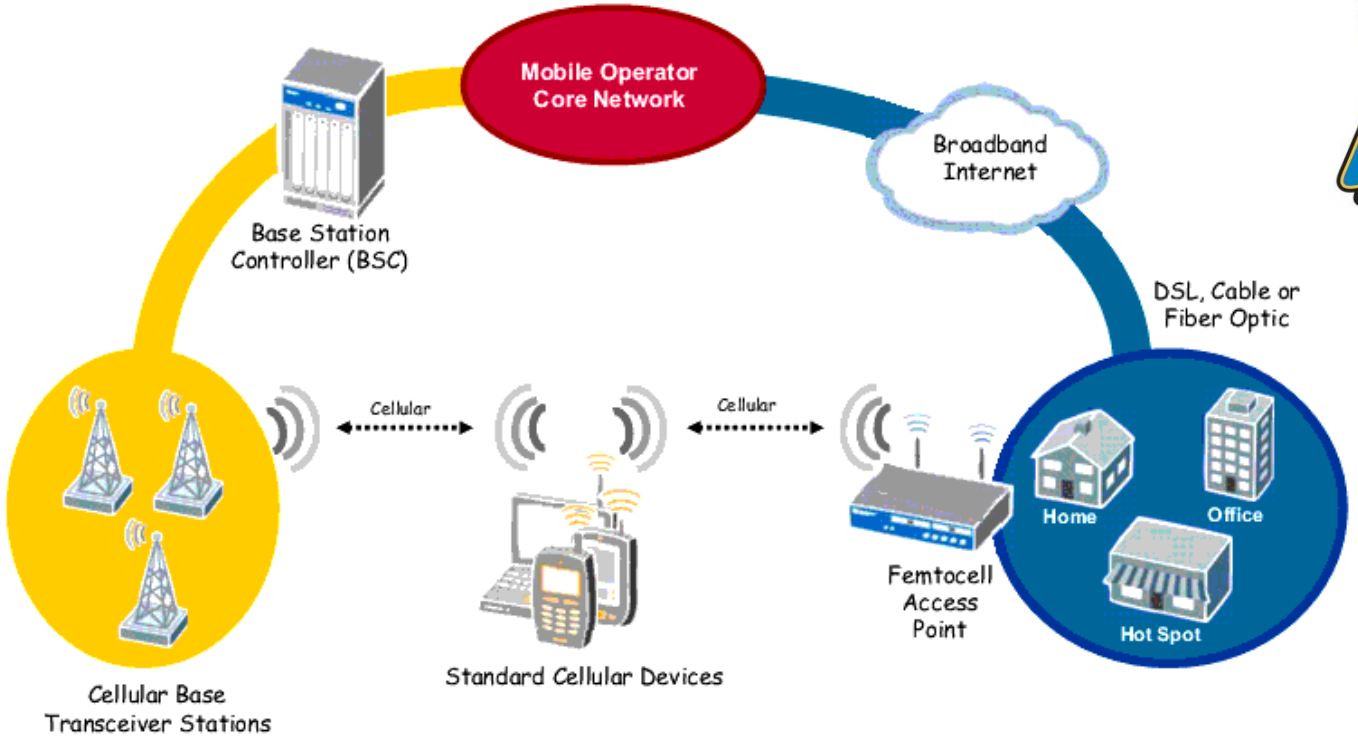






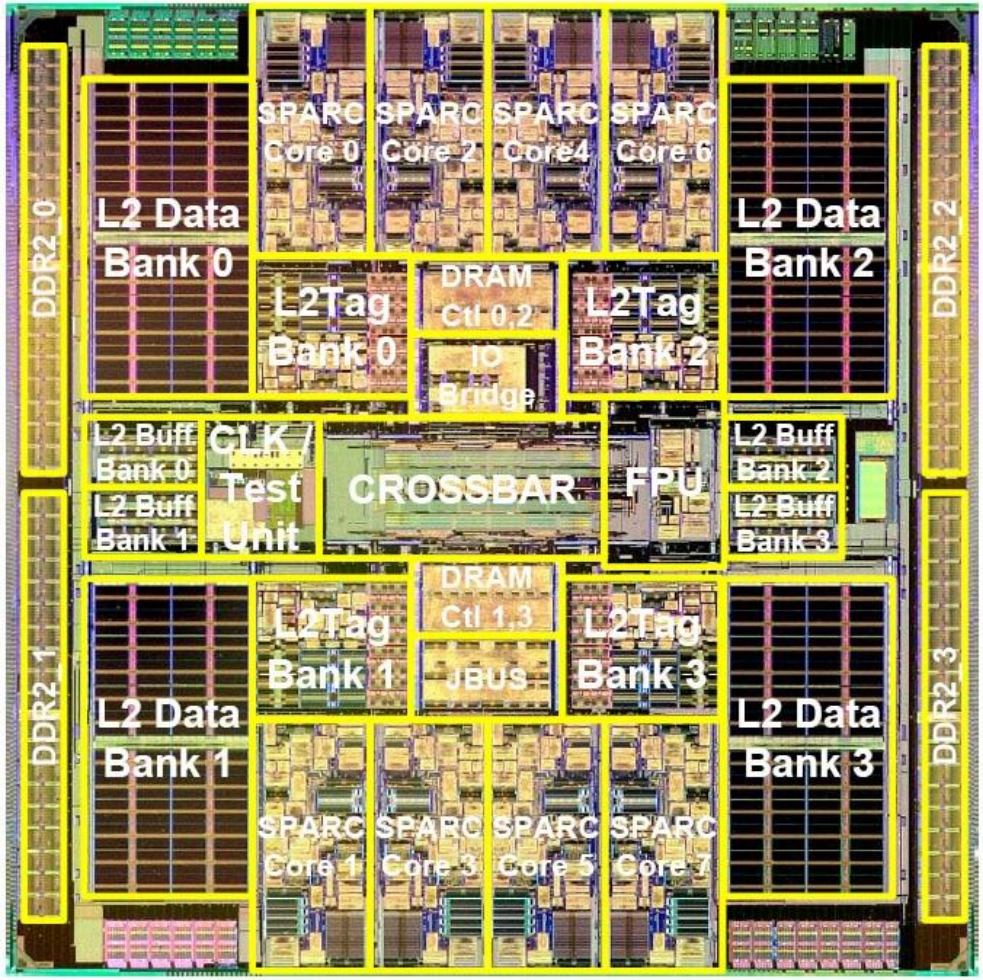
博士後研究工作 @ UCLA

- From Crypto-graphic, Arithmetic Design to system-level and designer.



客座研究員 @ Princeton

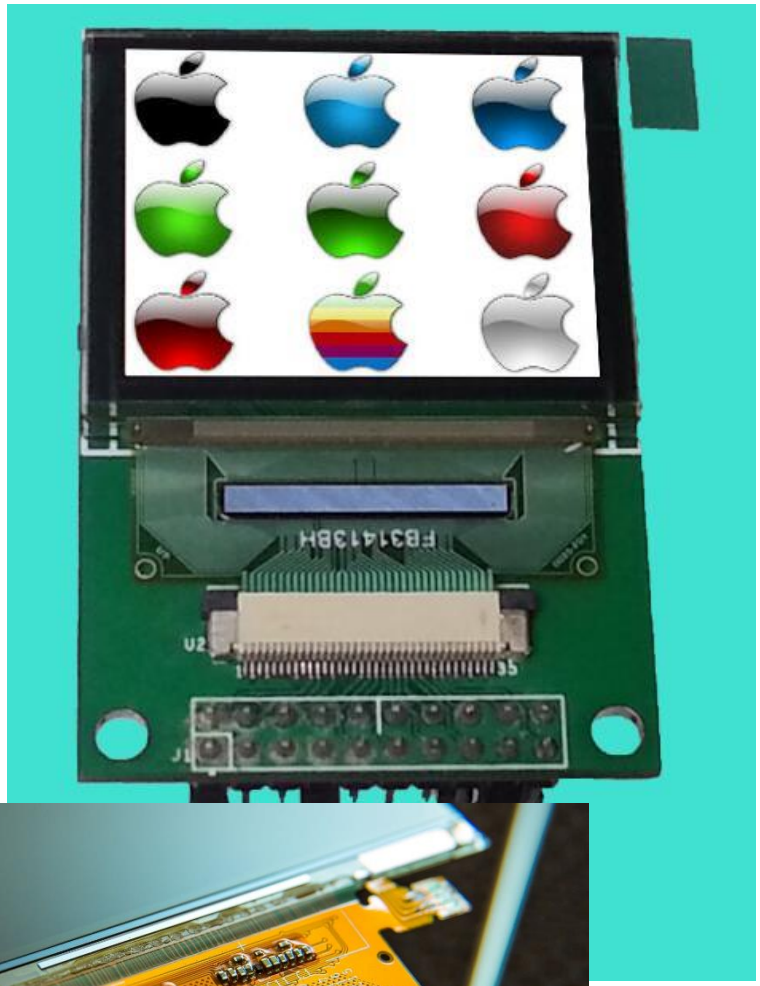
- Design a secure OpenSPARC Processor



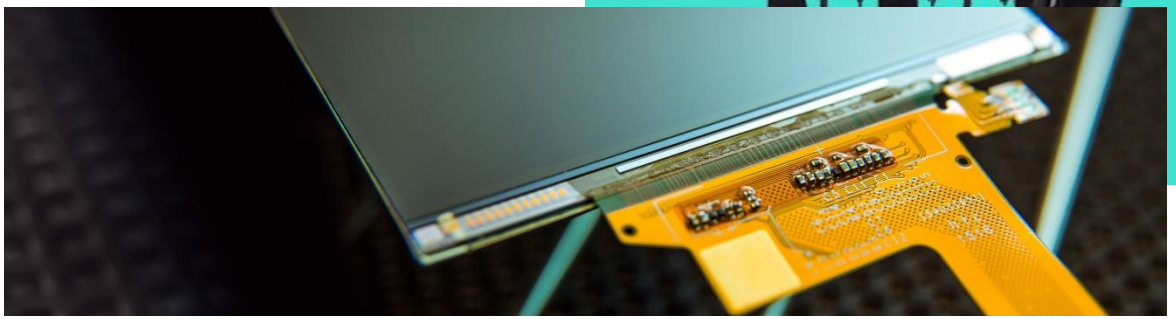
PRINCETON UNIVERSITY

Solomon Systech @ 香港科技園

- OLED Display IC Chip Designer
- Founded by a group of former Motorola Engineers
- Around 400 people



SOLOMON SYSTECH 晶門科技



城市大學電機工程

- My 10th year in CityU, EE

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City University of Hong Kong