Friday's Seminar

CITY UNIVERSITY OF HONG KONG
CENTER FOR CHAOS AND COMPLEX NETWORKS

HONG KONG POLYTECHNIC UNIVERSITY
DEPT. OF ELECTRONIC AND INFORMATION ENGINEERING

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Jointly present

SEMINAR SERIES ON COMPLEX SYSTEMS, NETWORKS, CONTROL AND APPLICATIONS

LEC : Learning Driven Data-path Equivalence Checking

by

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Date and Time: Friday, 18 October 2019, 4:30pm – 5:30pm
Venue: Room **CD634,** Hong Kong Polytechnic University
Reception starts at 4:15pm
(Language: **English**)

Abstract
In LEC system, we present a learning-based framework to solve the data-path equivalence checking problem in a high-level synthesis design flow, which is gaining popularity in modern day SoC design process where CPU cores are accompanied by dedicated accelerators for computation intensive applications. In such a context, the data-path logic is no longer a 'pure' data computation logic but rather an arbitrary sea-of-logic, where highly optimized computation intensive arithmetic components are surrounded by a web of custom control logic. In such a setting, the state-of-art SAT-sweeping framework at the Boolean level is no longer effective as the specification and implementation under comparison may not have any internal structural similarities. LEC employs an open architecture, iterative compositional proof strategies, and a learning framework to locate, isolate and reverse engineer the true bottlenecks in order to reason about their equivalence relation at a higher level. The effectiveness of LEC procedures is demonstrated by benchmarking results on a set of realistic industrial problems.

About the speaker
Jiang graduated from Computer Science Department at Jilin University, Changchun, China in 1992. In 1996, Jiang entered the graduate program in Computer Science at Tsinghua University, Beijing, China. A year later, from 1997 to 1999, Jiang studied in Computer Science Department at University of Texas at Austin as a graduate student. It is during the years at UT-Austin, Jiang developed an interest and focused in the field of formal verification of digital systems ever since. Between 2000 and 2014, Jiang worked on EDA formal verification tool development at Synopsys Inc and later at Mentor Graphics Corporation. Since March 2014, Jiang worked at Apple silicon division on SoC design formal verification and currently focusing on verification methodology and tool development for Apple CPU design and verification. While working in industry, between 2008 and 2017, Jiang completed his PhD degree at EECS Department in University of California at Berkeley in the area of logic synthesis and verification. Jiang 's dissertation work is on reasoning about high-level constructs for hardware and software formal verification in the context of high-level synthesis design flow.

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