PhD Oral Defense

Date: **5 August 2021 (Thursday)** **Time:** **10:00am**

Thesis Title

Novel Design, Architecture, and Optimization of Content-Addressable Memory (CAM)

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Abstract

Content-addressable memory (CAM) is a high-speed lookup memory, which searches the entire memory in parallel and provides address of the input search word. FPGA-based CAM research focuses on three parameters of the CAM design on FPGA resources, i.e., hardware utilization, power consumption, and speed. Four independent but closely related projects have been completed so far. Zi-CAM and RPE-TCAM has improved the power consumption while D-TCAM and MUX-Update has improved the speed compared to the existing CAM architectures. Zi-CAM: Power consumption of FPGA-based binary CAM is reduced by proposing a novel architecture using LUTs. The whole architecture is divided into RAM block and LUT block. D-TCAM: A high-throughput (speed) ternary CAM is proposed in this work which exploits the LUT-FF pair nature of Xilinx FPGAs. We presented two mechanisms for updating FPGA-based TCAM. A novel power-aware reconfigurable FPGA-based TCAM architecture is proposed that enables only a portion of the hardware to perform the search operation. We propose a solution to bank overflow using backup CAM (BUC) to handle the overflowed CAM entries. Future work includes exploring these memory architectures to accelerate machine learning and further optimize its implementation on FPGAs.