

Huawei Hong Kong Research Center

Huawei Hong Kong Research Center was established in 2018, focusing on chipsets, software engineering, AI, and theoretical researches. We are currently seeking high-caliber Engineers and Researchers at all levels to join our new team.

Job Highlights

- R&D
- High speed SERDES, high performance linear regulator, PLL
- Mixed-Signal IC Design

Analog Design Engineer

You will take part in designing and evaluating current micro-architecture of different major Analog IPs, including high speed SERDES, high performance linear regulator, PLL, etc. and contribute to the various phases of the development work, including but not limited to feasibility studies, performance and functional modeling, design benchmarking, micro-architecture definition. You will work closely with the architects, signal integrity team, physical integration team and product team to deliver best in class Analog IPs design.

Responsibilities

- Generate design specifications and determining micro-architecture for Memory PHY and High Speed SERDES IPs, high performance on-die linear regulator and PLL;
- Participate in circuit design and simulation, physical layout design and review of physical design layout of circuits;
- Participate in development of rtl behavioral model, timing model, and system performance model of circuits;
- Participate in evaluation and troubleshooting of circuits.

Qualifications

- Bachelor or higher degree in Electronic/Computer Engineering;
- Strong knowledge of mixed-signal design, signal integrity and power delivery network analysis;
- Design and development experience on various analog circuits, like high speed serial transmitter and receiver, high performance linear regulator, DLLs, and/or PLLs;
- Good understanding of ESD and latch-up requirements and device reliability rules;
- Strong knowledge of deep sub-micron/finfet CMOS process technology;
- Good knowledge of layout techniques, extractions and parasitic effects;

- Experience with system behavioral and performance modeling with Matlab/Verilog-AMS is highly desirable;
- Good command of written and spoken English and Chinese (Mandarin).
- Good team player with strong communication skills.

For interested parties, please send your full resume with and salary expectation to: chung.pui.yi@huawei.com. Applicants who are not invited for interview within 6 weeks may assume their application unsuccessful.