

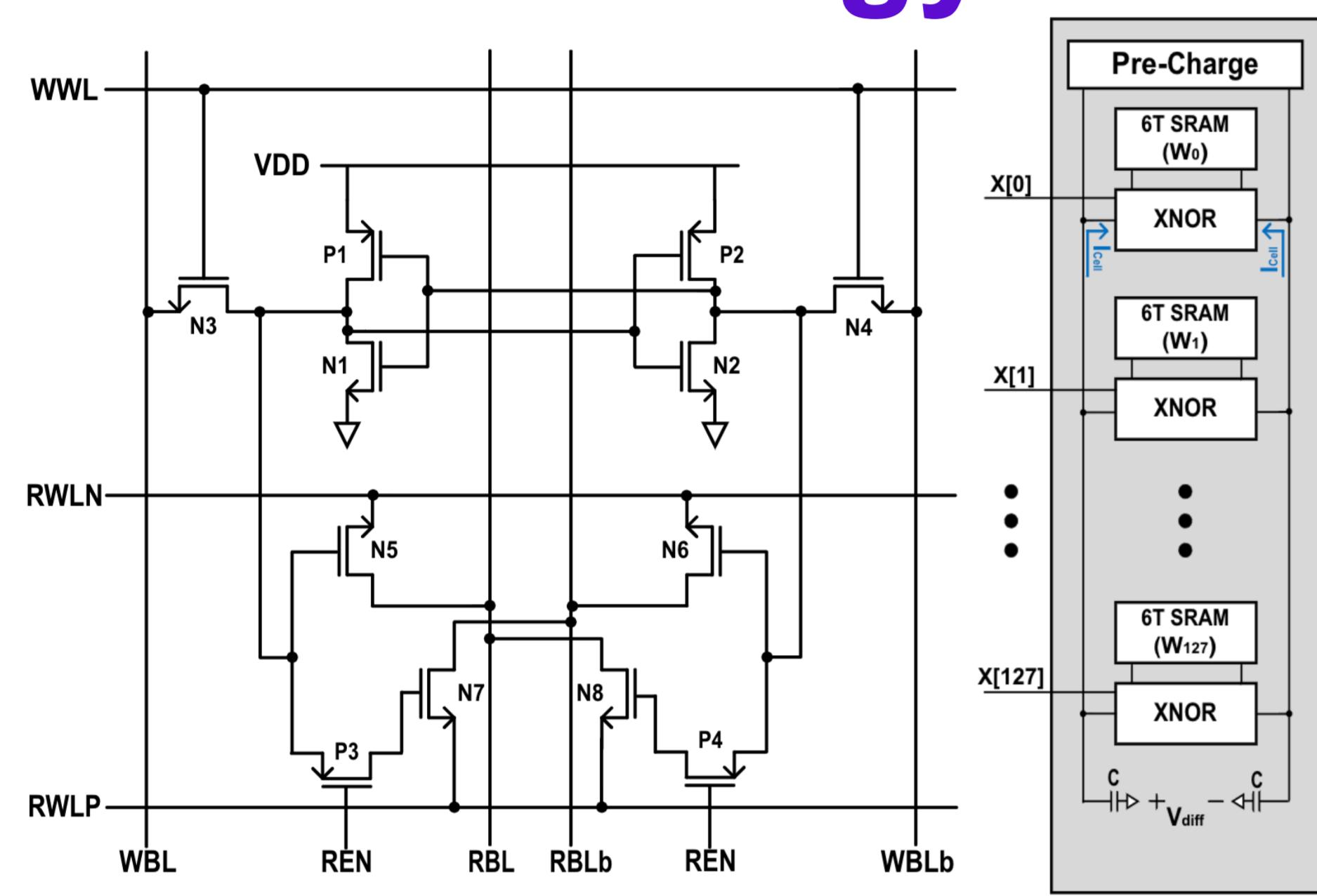
A Current-Based 12T XNOR SRAM Compute-In-Memory (CIM) Macro For Binary/Ternary Deep Neural Networks

PARK Junghyun ECE
Supervisor: Prof. Arindam BASU

Objective/Background

Develop a XNOR SRAM based CIM Macro
Featuring Current-Based XNOR Accumulation
for Binary/Ternary DNNs

Methodology

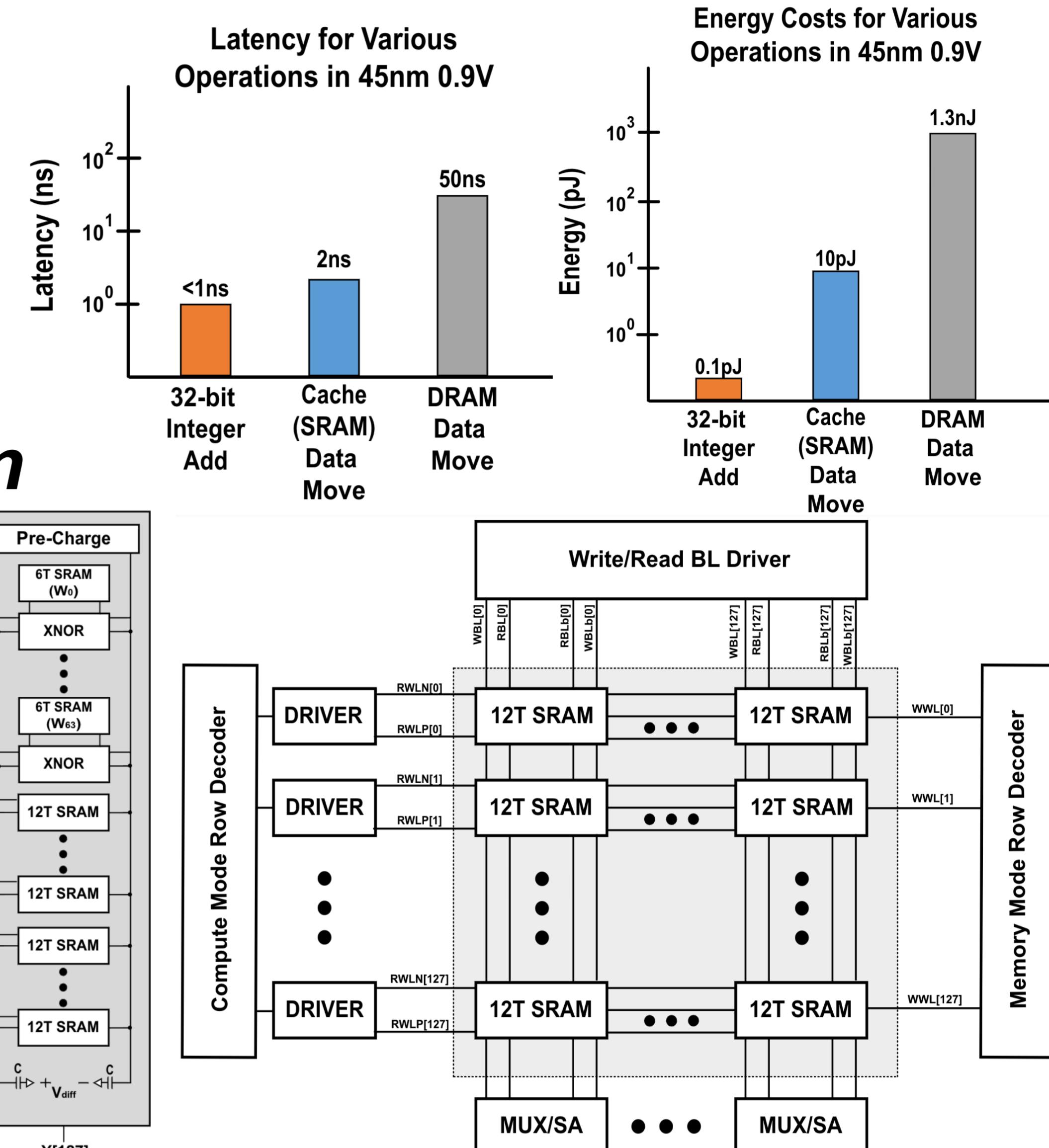


Bottom-Up Block Design

$$x^b = \text{Sign}(x) = \begin{cases} +1 & \text{if } x \geq 0 \\ -1 & \text{otherwise} \end{cases}$$

$$T_i = f_{\text{ternary}}(I_i, \Delta) = \begin{cases} +1, & I_i > \Delta; \\ 0, & |I_i| \leq \Delta; \\ -1, & I_i < -\Delta; \end{cases}$$

Why CIM?

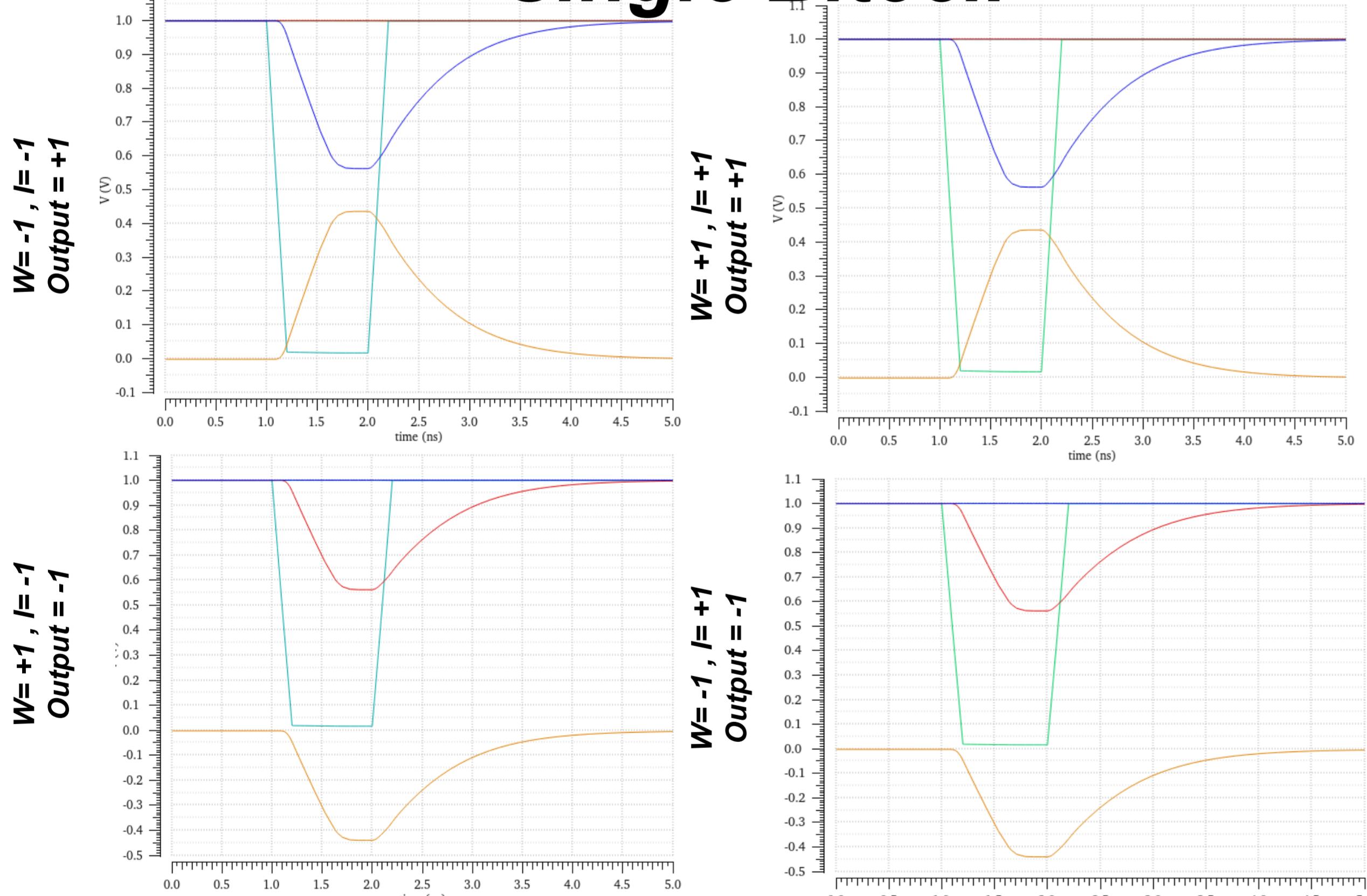


Logic Table

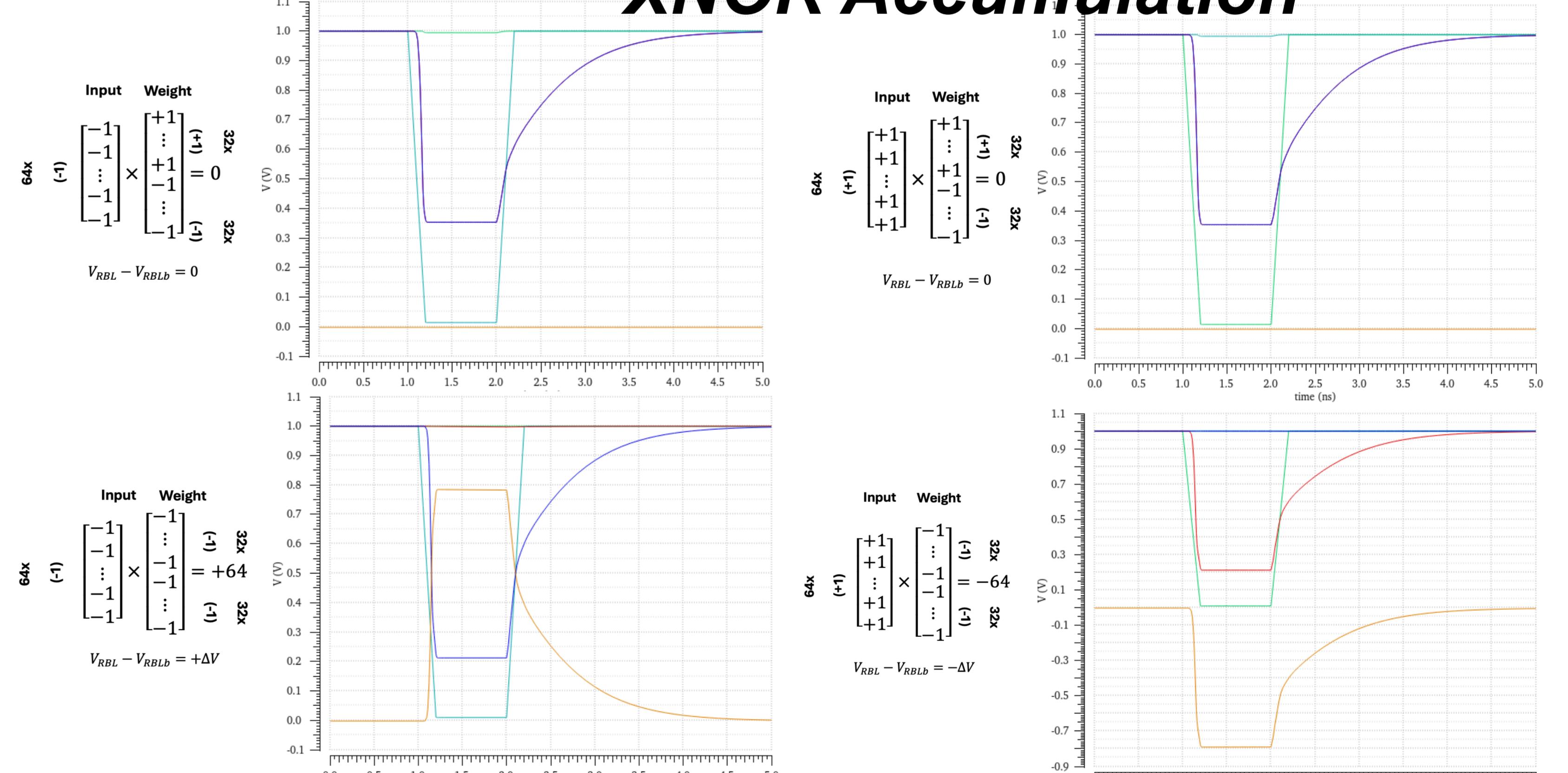
Input Weight	-1 (Q=H, Qb=L)	0 (No Change)	+1 (-ΔV)
RWLN = H RWLP = L	RWLN = H RWLP = L	RWLN = L RWLP = H	RWLN = L RWLP = L
+1 (Q=L, Qb=H)	-1 (-ΔV)	No Change	+1 (+ΔV)
-1 (+ΔV)	0	No Change	-1 (-ΔV)
+1 (-ΔV)	-1	No Change	+1 (+ΔV)

Results/Application

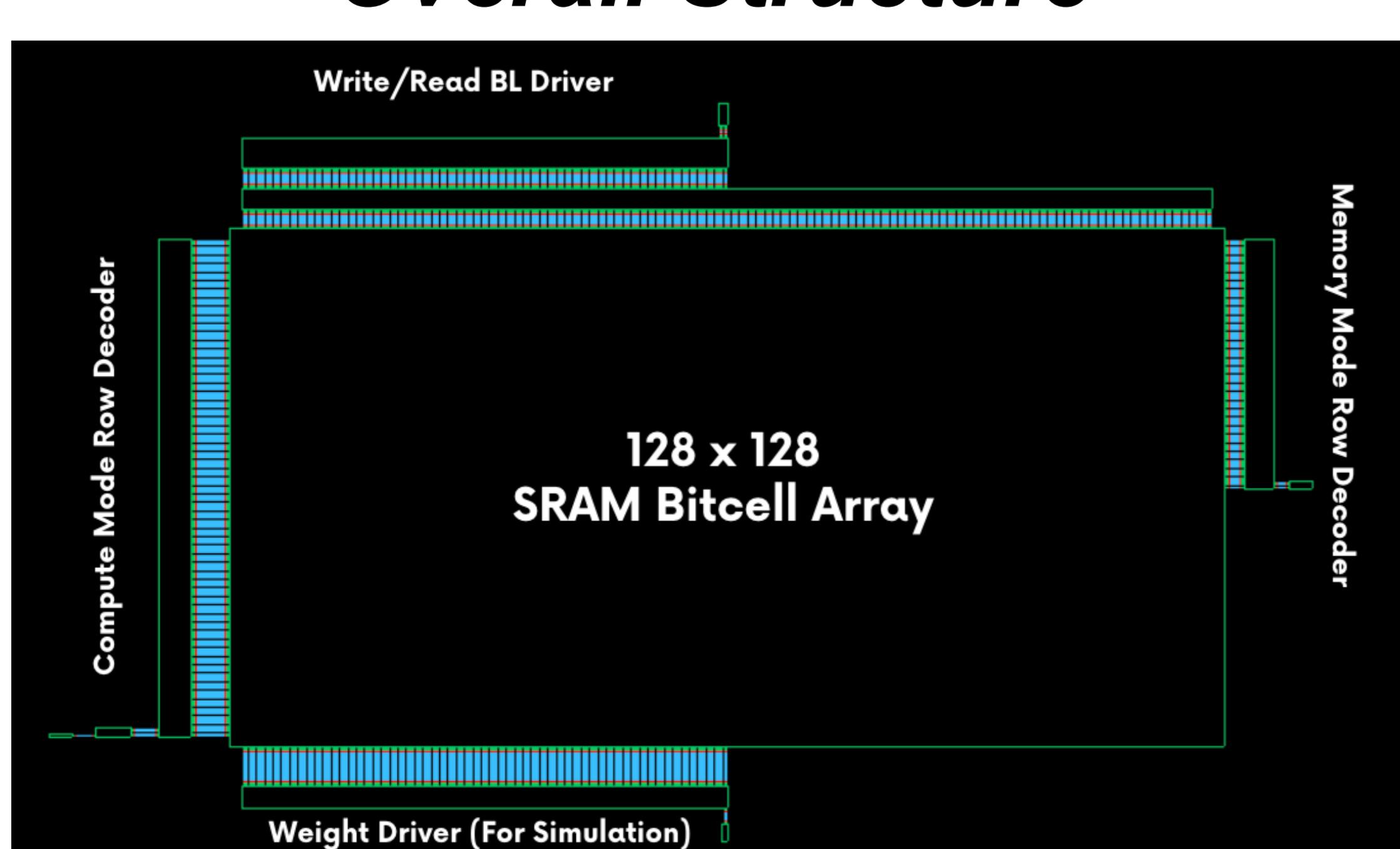
Single Bitcell



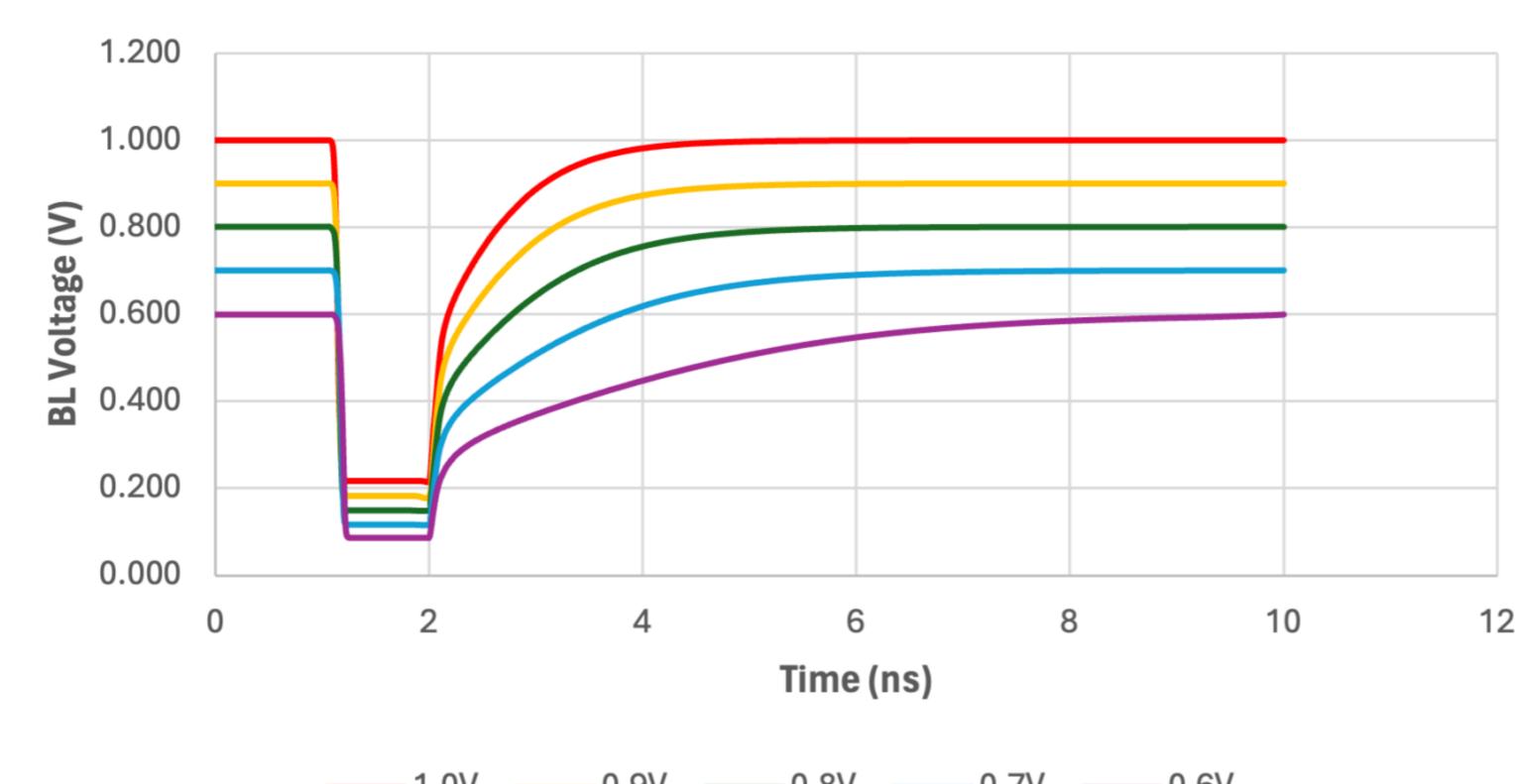
XNOR Accumulation



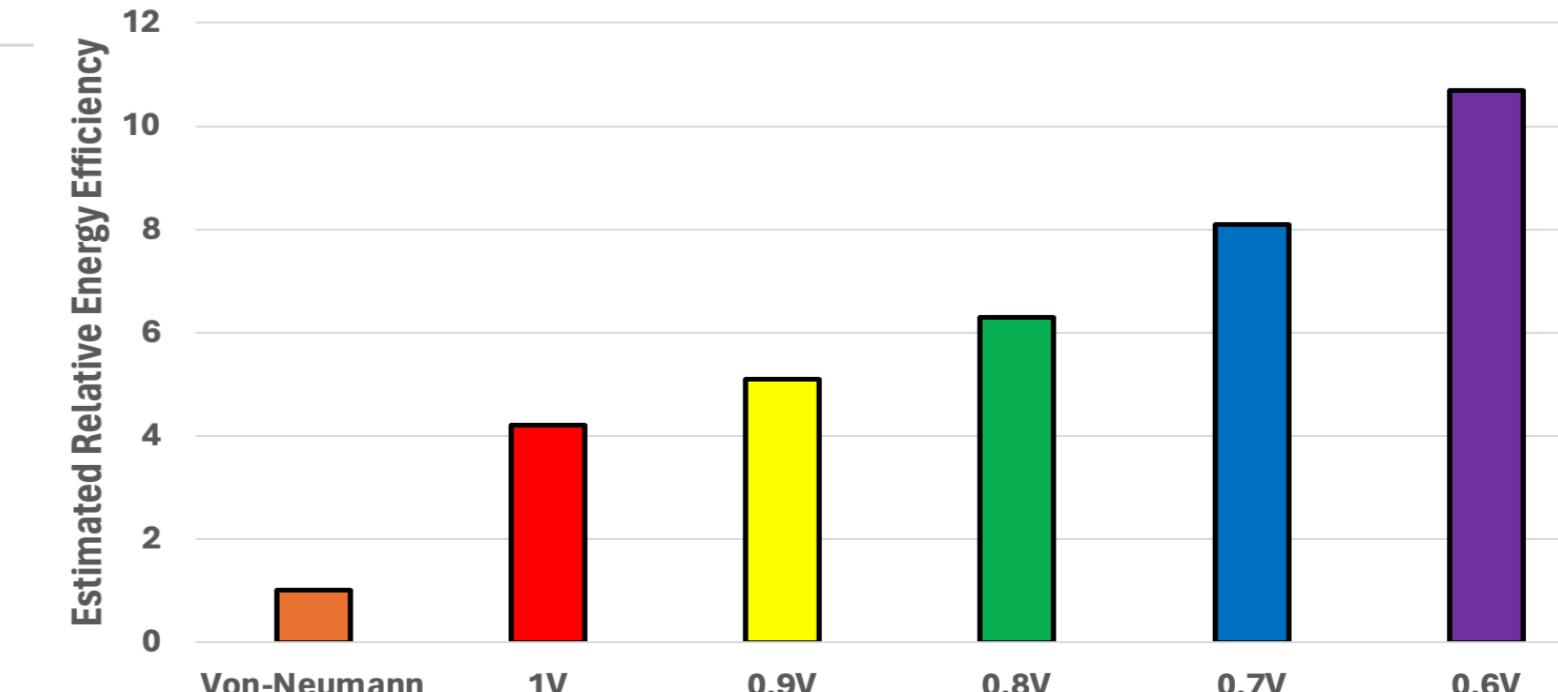
Overall Structure



Temporal Analysis of RBL (or RBLb) Voltage under VDD Scaling Variations



Energy Efficiency (XNOR Accumulation)



RBL/RBLb Voltage Drop Analysis in Relation to XAC Values

