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POWER MANAGEMENT IC DESIGN

Topologies and Models of DC/DC Converters

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Contents

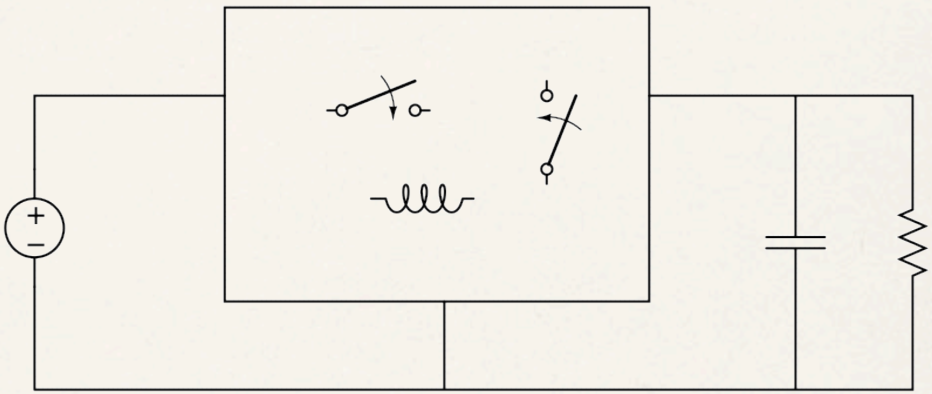
- Basic DC/DC converters
  - Basic topologies
  - Higher order converters
  - Transformer isolated versions

Models

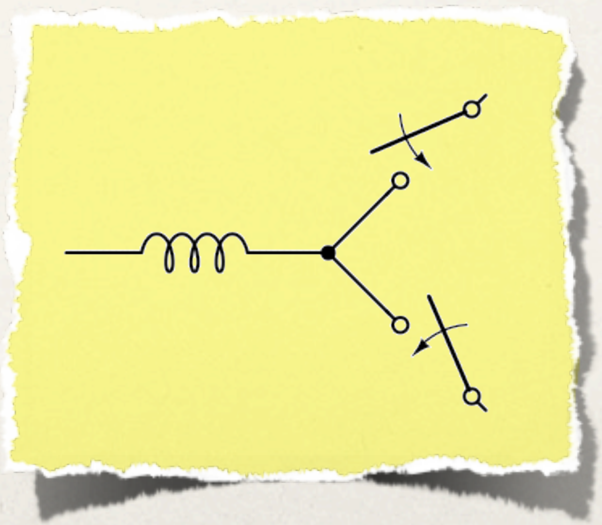
- Averaging
- Small-signal linearization
- Dynamic response of converters

DC/DC Converters

- **Initial criteria:**
  - voltage to voltage
    - (can be varied)
  - lossless conversion
  - being controllable
    - (voltage conversion ratio, power flow, etc.)

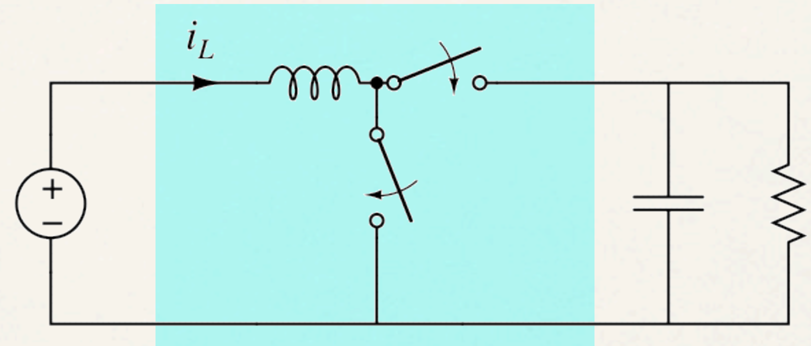


- *The simplest converter as constrained by Kirchhoff's laws should have*
  - *one inductor (current interface)*
  - *two switches*

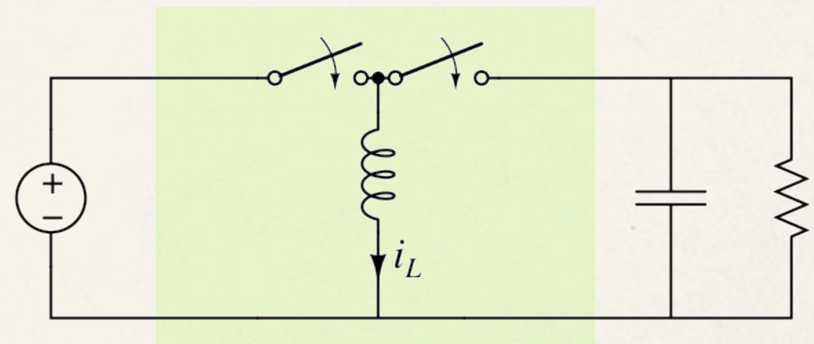


Three simplest topologies

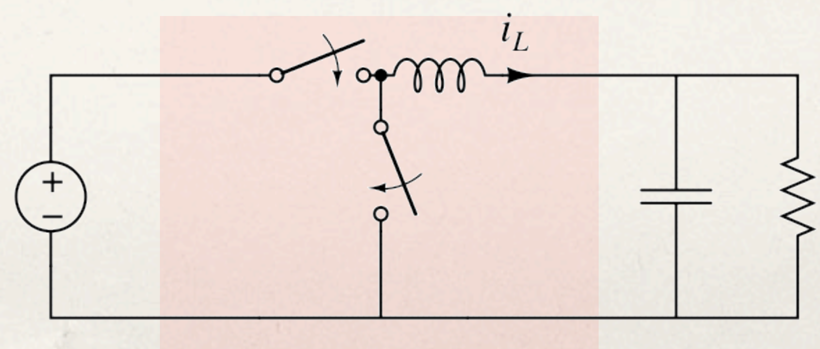
Boost converter



Buck-boost converter



Buck converter



The buck converter

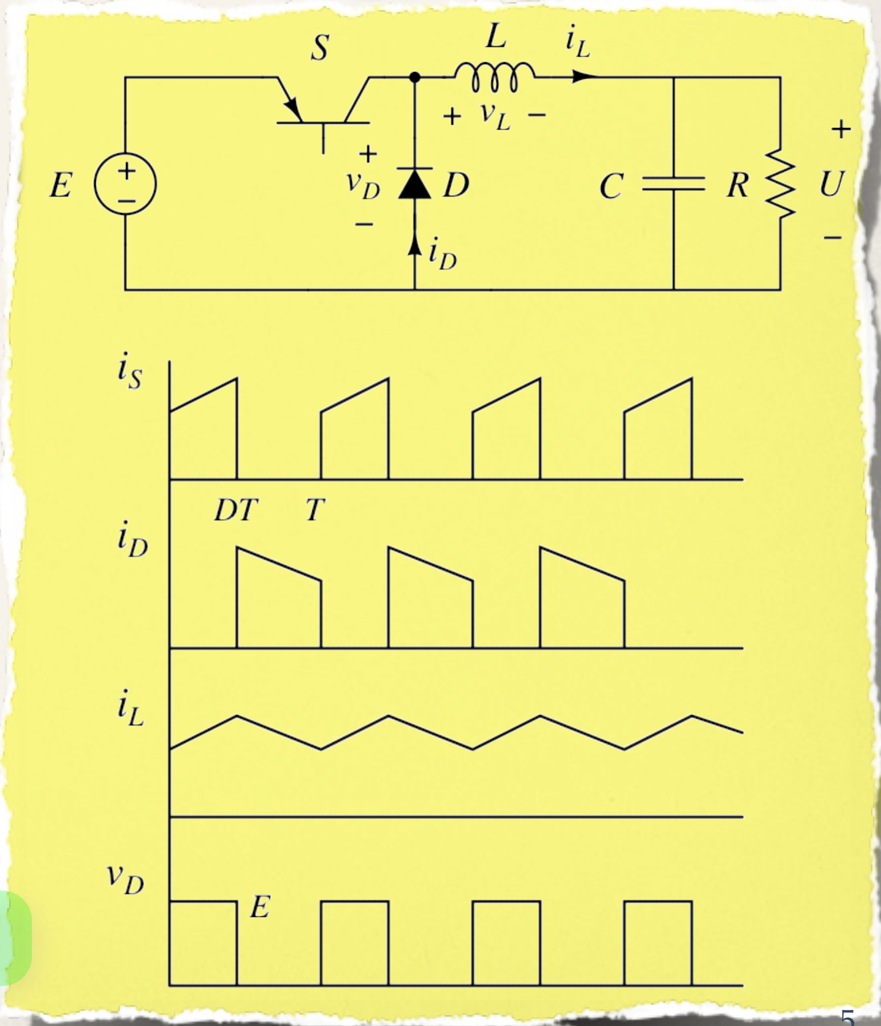
- Switch S is turned on and off very quickly, at a rate much greater than the output filter natural frequency. Switching period = T.
- Control parameter is ***duty cycle, d***

$$d = \frac{\text{duration when } S \text{ is on}}{\text{period}} = \frac{t_{\text{on}}}{T}$$

- OFF time: i_L falls, and $v_L = -U$.
- ON time: i_L climbs only if $E > U$, and $v_L = E - U$.
- At steady state, average v_L must be 0. Thus,

$$(E - U)D = U(1 - D)$$

- Hence, $U = D\,E < E$, i.e., **step-down converter**



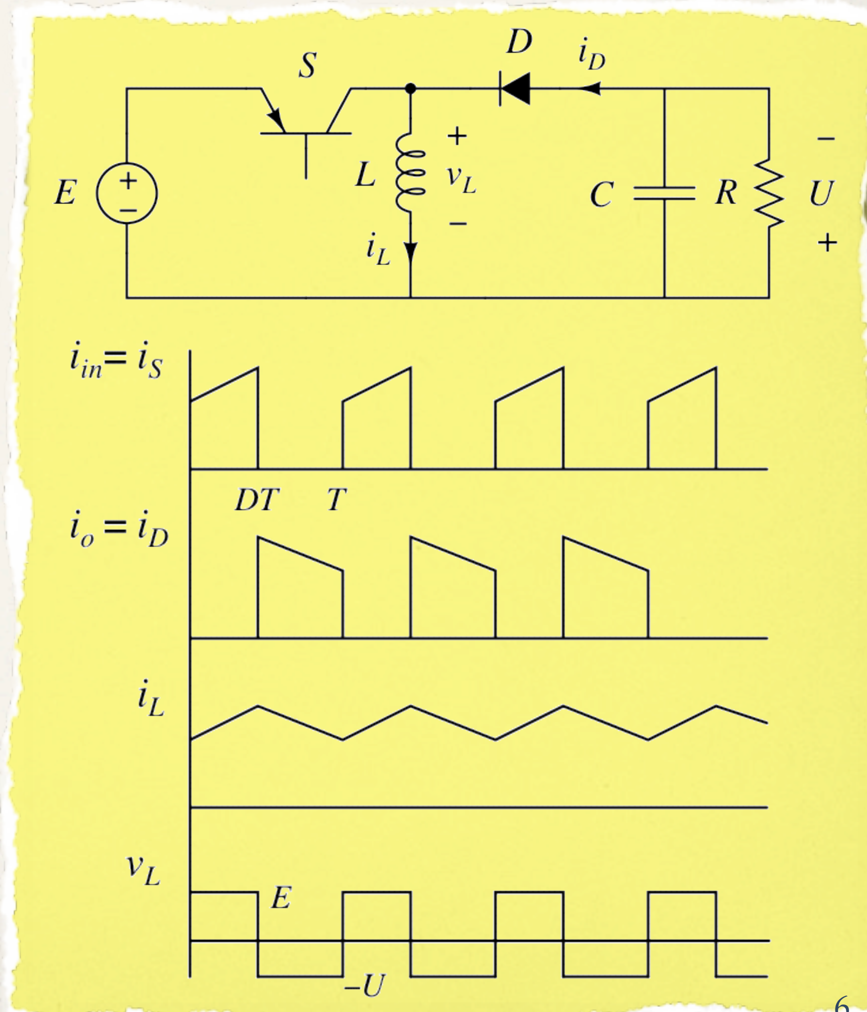
The buck-boost converter

- The inductor is connected to the source for DT and to the load for $(1–D)T$.
- ON time: i_L climbs, and $v_L = E$.
- OFF time: i_L falls, and $v_L = – U$.
- Thus, depending on the value of D, the output U can be either larger or smaller than E.
- At steady state, average v_L must be 0, i.e.,

$$ED = U(1 - D)$$

- Hence, $$U = \frac{D}{1-D}E$$

$$\begin{aligned} U &< E \quad \text{for all } 0 < D < 0.5 \\ &> E \quad \text{for all } 0.5 < D < 1 \end{aligned}$$



The boost converter

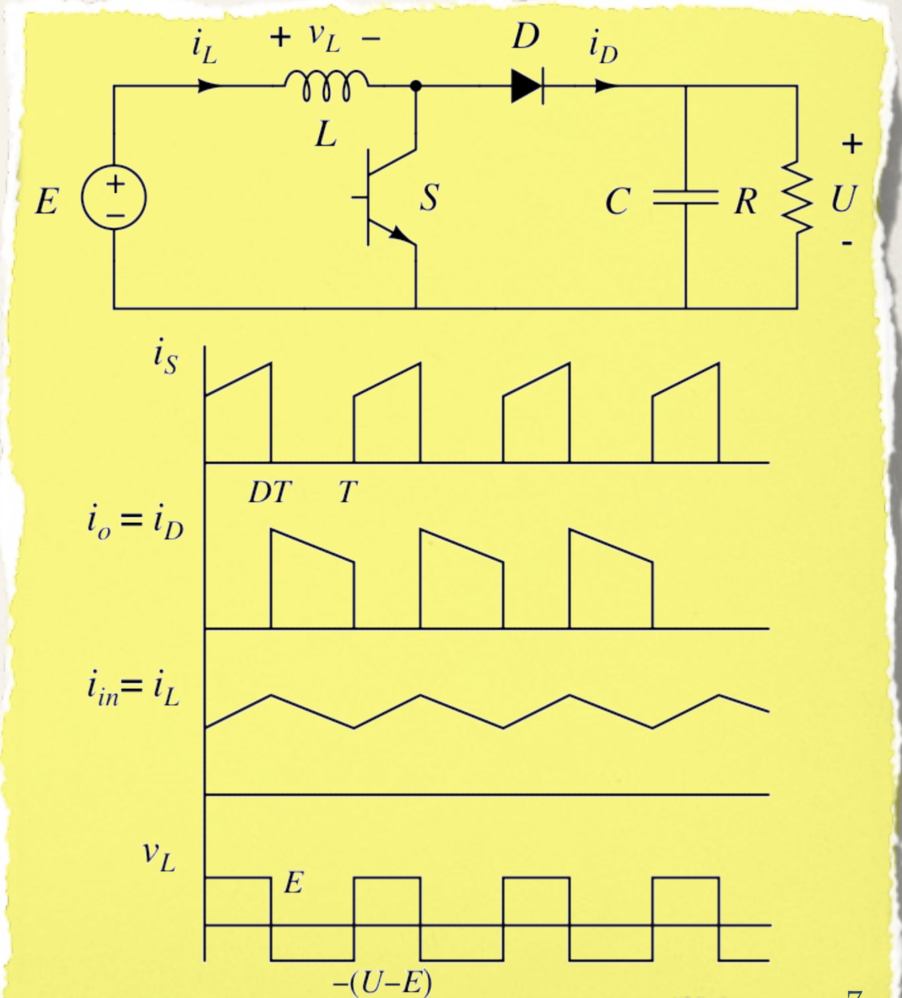
- The inductor is connected to the source for T and to the load for (1–D)T.
- ON time: i_L climbs, and $v_L = E$.
- OFF time: i_L falls, and $v_L = -(U-E)$.
- Thus, U must be larger than E for equilibrium to be achieved.
- At steady state, average v_L must be 0, i.e.,

$$ED = (U - E)(1 - D)$$

- Hence,

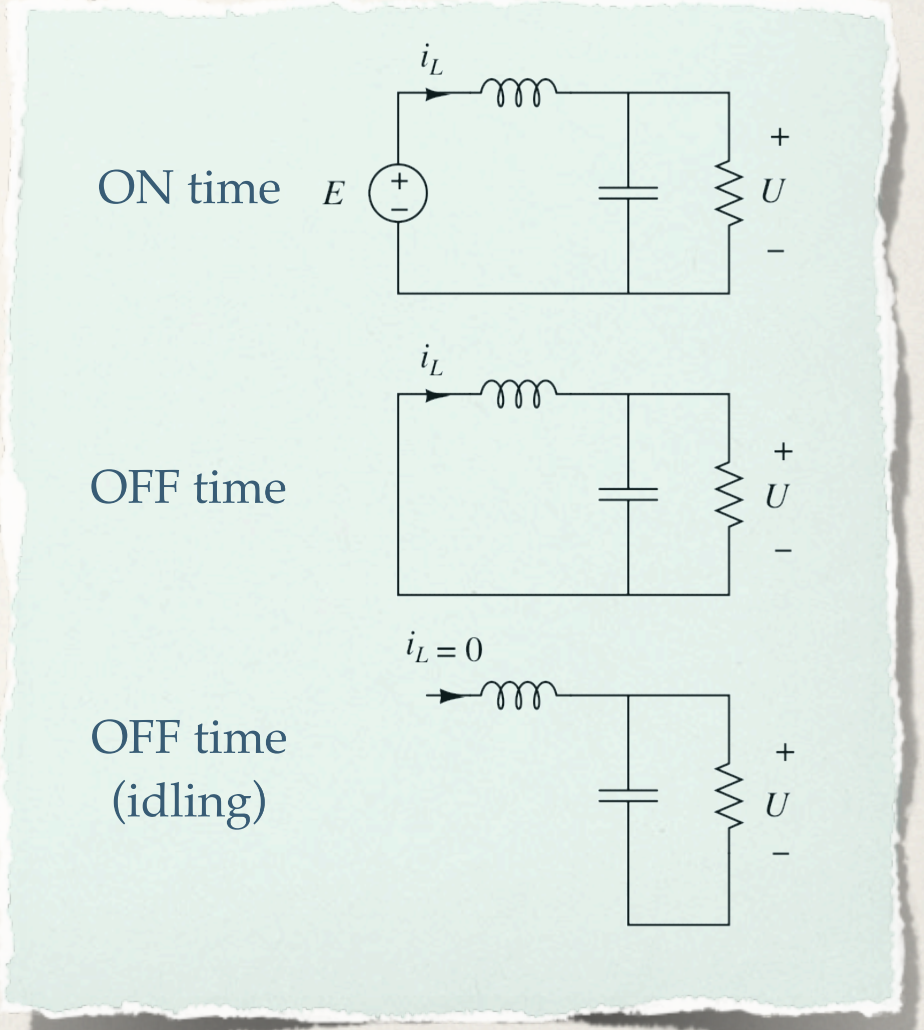
$$U = \frac{E}{1 - D} > E$$

  - i.e., **step-up converter**



Operating modes

- So far, we have assumed the inductor current maintains a positive value throughout the period. This operation is called ***continuous conduction mode (CCM)***.
- Let's look at the buck converter. However, if
  - ***the inductor is too small OR the period is too long,***
- then the inductor current could fall to zero during OFF time and the diode would be open again. This introduces an IDLING interval in which $i_L = 0$. This is ***discontinuous conduction mode (DCM)***.



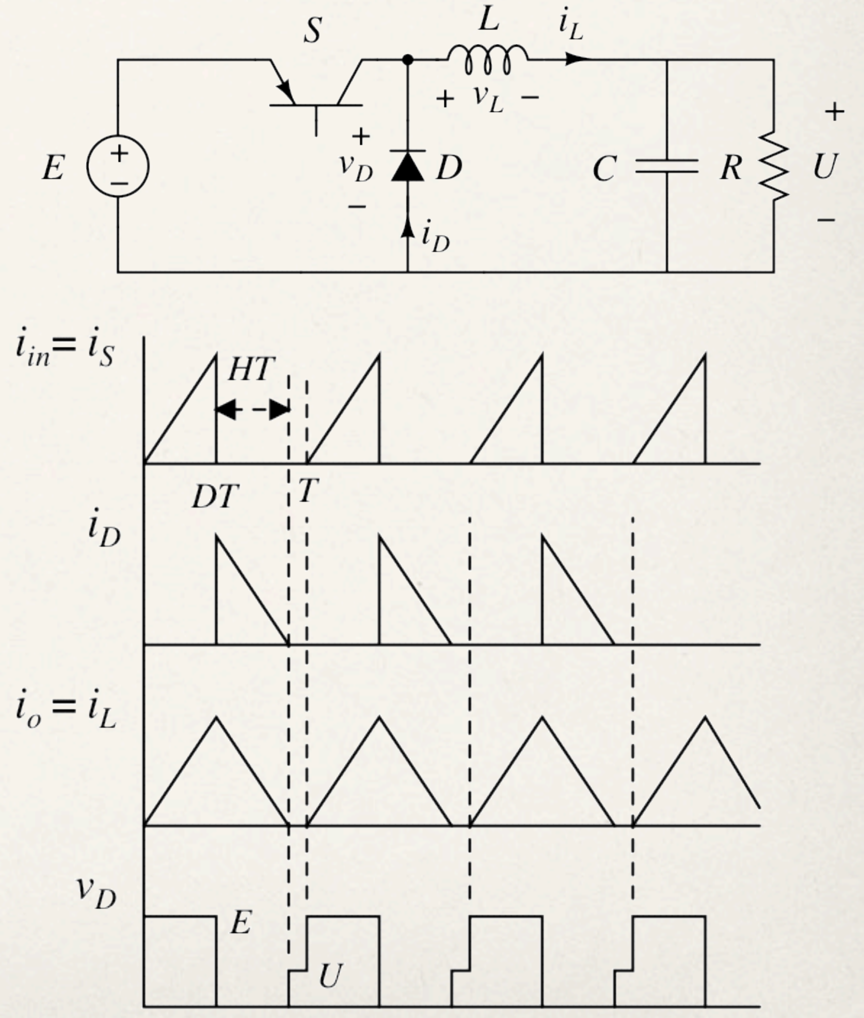
Discontinuous conduction mode

- Waveforms for the **buck converter in DCM**.
- Let the OFF time = *HT*;
  - and idling time = (1–*D*–*H*)*T*
- At steady state, the average output voltage, average inductor current, and peak inductor current can be found as

$$H = \frac{(E-U)D}{U}$$

$$I_{L,\text{average}} = \frac{I_{\max}(D+H)}{2} = \frac{U}{R}$$

$$U = \frac{2E}{1+\sqrt{1+\frac{8L}{RD^2T}}}$$



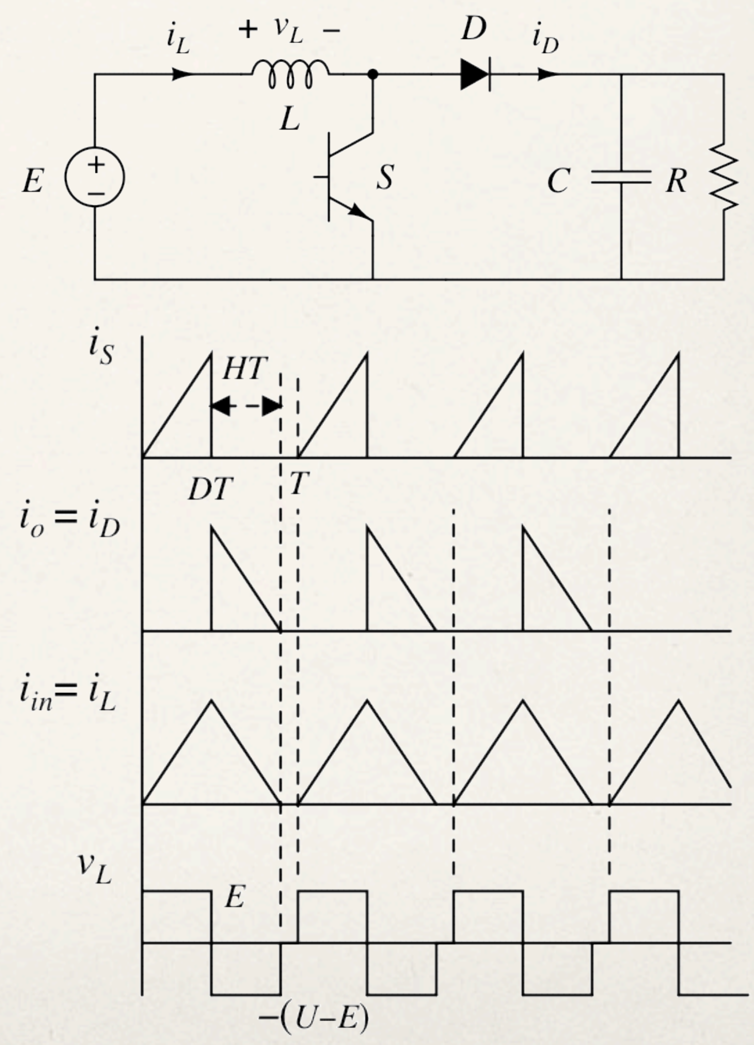
Discontinuous conduction mode

- For the **boost converter in DCM**, we have

$$H = \frac{ED}{U-E} = \frac{LI_{\max}}{(U-E)T}$$

$$I_{\text{in,average}} = \frac{(D+H)I_{\max}}{2}$$

$$U = \frac{E}{2}\left[1+\sqrt{1+\frac{2RD^2T}{L}}\right]$$



Mode boundary

- At the borderline, the inductor current just touches zero at the end of the period. There is no idling interval, and yet the inductor current has a momentarily zero value.
- For the **buck converter**, at the boundary of two modes,
  - the input power is $P_{\text{in}} = \frac{1}{2} I_{\max} D E$
  - the output power is $P_{\text{out}} = \frac{1}{4} I_{\max}^2 R$
- Also,

$$I_{\max} = \frac{DT(E-U)}{L}$$

- Equating the input power and output power, we get the boundary condition as

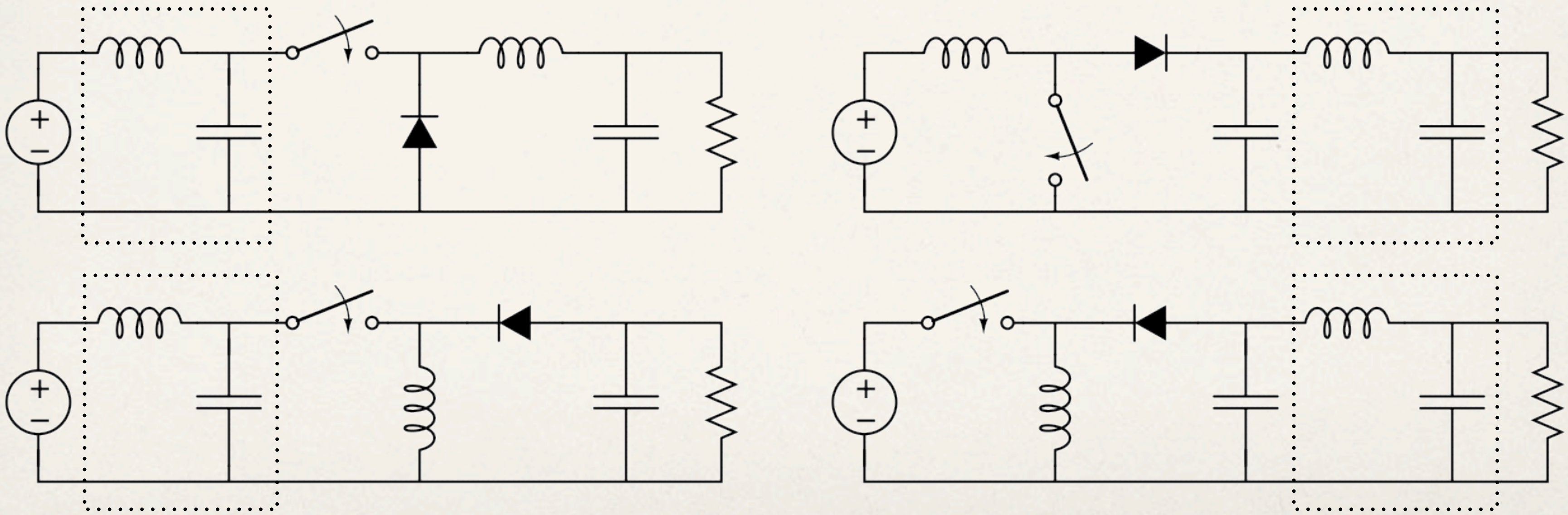
$$L_{\text{crit}} = \frac{(1-D)TR}{2}$$

Conditions for CCM: $L > L_{\text{crit}}$

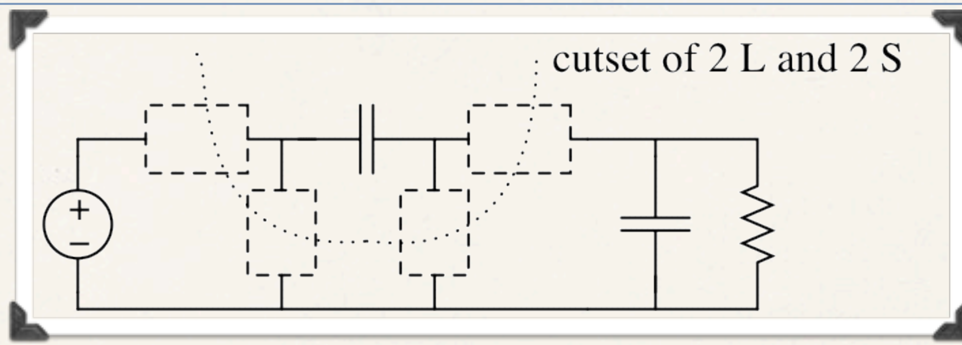
- Buck converter $$L_{\text{crit}} = \frac{(1-D)TR}{2}$$
- Buck-boost converter $$L_{\text{crit}} = \frac{(1-D)^2 TR}{2}$$
- Boost converter $$L_{\text{crit}} = \frac{(1-D)^2 DTR}{2}$$

Fourth order converters

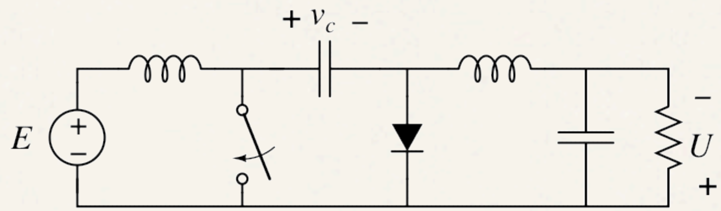
- The buck converter has pulsating input current.
- The boost converter has pulsating output current.
- The buck-boost converter has both pulsating input and output currents.
- We may add filter to the source side of the buck converter, and the load side of the boost converter. etc.
- The results are some higher order converters.



4th order converters with a cutset of 2 inductors and 2 switches

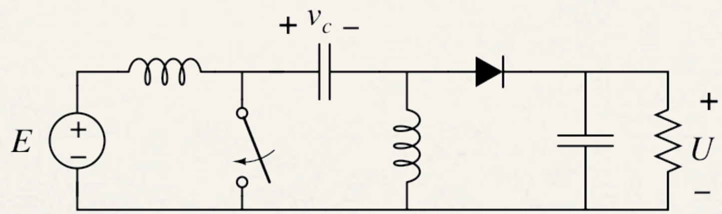


- Ćuk converter

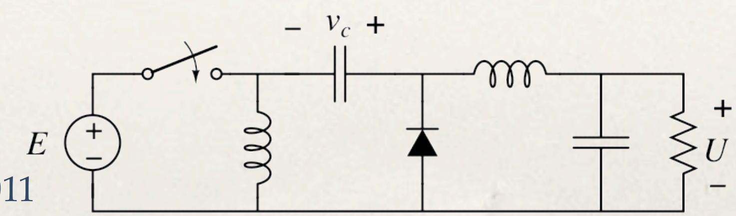


Both input and output current are non-pulsating!

- Zeta converter



- SEPIC converter

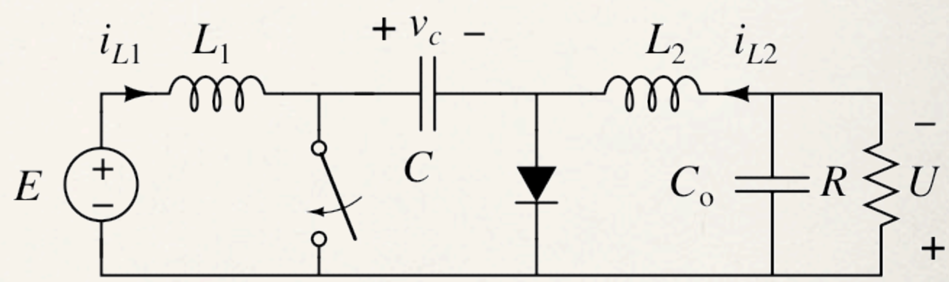


The Ćuk converter

- At steady state, it behaves like a cascade connection of a boost converter and a buck converter, with the storage capacitor as intermediate output. In CCM, we have

$$V_c = \frac{E}{1-D}$$

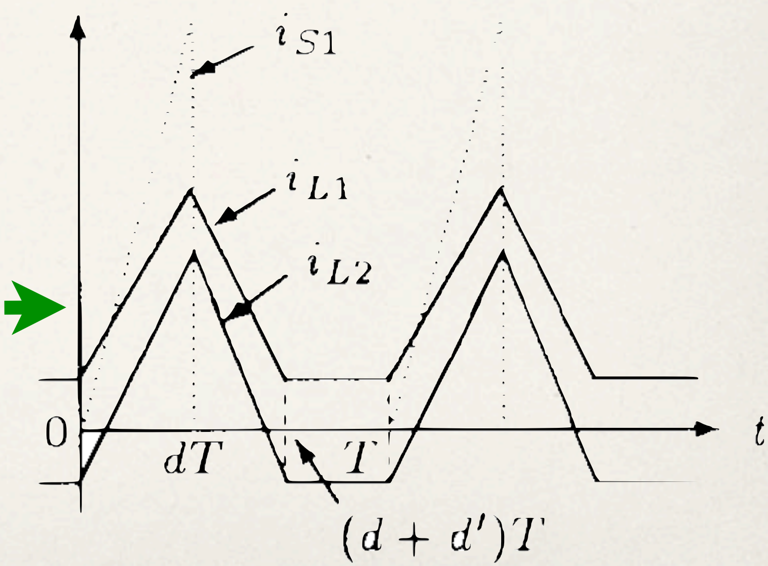
$$U = DV_c$$



- Hence,

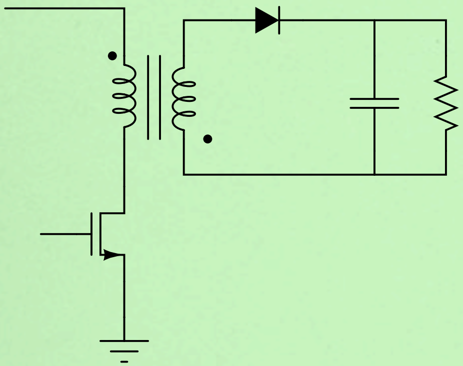
$$U = \frac{D}{1-D}E$$

- Of course, it can operate in DCM, but the inductor currents may not go to zero, though their sum is zero in the idling interval.
- It also has a special discontinuous capacitor voltage mode (DCVM).



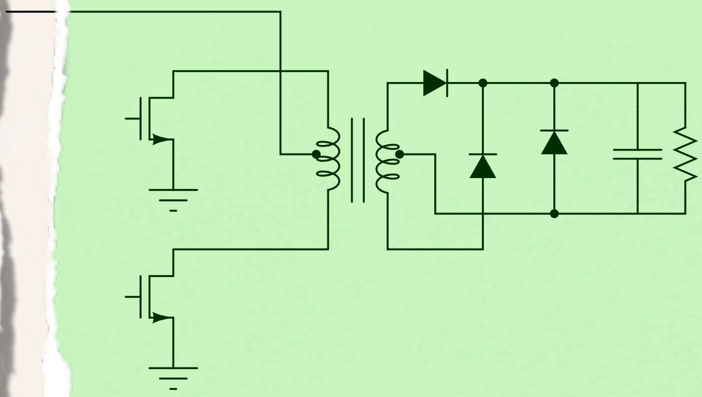
Transformer isolated versions

- Flyback converter (buck-boost)



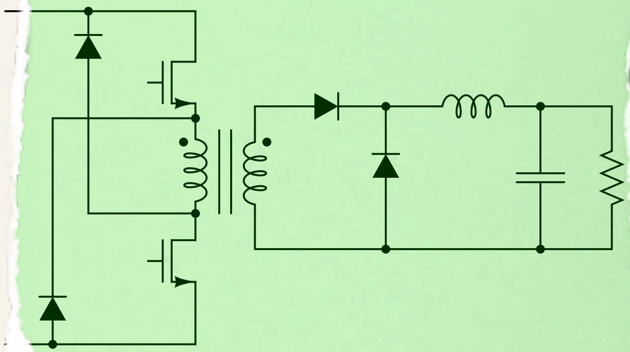
  - simple
  - storage inductor provided by transformer's magnetizing inductance

- Push-pull converter (buck)



  - Better core utilization as positive and negative flux polarities are used
  - Heat dissipation shared by two switches

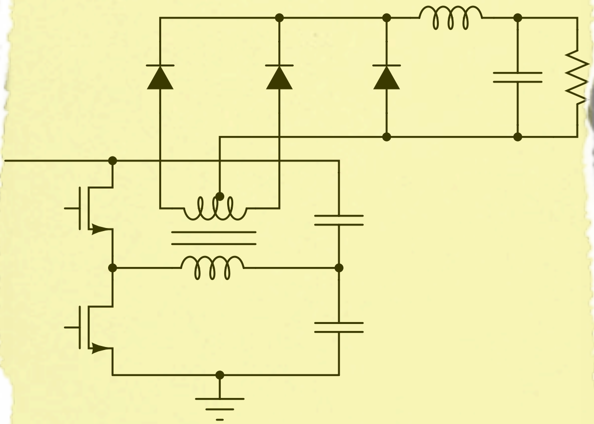
- Forward converter (buck)



  - Simple core reset
  - Limits d < 0.5
  - Reduced voltage stress

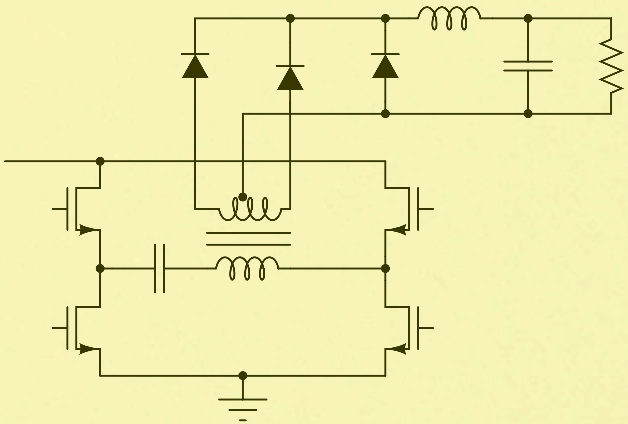
Transformer isolated versions

- Half-brdge converter (buck)



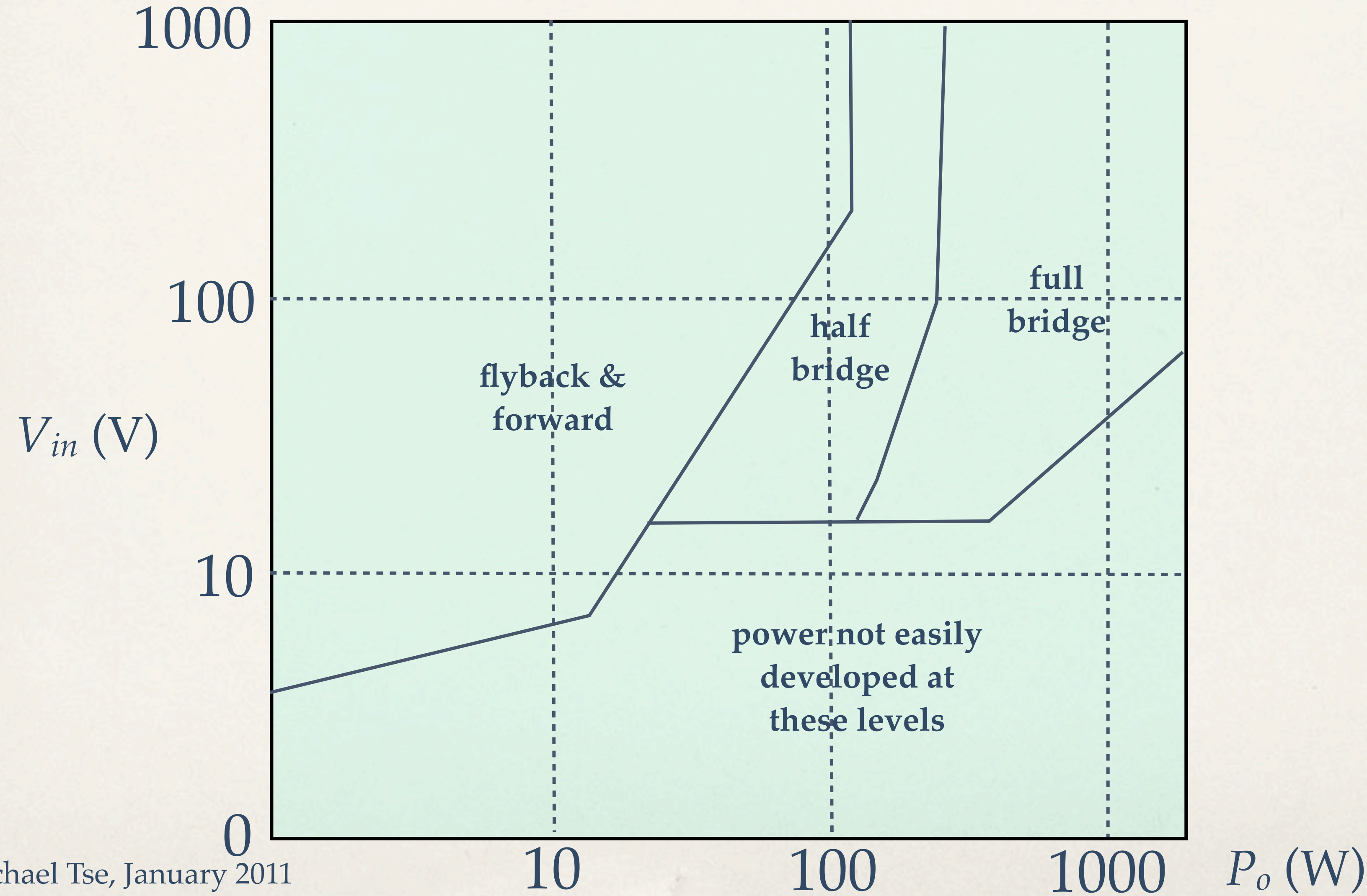
- Automatic core balance
- Voltage stress shared by two devices (low voltage ratings of devices)

- Full-brdge converter (buck)



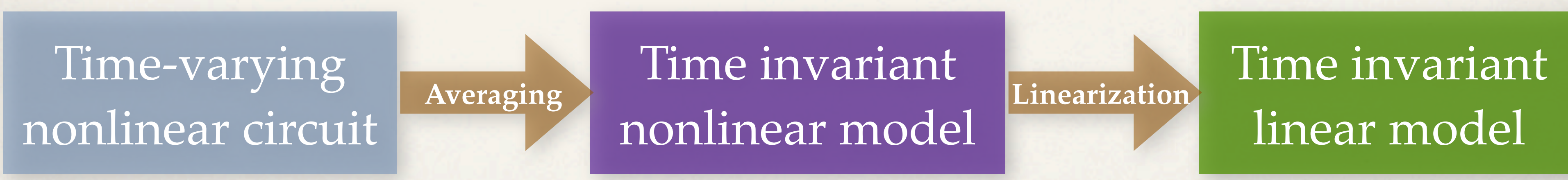
- Automatic core balance
- Switches operate in pairs
- Reduced peak current compared to half-bridge converter

General selection guideline



Models

- **Average models**
- IDEA:
  - Switching details are uninteresting
  - Focus on the low-frequency dynamics
    - Resulting models have no switch, but can be nonlinear
    - Resulting models can be linearized to produce small-signal models

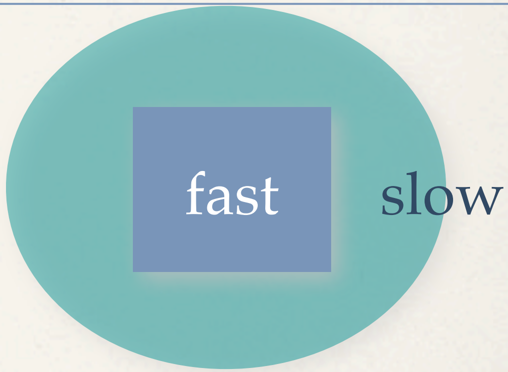


Dc/dc converters

Nonlinear large-signal model

Linear small-signal model

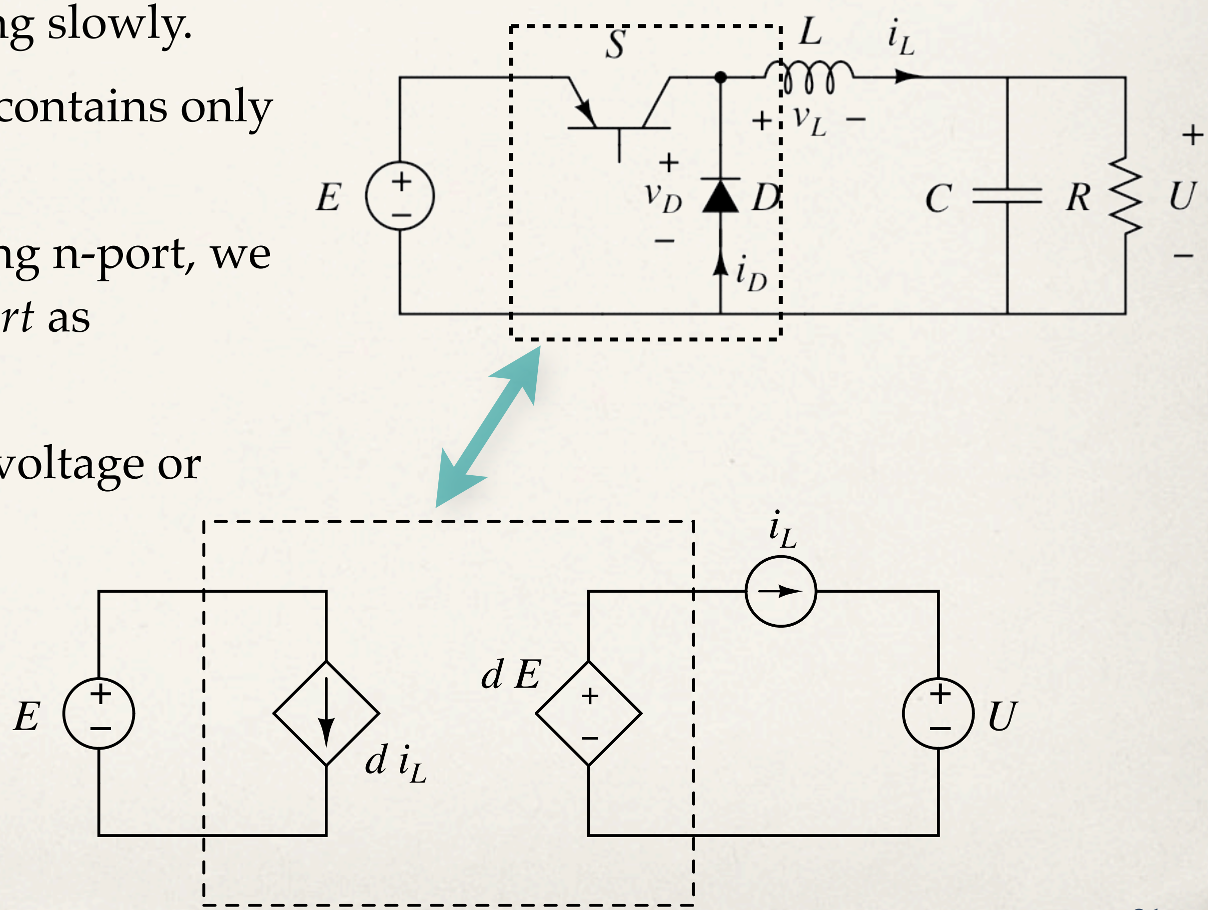
Averaging



- Separate the dc/dc converter into two parts:
    - switching n-port (fast part) and
    - the remaining slow part.
- Identify the ***switching n-port*** and replace it by equivalent average controlled sources.
    - **Essential idea:**
        - The switching n-port has high-frequency operation, and the rest can be considered very slow and hence can be regarded as "constant" while modeling the switching n-port.

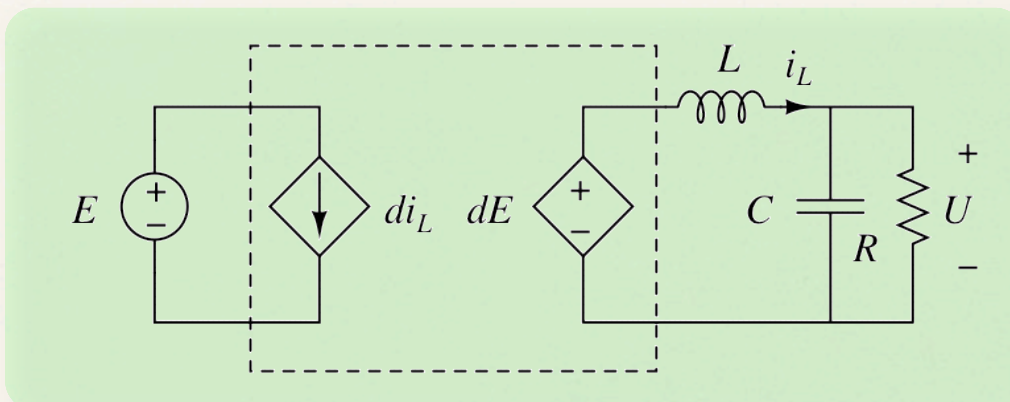
Example: buck converter in CCM

- In the buck converter in CCM, the inductor current is continuous and varying slowly.
- The switching n-port (fast part) contains only D and S.
- So, when we model this switching n-port, we may treat *the part outside the n-port* as "constant" source.
- Derive the average terminating voltage or current.

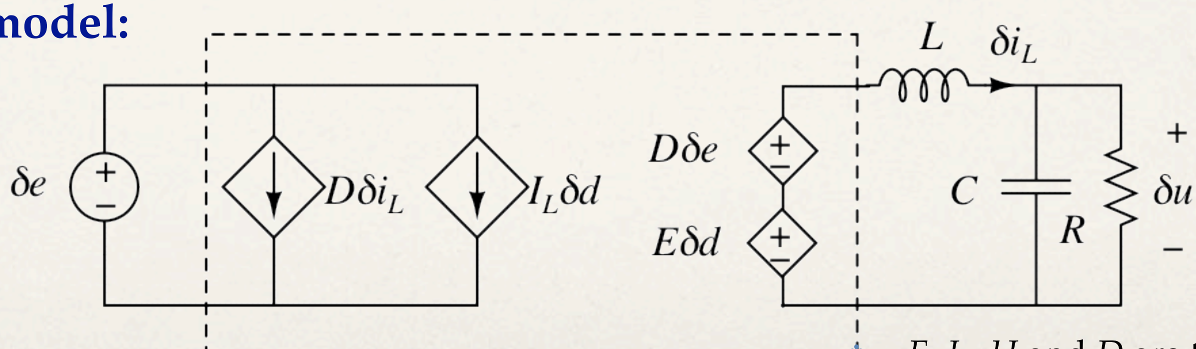


Example: buck converter in CCM

- **Finally, the inductor dynamics is resumed for analysis. The average model for CCM buck converter is**



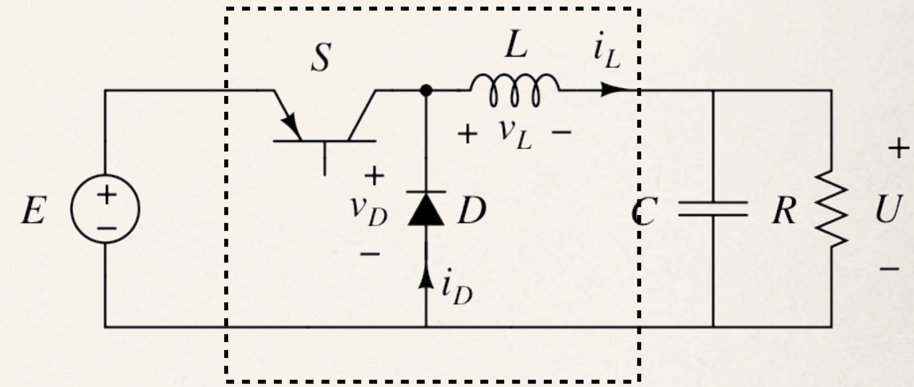
- **Small-signal model:**

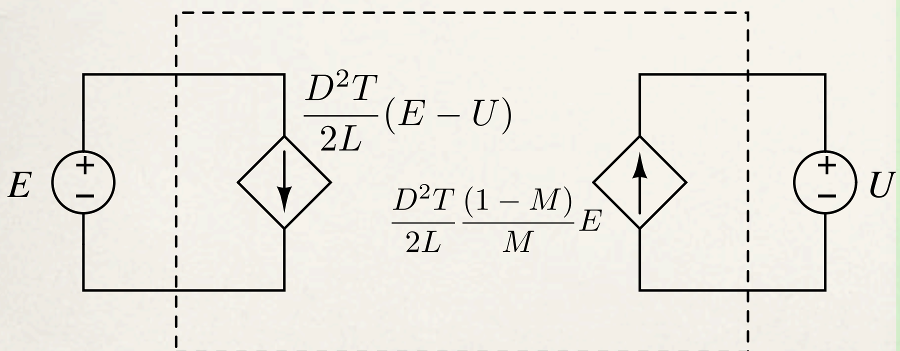


- E, I_L, U and D are the steady state values.
- δx is the small-signal value of x.

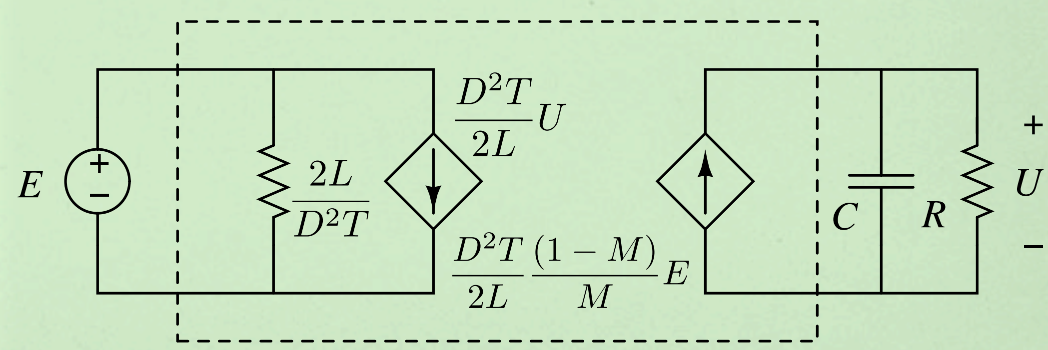
Example: buck converter in DCM

- In the buck converter in DCM, the inductor is absorbed in the switching n-port (fast part).
- Again, when we model this switching n-port, we can treat *the part outside the n-port* as a "constant" source.
- Derive the average terminating voltage or current.

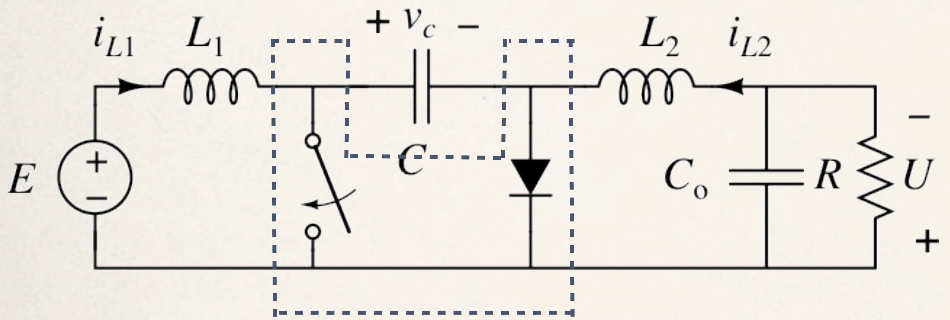


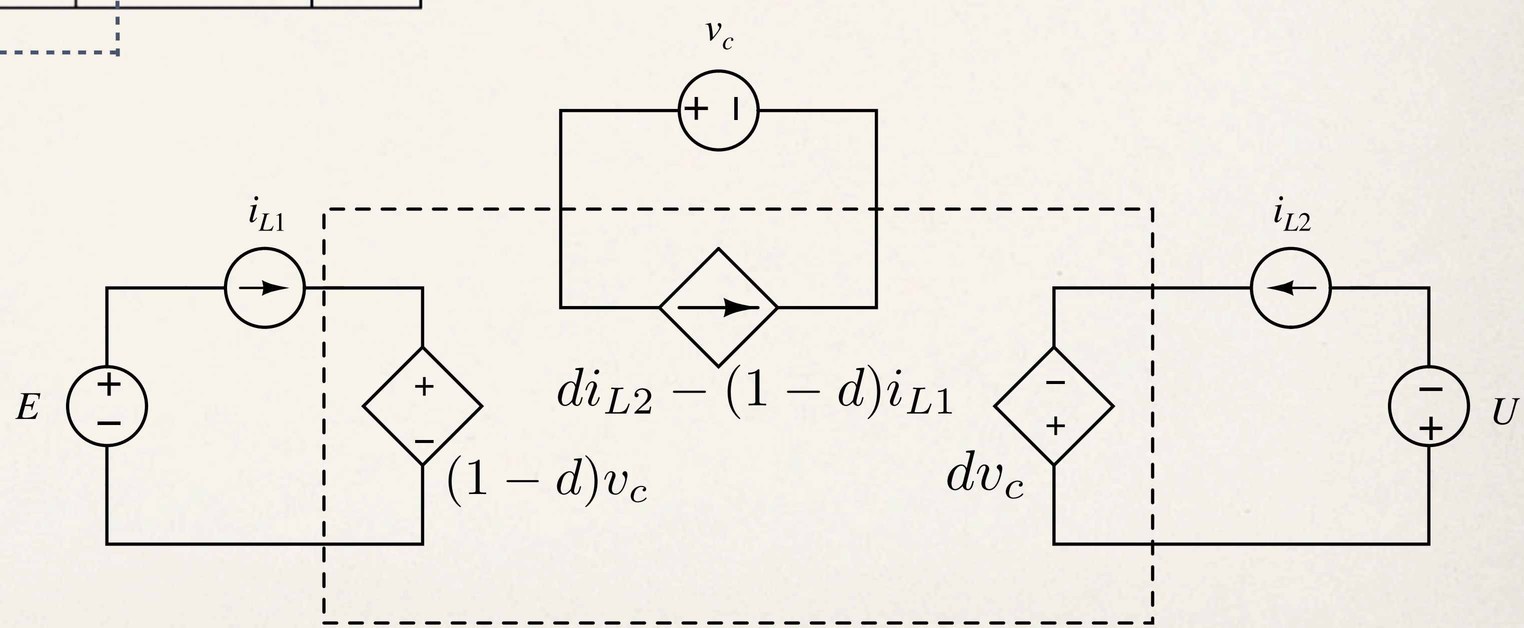


where $M = \frac{U}{E}$



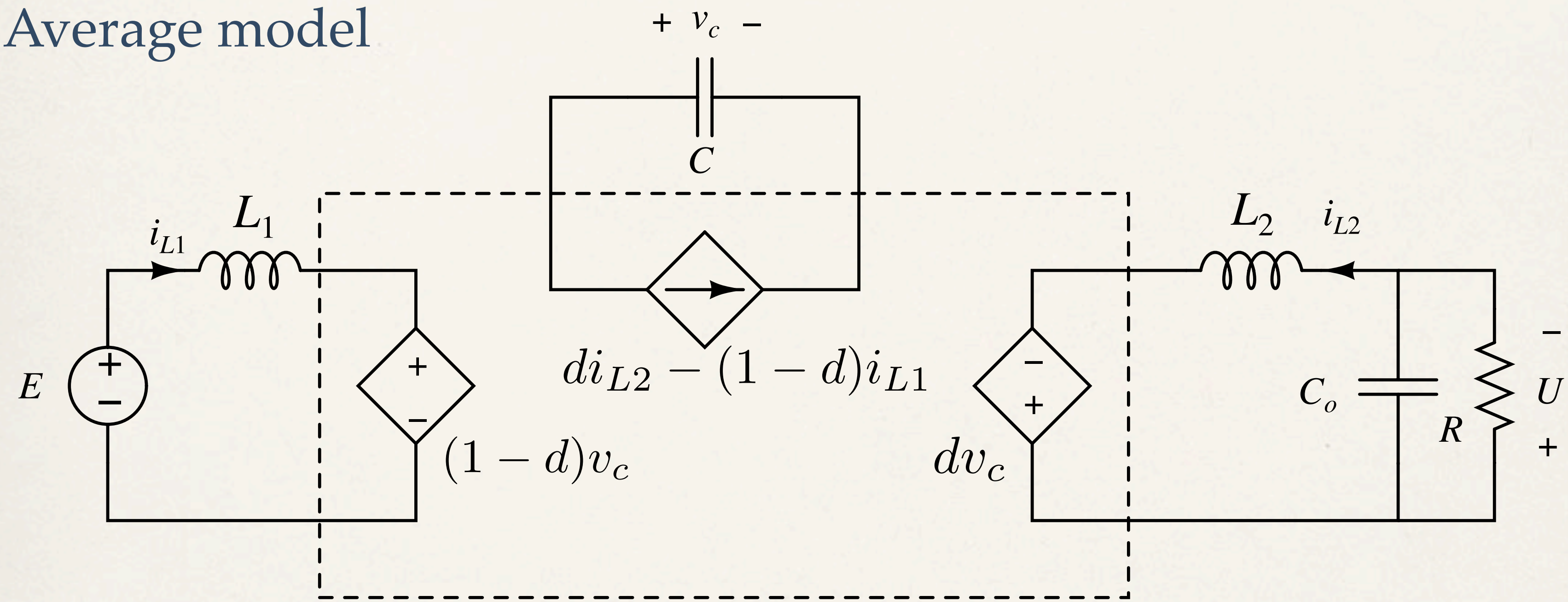
Example: Cuk converter in CCM





Example: Cuk converter in CCM

Average model



Small-signal model of the buck converter

- From the model, we identify two inputs:

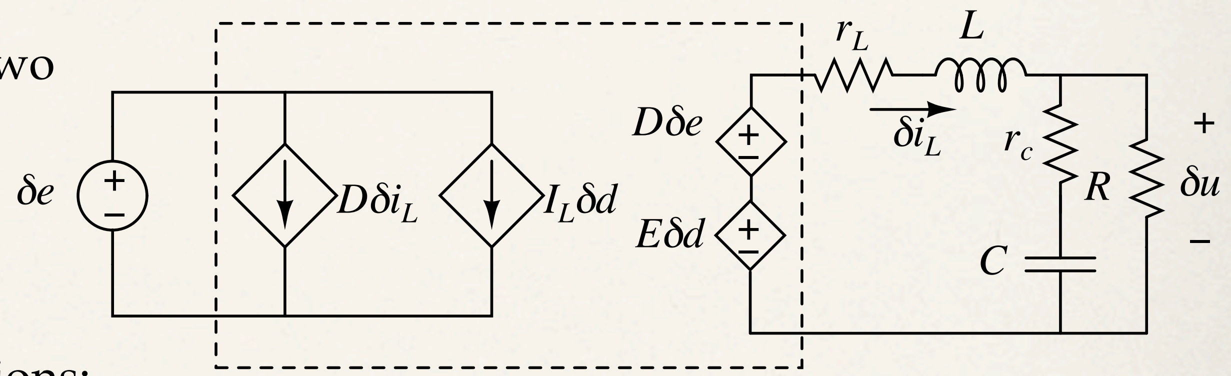
  $$\delta e \text{ and } \delta d$$

- The output is δu.
- We can develop transfer functions:
  - Control-to-output t/f:

$$\frac{\delta u}{\delta d} = \frac{U}{D}\left[\frac{1+sCr_c}{1+s\left((r_c+r_L\|R)C+\frac{L}{r_L+R}\right)+s^2LC\frac{r_c+R}{r_L+R}}\right]$$

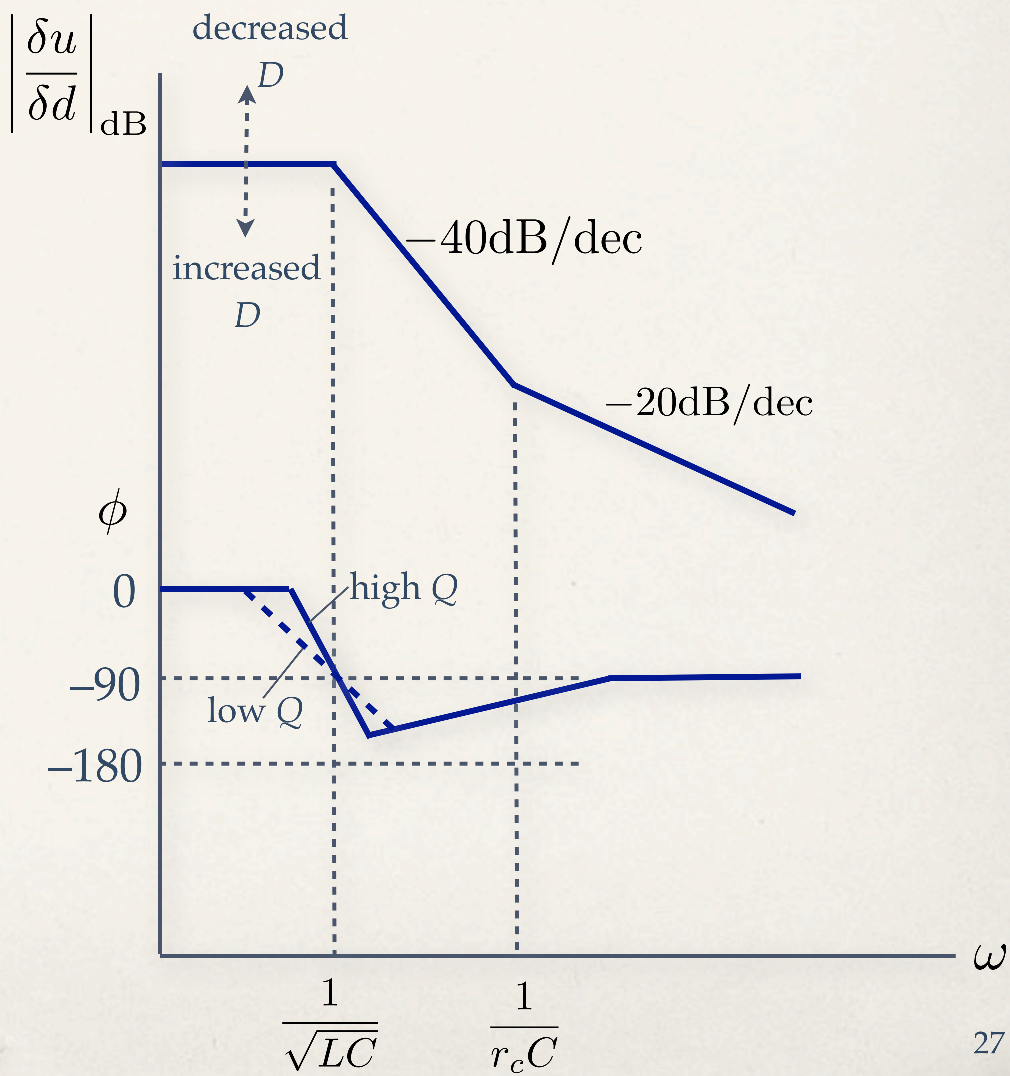
  - Input-to-output t/f:

$$\frac{\delta u}{\delta e} = \frac{DR}{r_L+R}\left[\frac{1+sCr_c}{1+s\left((r_c+r_L\|R)C+\frac{L}{r_L+R}\right)+s^2LC\frac{r_c+R}{r_L+R}}\right]$$



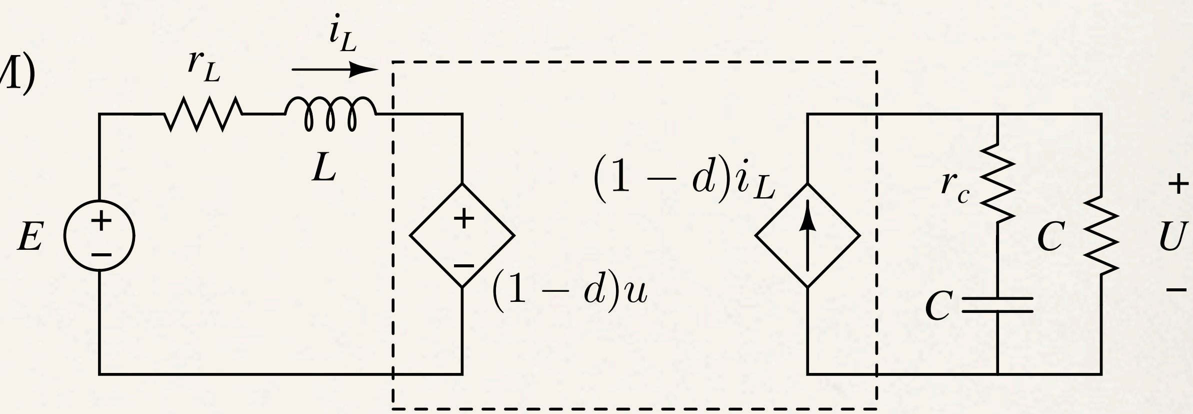
Small-signal dynamics of the buck converter

- BUCK CONVERTER
  - When ESRs are included, a zero at $-1/r_cC$ appears. Thus, a +20dB/dec response is expected from $1/2\pi r_cC$ Hz.
  - A pair of complex poles at fixed locations. Thus, a –40dB/dec response is expected from $1/2\pi LC$ Hz.

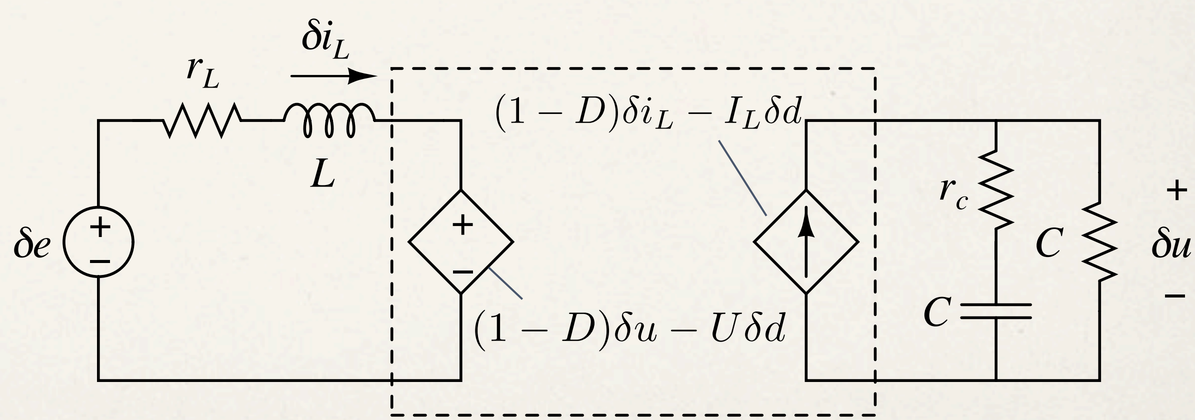


Small-signal model of the boost converter

- BOOST CONVERTER (CCM)
- Average model (nonlinear):



- Linear small-signal model:



Transfer functions for the boost converter

- Control-to-output t/f:

$$\frac{\delta u}{\delta d} = \left[\frac{U}{(1-D)R'}\right]\left[\frac{(1-D)^2R^2}{r_C+R} - r_L\right]\left[\frac{(1+sr_cC)\left(1-\frac{sL(r_L+R)}{(1-D)^2R^2}\right)}{1+s\left(\frac{L}{R'}+\frac{(r_LR+r_cr_L+(1-D)r_cR)C}{R'}\right)+s^2LC\left(\frac{r_c+R}{R'}\right)}\right]$$

where $R' = \dfrac{(1-D)^2R^2}{R+r_c} + (1-D)(r_c\|R) + r_L$

- Input-to-output t/f:

$$\frac{\delta u}{\delta e} = \left[\frac{(1-D)R}{R'}\right]\left[\frac{(1+sr_cC)}{1+s\left(\frac{L}{R'}+\frac{(r_LR+r_cr_L+(1-D)r_cR)C}{R'}\right)+s^2LC\left(\frac{r_c+R}{R'}\right)}\right]$$

Small-signal response of the boost converter

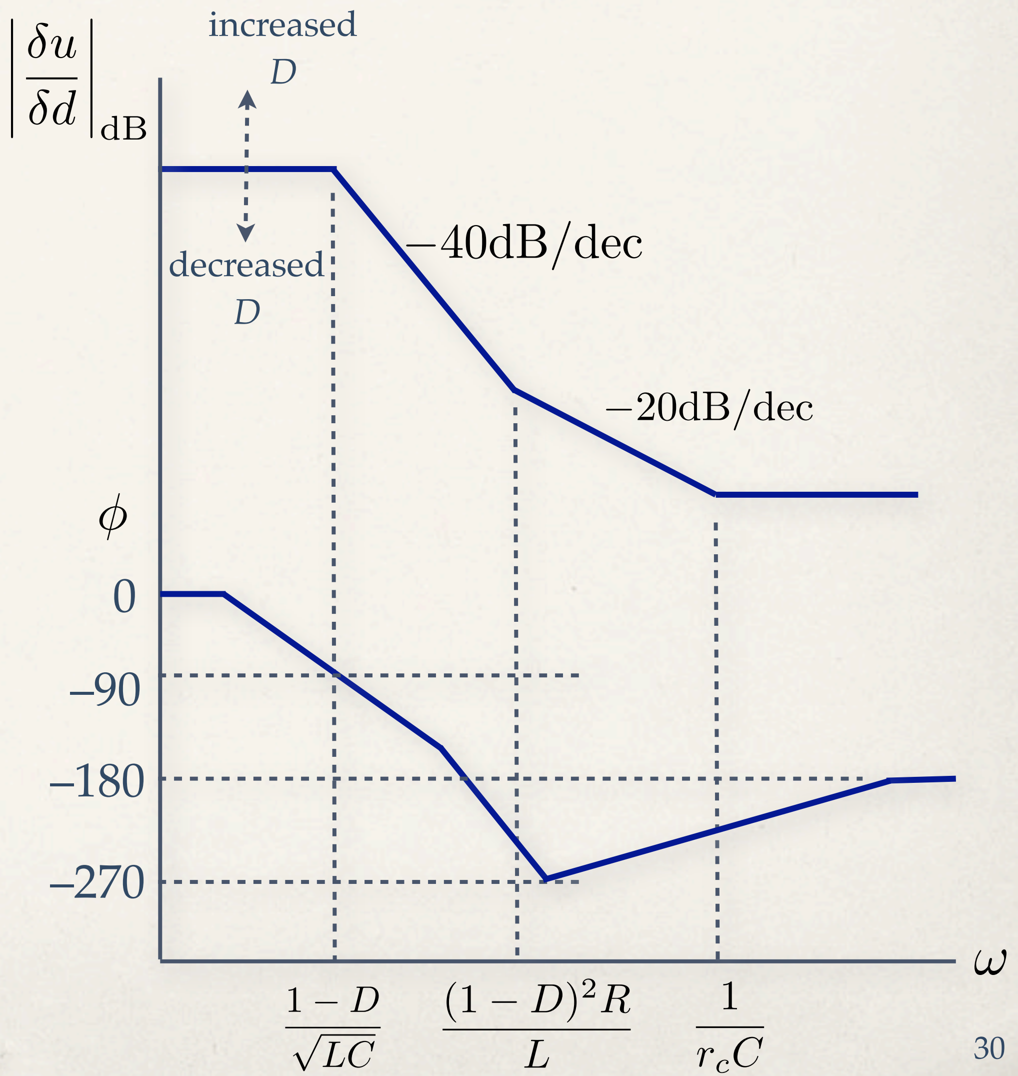
- A right-half-plane zero exists in the control-to-output transfer function of the boost converter!

$$\omega_{\mathrm{RHP}} = \frac{1}{L}\left[\frac{(1-D)^2R^2}{R+r_c} - r_L\right] \approx \frac{(1-D)^2R}{L}$$

- The complex poles are not fixed, but depend on the duty cycle D.

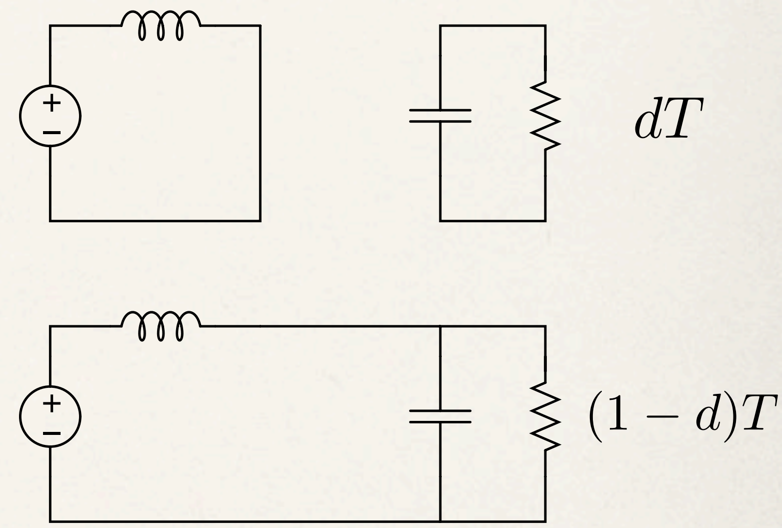
$$\omega_s = \sqrt{\frac{R'}{(r_c+R)LC}} \approx \frac{1-D}{\sqrt{LC}}$$

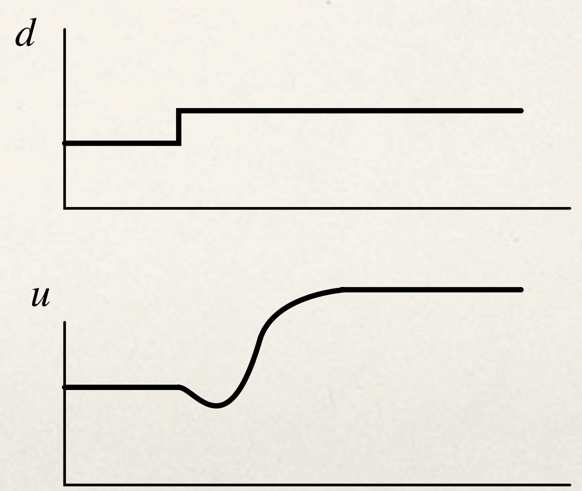
- The ESR zero still exists at $1/2\pi r_c C$ Hz.



Right-half-plane zero or Non-minimum phase response

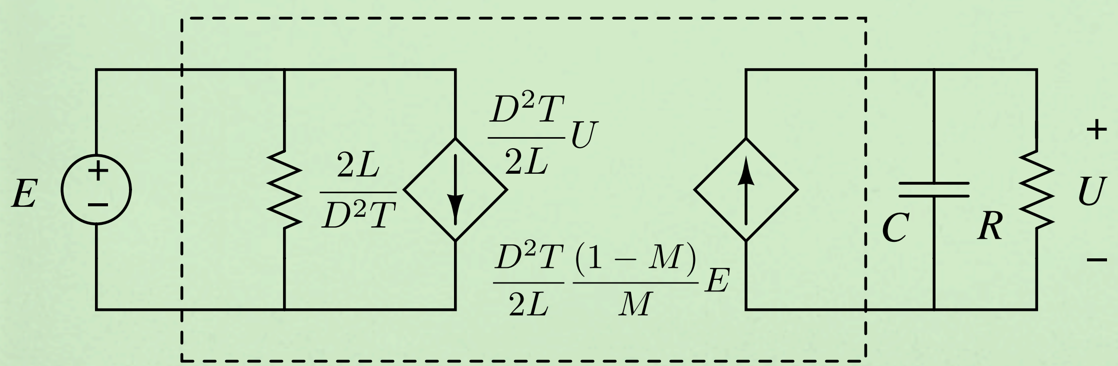
- In the time domain, a non-minimum phase response is characterize an initial momentarily drop in output when a step increase in duty cycle is applied. The output eventually rises.
- The physical origin can be easily understood from the structure of the boost converter.
  - Increasing the duty cycle means that the inductor is charged for a longer interval. This makes the output capacitor discharge for a longer time. But as soon as more current is supplied to the output network in subsequent cycles, the output eventually increases.
- ***This phenomenon occurs in boost and buck-boost (flyback) converters.***



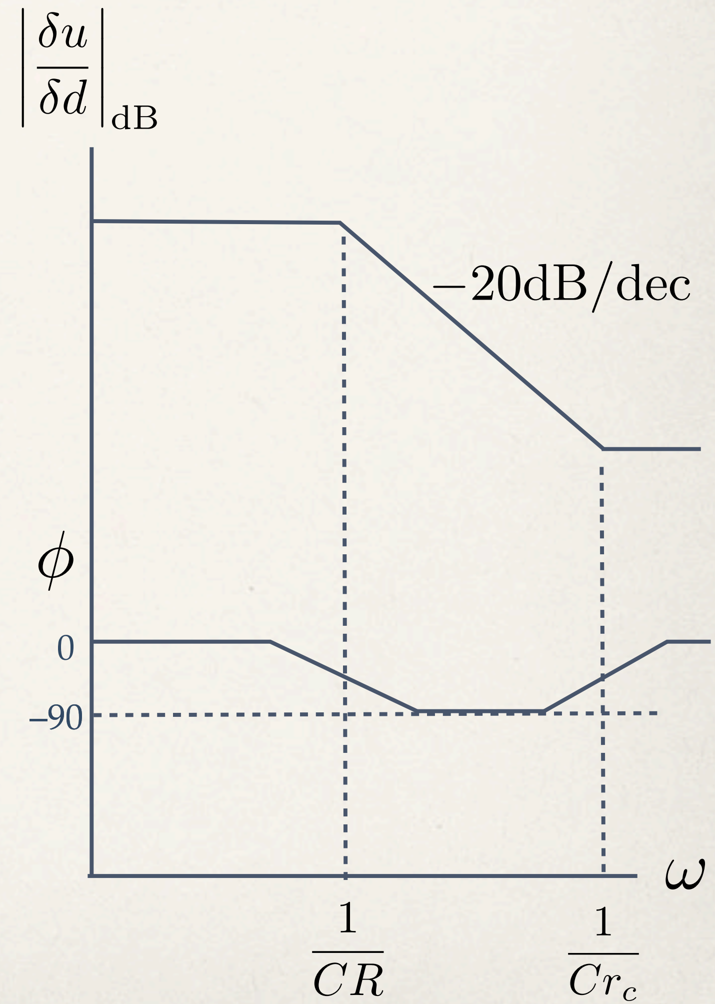


Note on DCM converters

- Essentially first-order, because inductor current assumes zero value periodically, and its average becomes devoid of dynamics.
- The dynamics is a single-pole response, roll-off at $1/CR$. Of course ESR zero still exists.
- Easy control!

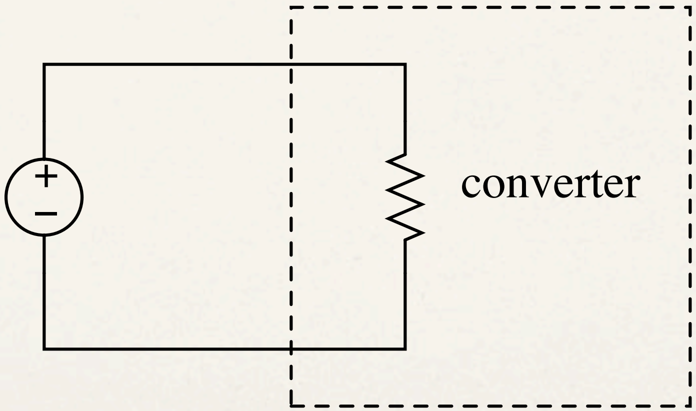


Buck converter average model



Probing further

- How does the input like look?
- Can it become resistive? Under what condition?
- Any application if it has a resistive input?
  - Cheap and simple power-factor-correction converter!



Conclusion

- Simple converters: buck, buck-boost and boost converters
- Fourth order converters: Cuk converter
- Transformer isolated converters
- Average models
  - Switching details removed
  - Nonlinear models for analysis
  - Linearization to yield small-signal models
    - Transfer functions
    - Dynamic responses
    - Converters with RHP zero need special control strategies.

References

1. R.D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," *IEEE Power Electronics Specialists Conference*, pp. 18–34, 1976.
2. R.P. Severn and G.E. Bloom, *Modern DC-to-DC Switchmode Power Converter Circuits*, Van Nostrand Reinhold, 1985.
3. C.K. Tse, Y.S. Lee and W.C. So, "An Approach to Modelling DC-DC Converter Circuits Using Graph Theoretic Concepts," *Int. J. Circuit Theory and Applications*, vol. 21, no. 4, pp. 371–384, July-August, 1993.
4. N. Mohan, T.M. Undeland and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, Wiley, 2003.