Analysis and Control of Power Converters

C.K. Michael Tse

Hong Kong Polytechnic University

Cover illustration:
Tan, Lai and Tse, *Sliding Mode Control of Switching Power Converters: Techniques and Implementation*, CRC Press, 2011

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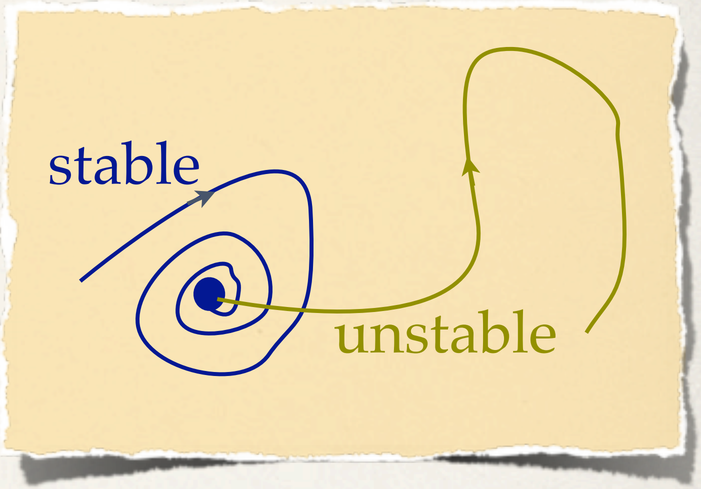
- Instability
  - Practical meanings
  - Usefulness of bifurcation analysis
- On analysis
  - Case study: boost converter’s stability analysis
- On control
  - Case study: parallel converters
    - Current-mode control versus voltage-mode control
    - Connection configuration affects the choice of control strategy

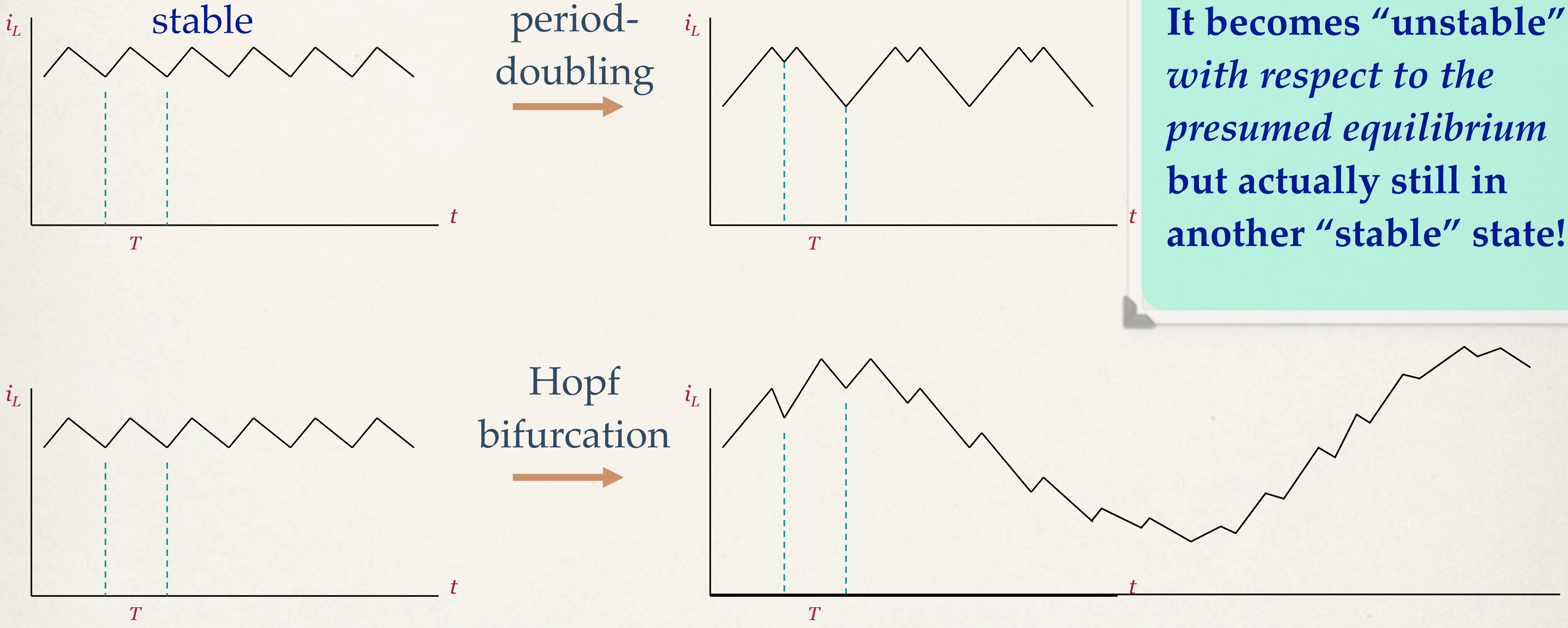
The meaning of "instability"

- **Instability from linear theory**
  - When a system converges to an equilibrium point under any disturbance, it is STABLE.
  - When a system cannot converge to the equilibrium point, it is unstable.
    - When it is unstable, it moves away from the equilibrium and goes to infinity.



- **Practical instability**
  - When a system is unstable, it fails to converge to the presumed equilibrium point, but it actually must have moved to a new steady-state equilibrium which is usually not wanted. There is no infinity!

Getting unstable = assuming a new equilibrium



stable

period-doubling

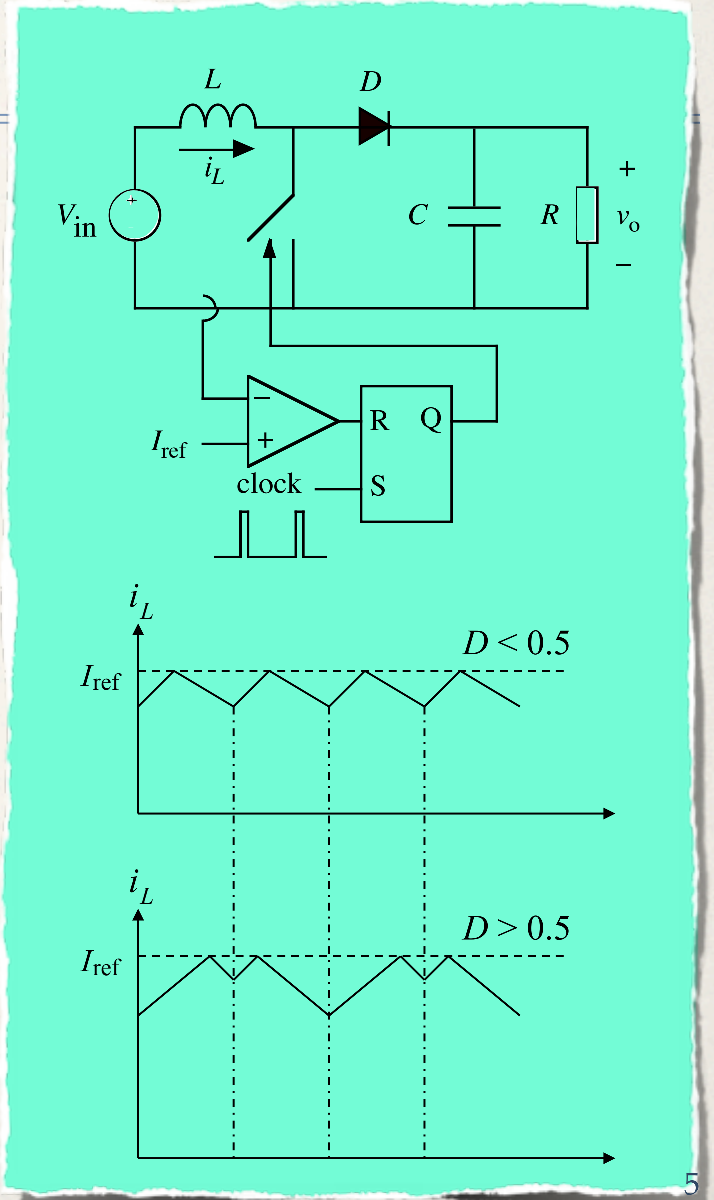
Hopf bifurcation

It becomes "unstable" ***with respect to the presumed equilibrium*** **but actually still in another "stable" state!**

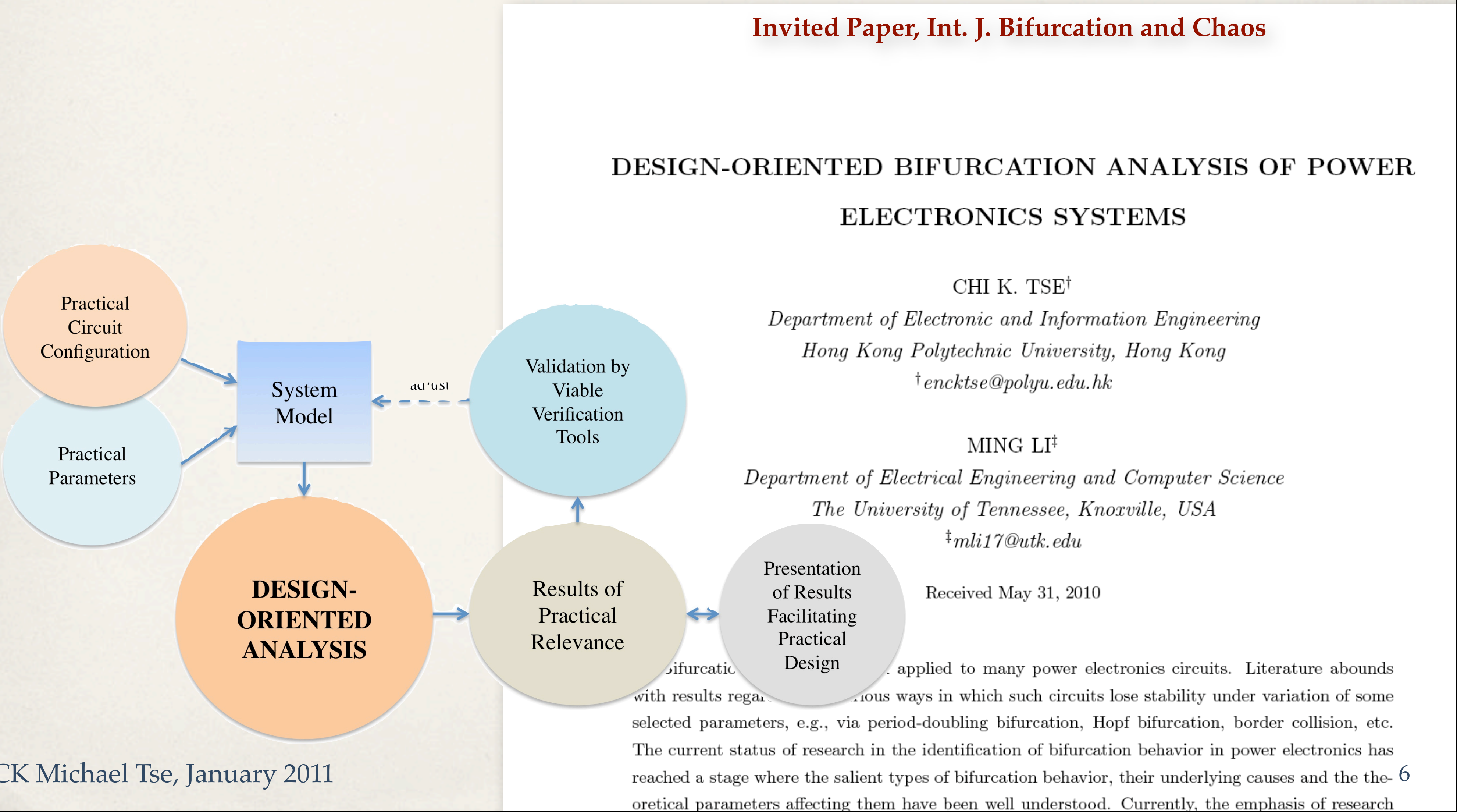
The right questions

- Unstable? *With respect to which operating state?*
- Under what conditions the system become unstable?
- When it loses stability, where would it go then (what is the "new" state)?
    - Conditions of the "new" state: would it make the operation undesirable? e.g., changes in voltage stress and current stress.

- **Study of Bifurcation**
    - Bifurcation = Change in state (behavior) when some parameters are changed.
    - For example, in a current-mode controlled converter, when the duty cycle goes beyond 0.5, the periodic operation loses stability, and it goes to a subharmonic oscillation. This bifurcation is called **period-doubling**. Note again that the system is still "stable" strictly!



Practical bifurcation analysis



Invited Paper, Int. J. Bifurcation and Chaos

DESIGN-ORIENTED BIFURCATION ANALYSIS OF POWER ELECTRONICS SYSTEMS

CHI K. TSE[†]
Department of Electronic and Information Engineering
Hong Kong Polytechnic University, Hong Kong
[†]*encktse@polyu.edu.hk*

MING LI[‡]
Department of Electrical Engineering and Computer Science
The University of Tennessee, Knoxville, USA
[‡]*mli17@utk.edu*

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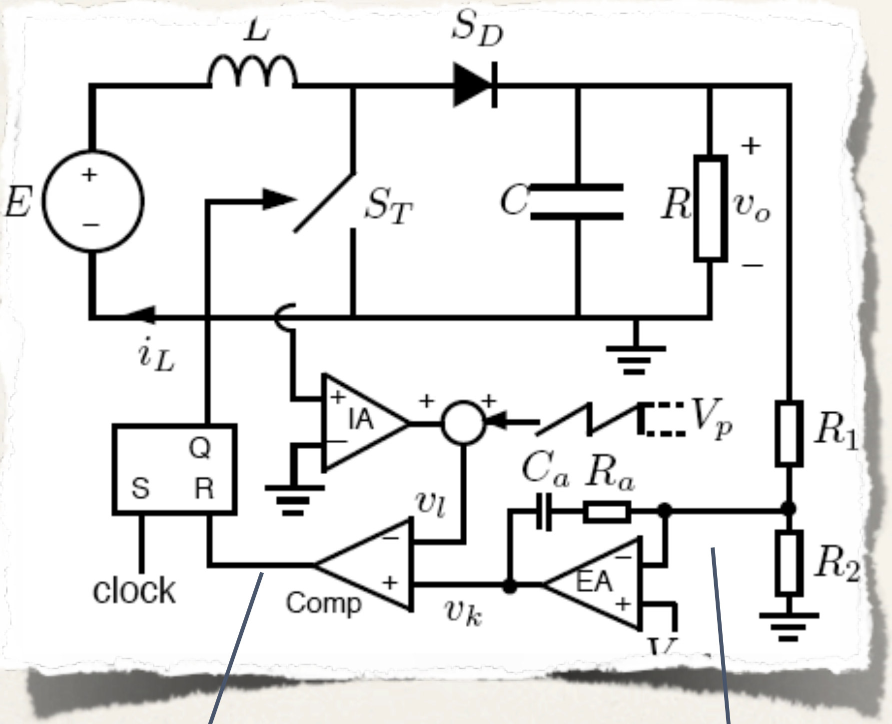
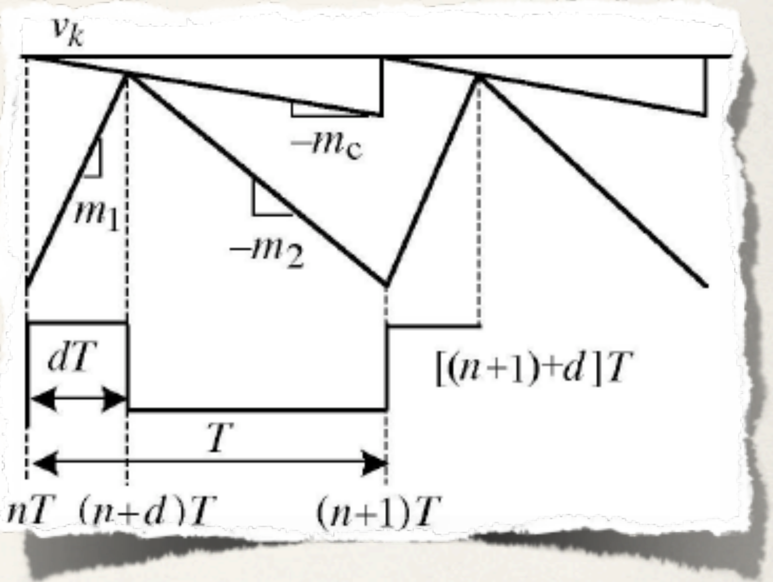
bifurcatic applied to many power electronics circuits. Literature abounds with results rega ious ways in which such circuits lose stability under variation of some selected parameters, e.g., via period-doubling bifurcation, Hopf bifurcation, border collision, etc. The current status of research in the identification of bifurcation behavior in power electronics has reached a stage where the salient types of bifurcation behavior, their underlying causes and the theoretical parameters affecting them have been well understood. Currently, the emphasis of research

Case study 1: on analysis

- Current-mode controlled boost converter





current waveform

inner current loop (fast)

outer voltage loop (slow)

Parameters affecting stability

- **Main parameters**
  - Affecting fast-scale bifurcation (inner loop instability problem)
    - Rising slope of inductor current $m_1 = E/L$
    - Compensation slope m_c
  - Affecting slow-scale bifurcation (outer loop instability problem)
    - Voltage feedback gain g
    - Feedback time constant τ_f

Previous results

- Previous studies
  - The two kinds of bifurcation were studied and reported ***separately***.
  - Fast-scale bifurcation focuses on the ***period-doubling*** phenomenon, assuming that the outer loop is very slow and essentially provides a constant reference current for the inner loop.
  - Slow-scale bifurcation focuses on the ***Hopf bifurcation*** as the feedback gain and bandwidth are altered, assuming that the inner is stable.

  - Both are practical phenomena.

What can happen in a boost converter?

- Get a quick glimpse
  - Cycle-by-cycle simulation of the system with the exact piecewise switched model. Circuit components are as follows:

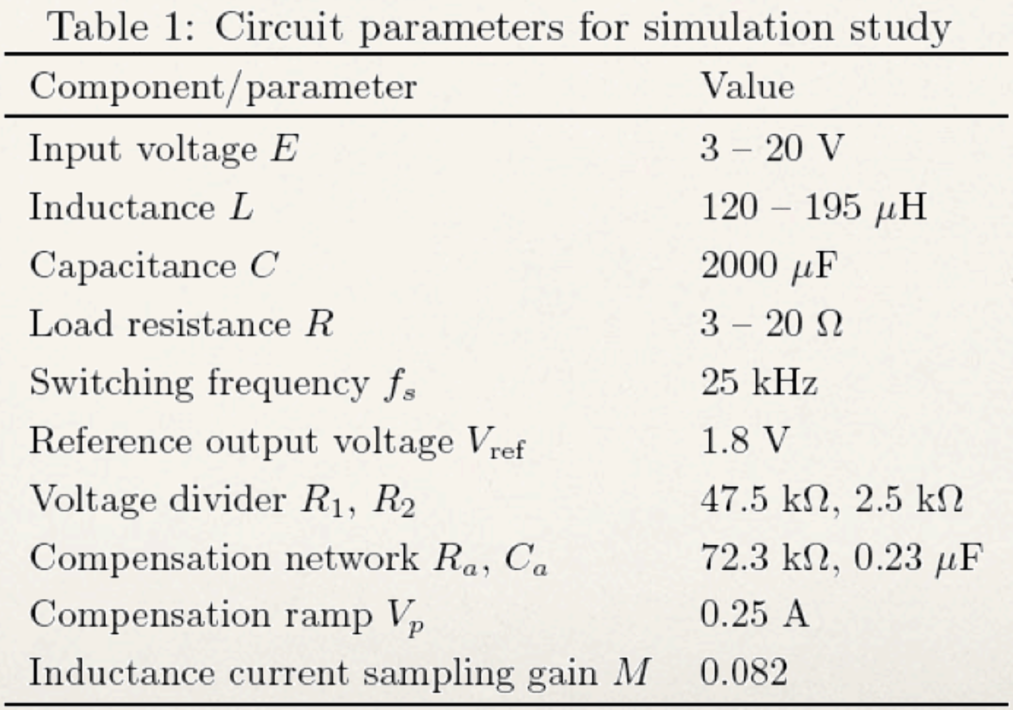
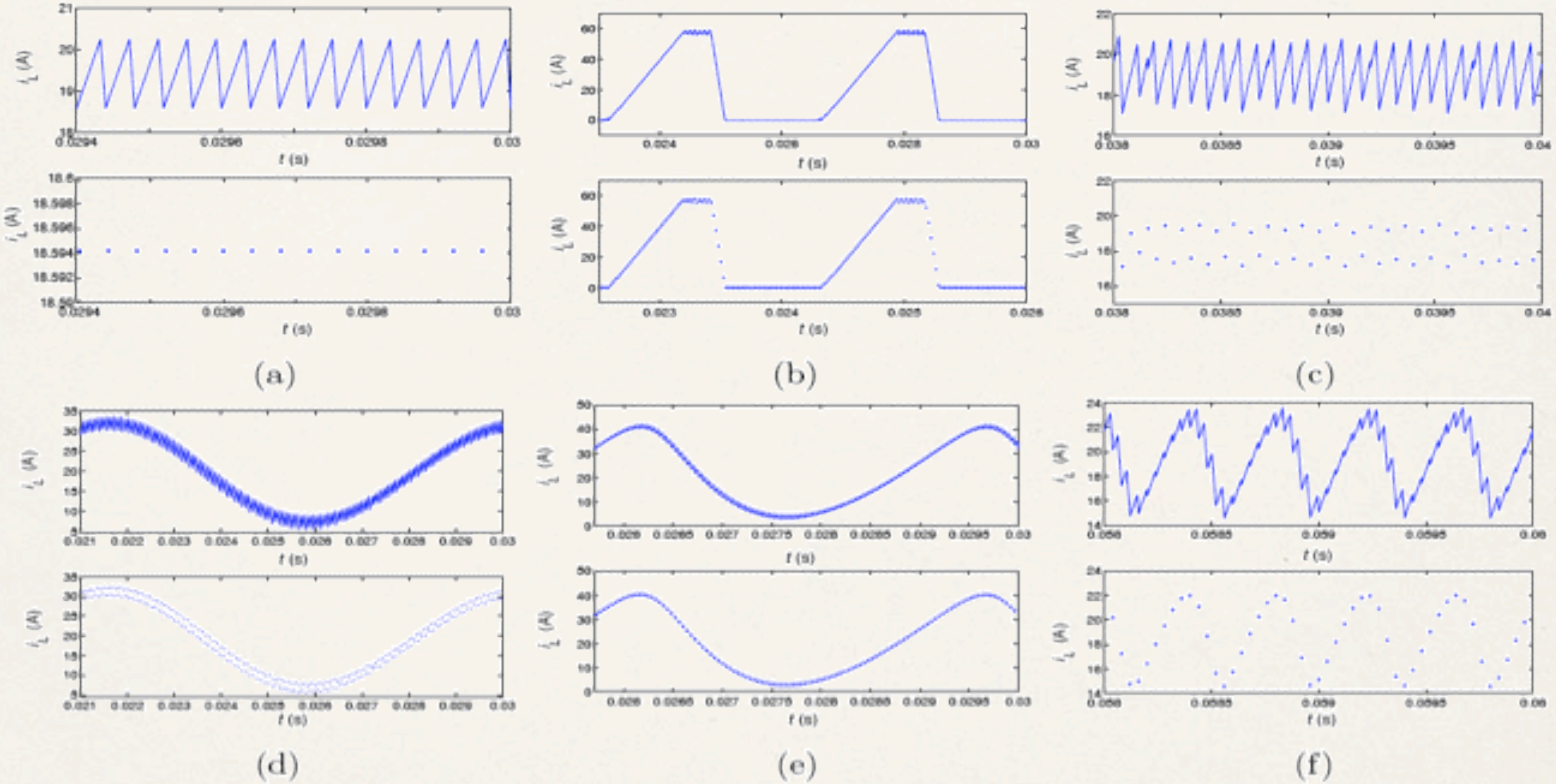


Table 1: Circuit parameters for simulation study

Component/parameter	Value
Input voltage E	3 – 20 V
Inductance L	120 – 195 μH
Capacitance C	2000 μF
Load resistance R	3 – 20 Ω
Switching frequency f_s	25 kHz
Reference output voltage V_{ref}	1.8 V
Voltage divider R_1, R_2	47.5 kΩ, 2.5 kΩ
Compensation network R_a, C_a	72.3 kΩ, 0.23 μF
Compensation ramp V_p	0.25 A
Inductance current sampling gain M	0.082

Simulations

Quick glimpse at changing g and τ_f



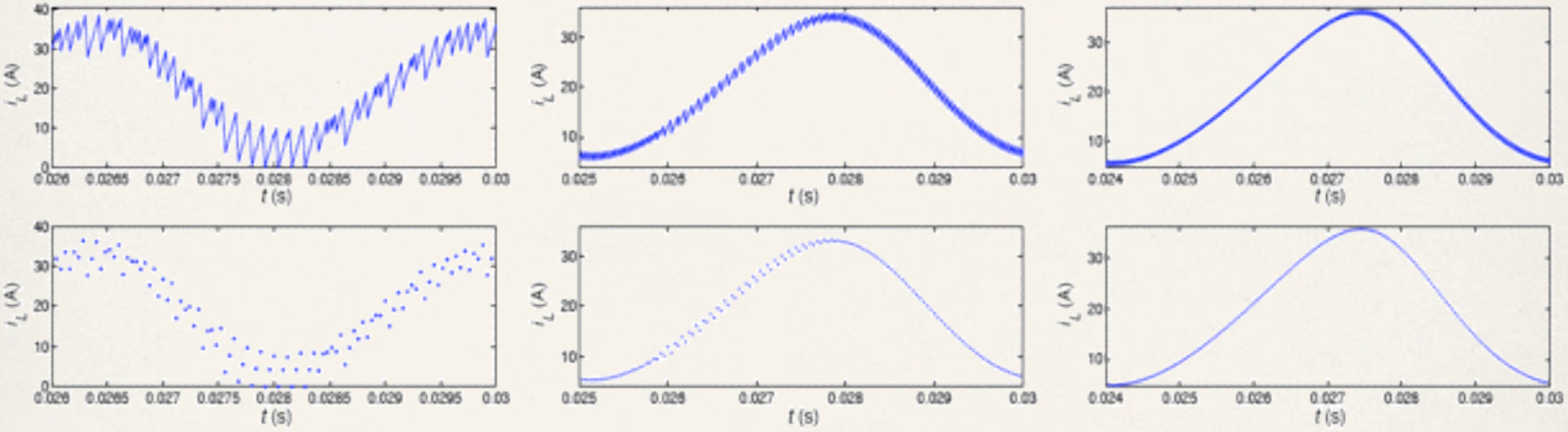
(a) (b) (c)

(d) (e) (f)

Figure 2: Simulated behaviors for different feedback gain $g = R_a/R_1$ and time constant $\tau_f = R_1 C_a$, with $1/m_1 = 19.835 \times 10^{-6}$ s/A, $m_e = 6.25 \times 10^3$ A/s. Upper trace: actual waveforms, lower trace: sampled-data waveforms. (a) Stable periodic operation with $g = 1.522$ and $\tau_f = 0.5225$ ms, (b) saturated operation with $g = 1.522$ and $\tau_f = 0.475$ ms, (c) fast-scale bifurcation with $g = 0.1$ and $\tau_f = 10.925$ ms, (d) coexisting (interacting) fast and slow-scale bifurcation with $g = 0.1$ and $\tau_f = 2.09$ ms, (e) slow-scale bifurcation $g = 0.8$ and $\tau_f = 0.492$ ms, (f) slow-scale bifurcation with $g = 2.4$ and $\tau_f = 7.125$ ms.

Simulations

Quick glimpse at changing m_1 and τ_f

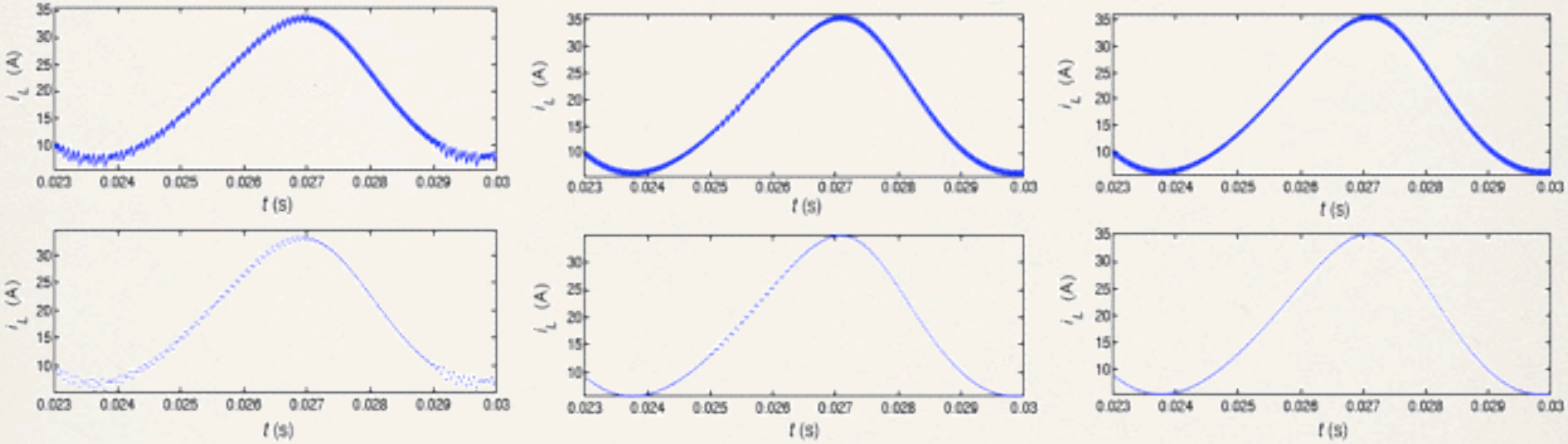


(a) (b) (c)

Figure 3: Simulated behaviors for different values of m_1 and τ_f, with $g = 0.4$ and $m_c = 6.25 \times 10^3$ A/s. (a) Coexisting (interacting) fast and slow-scale bifurcation with $1/m_1 = 9 \times 10^{-6}$ s/A and $\tau_f = 0.362$ ms, (b) coexisting (interacting) fast and slow-scale bifurcation with $1/m_1 = 19.835 \times 10^{-6}$ s/A and $\tau_f = 0.8265$ ms, (c) slow-scale bifurcation with $1/m_1 = 31.514 \times 10^{-6}$ s/A and $\tau_f = 1.3538$ ms.

Simulations

Quick glimpse at changing m_c

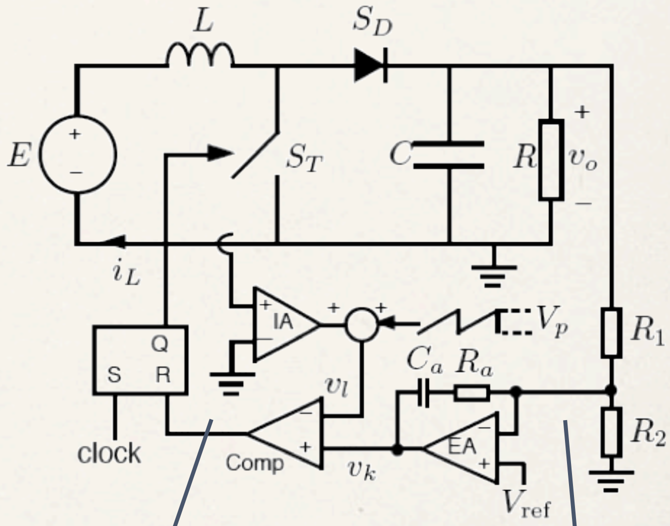


(a) (b) (c)

Figure 4: Simulated behaviors for different values of m_c, with $g = 0.4$, $\tau_f = 1.3253$ ms, and $1/m_1 = 31.514 \times 10^{-6}$ s/A. (a) Coexisting (interacting) fast and slow-scale bifurcation with $m_c = 2.825 \times 10^3$ A/s , (b) critical coexisting (interacting) fast and slow-scale bifurcation with $m_c = 3.825 \times 10^3$ A/s, (c) slow-scale bifurcation with $m_c = 4.0 \times 10^3$ A/s.

Complexity: interacting loops

- **Guiding questions:**
  - Under what parameter ranges the system will bifurcation into
    - fast-scale unstable region?
    - slow-scale unstable region?
    - interacting fast-scale slow-scale unstable region?
      - This requires bifurcation analysis.
      - Results have to be useful for design.

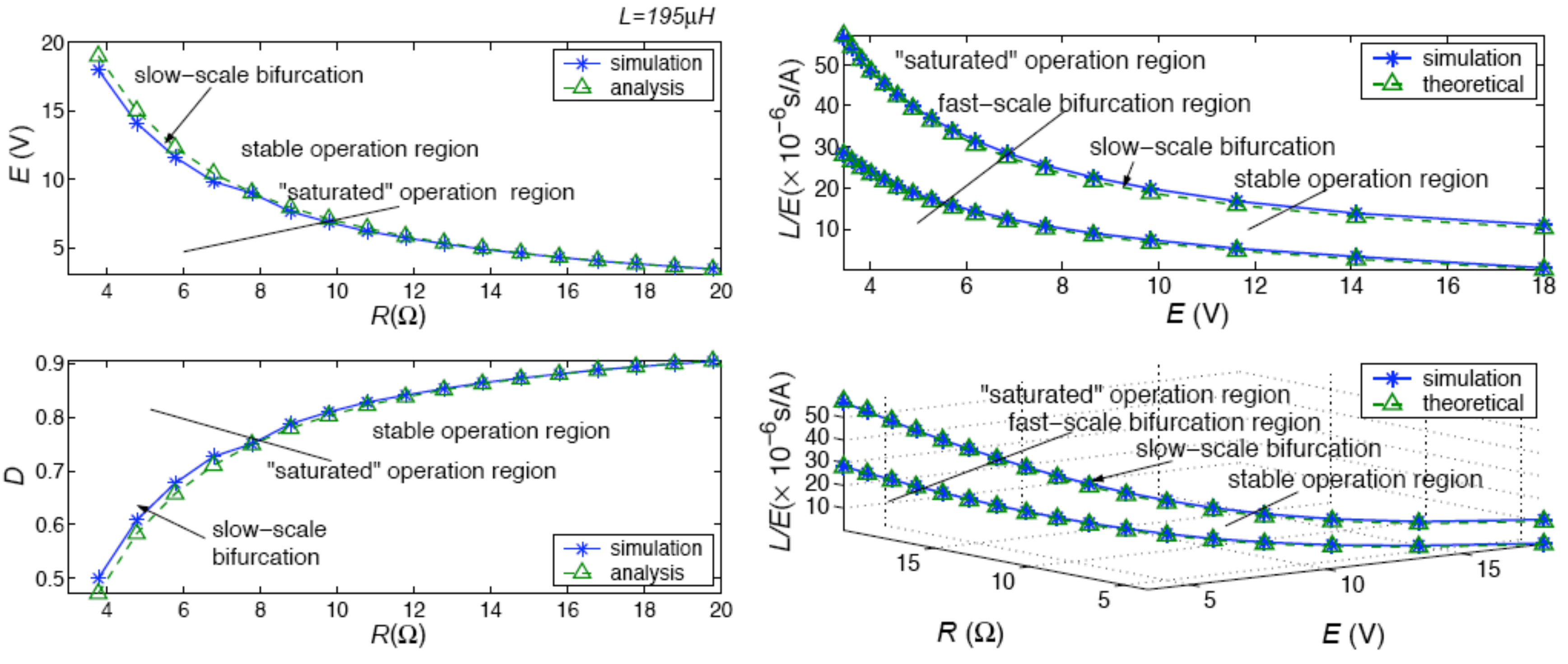


inner current loop (fast)

outer voltage loop (slow)

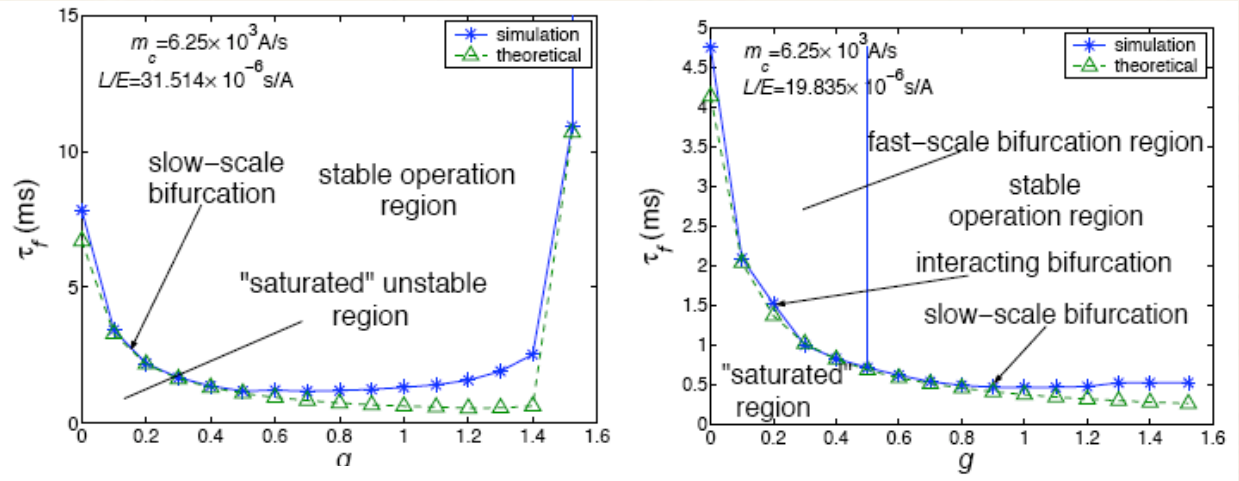
Sample results (detailed omitted)

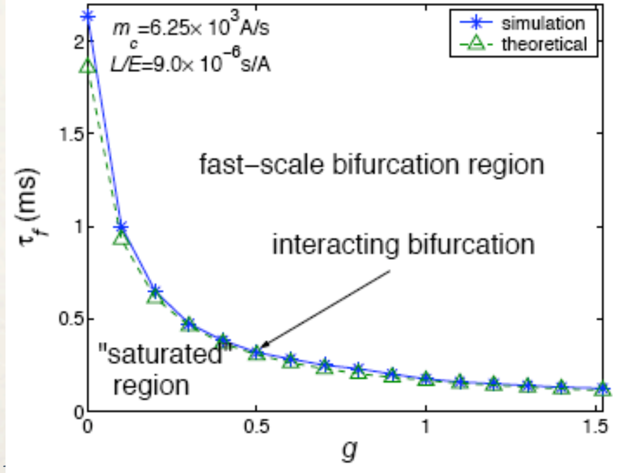
Design-oriented bifurcation charts



Sample results (detailed omitted)

Design-oriented bifurcation charts

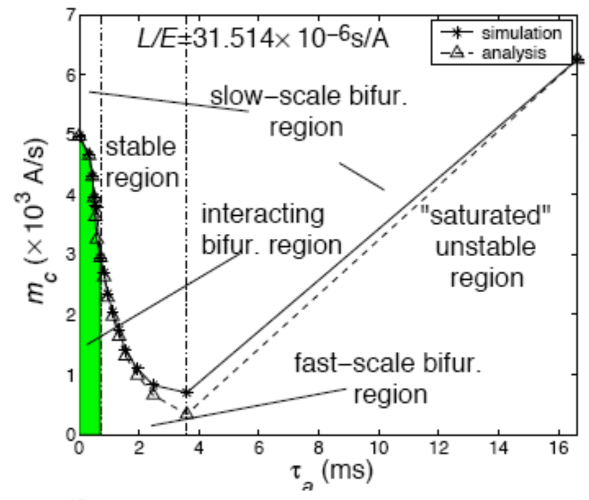


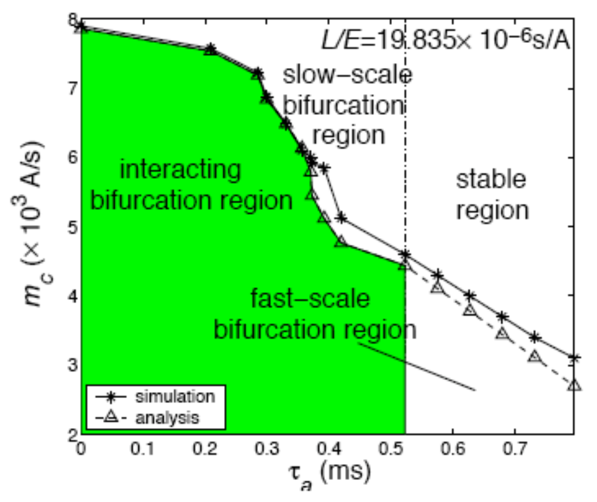


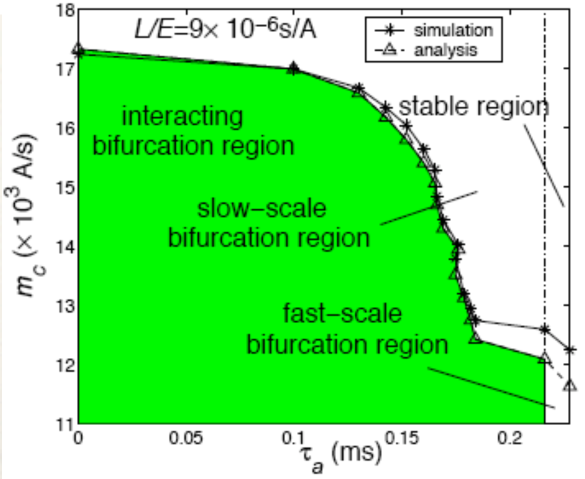
Operating boundaries under varying feedback gain and time constant

Sample results (detailed omitted)

Design-oriented bifurcation charts







Operating boundaries under varying m_c and τ_a

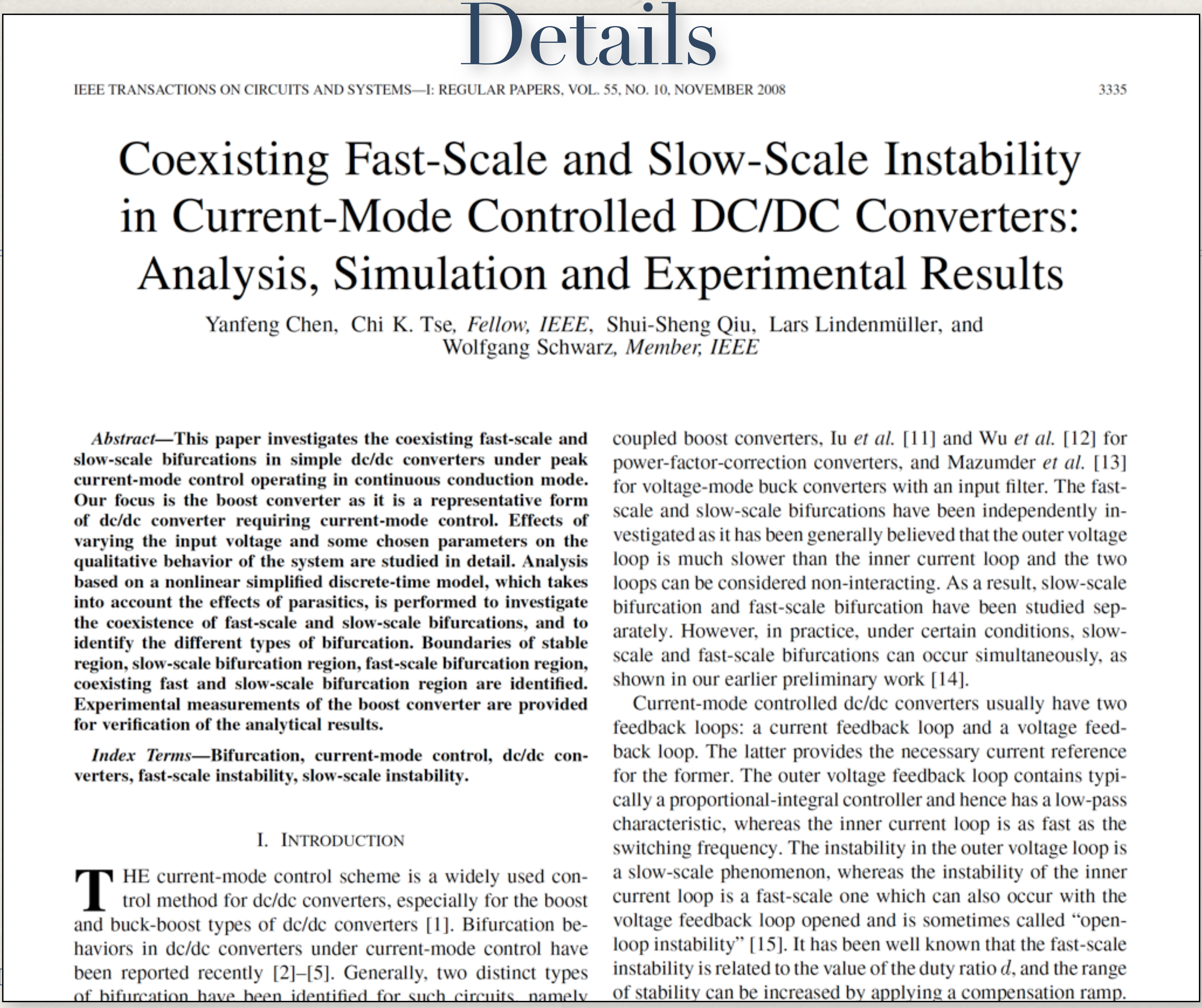
Analysis and verifications

- Analysis can be performed to provide closed-form expressions of the bifurcation conditions.
    - Analysis via examining Jacobian and movement of eigenvalues with variations of selected important parameters.
- Normally, experimental measurements are expected for verifying the qualitative results.

Deriving design guidelines

- Under certain parameter ranges, current-mode controlled boost converters can be fast-scale and slow-scale unstable simultaneously.
- The main parameters affecting fast-scale bifurcations are the rising slope of the inductance current, and the slope of compensation ramp,
- The main parameters affecting slow-scale bifurcations are the voltage feedback gain g and time constant.
- Slow-scale bifurcation can be eliminated by decreasing the feedback gain and/or bandwidth
- Fast-scale bifurcation can be reduced by increasing the slope of the compensation ramp or decreasing the rising slope of the inductor current.

Details



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Coexisting Fast-Scale and Slow-Scale Instability in Current-Mode Controlled DC/DC Converters: Analysis, Simulation and Experimental Results

Yanfeng Chen, Chi K. Tse, *Fellow, IEEE*, Shui-Sheng Qiu, Lars Lindenmüller, and
Wolfgang Schwarz, *Member, IEEE*

***Abstract*—This paper investigates the coexisting fast-scale and slow-scale bifurcations in simple dc/dc converters under peak current-mode control operating in continuous conduction mode. Our focus is the boost converter as it is a representative form of dc/dc converter requiring current-mode control. Effects of varying the input voltage and some chosen parameters on the qualitative behavior of the system are studied in detail. Analysis based on a nonlinear simplified discrete-time model, which takes into account the effects of parasitics, is performed to investigate the coexistence of fast-scale and slow-scale bifurcations, and to identify the different types of bifurcation. Boundaries of stable region, slow-scale bifurcation region, fast-scale bifurcation region, coexisting fast and slow-scale bifurcation region are identified. Experimental measurements of the boost converter are provided for verification of the analytical results.**

***Index Terms*—Bifurcation, current-mode control, dc/dc converters, fast-scale instability, slow-scale instability.**

I. INTRODUCTION

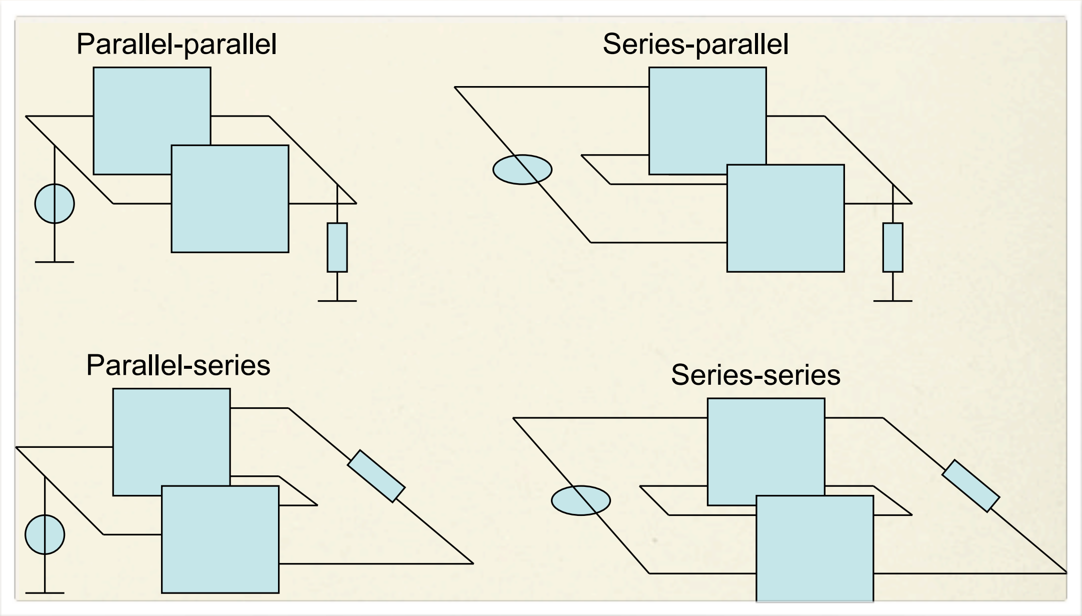
THE current-mode control scheme is a widely used control method for dc/dc converters, especially for the boost and buck-boost types of dc/dc converters [1]. Bifurcation behaviors in dc/dc converters under current-mode control have been reported recently [2]–[5]. Generally, two distinct types of bifurcation have been identified for such circuits, namely

coupled boost converters, Iu *et al.* [11] and Wu *et al.* [12] for power-factor-correction converters, and Mazumder *et al.* [13] for voltage-mode buck converters with an input filter. The fast-scale and slow-scale bifurcations have been independently investigated as it has been generally believed that the outer voltage loop is much slower than the inner current loop and the two loops can be considered non-interacting. As a result, slow-scale bifurcation and fast-scale bifurcation have been studied separately. However, in practice, under certain conditions, slow-scale and fast-scale bifurcations can occur simultaneously, as shown in our earlier preliminary work [14].

Current-mode controlled dc/dc converters usually have two feedback loops: a current feedback loop and a voltage feedback loop. The latter provides the necessary current reference for the former. The outer voltage feedback loop contains typically a proportional-integral controller and hence has a low-pass characteristic, whereas the inner current loop is as fast as the switching frequency. The instability in the outer voltage loop is a slow-scale phenomenon, whereas the instability of the inner current loop is a fast-scale one which can also occur with the voltage feedback loop opened and is sometimes called "open-loop instability" [15]. It has been well known that the fast-scale instability is related to the value of the duty ratio d, and the range of stability can be increased by applying a compensation ramp.

Case study 2: on control

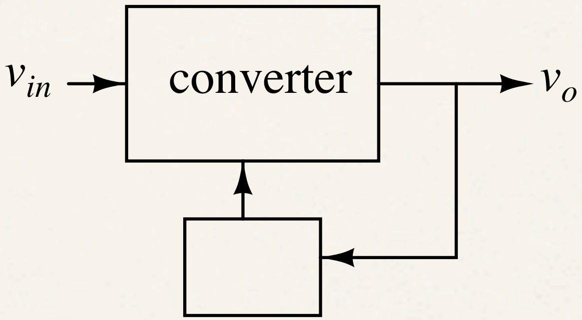
- Interconnected converters
  - Parallel - lower current stress
    - Input parallel connected
    - Output parallel connected
  - Series - lower voltage stress
    - Input series connected
    - Output series connected

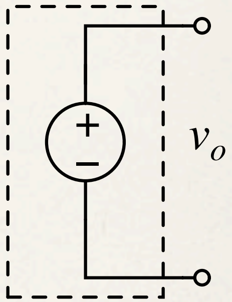


- **Question: How to control individual converters?**

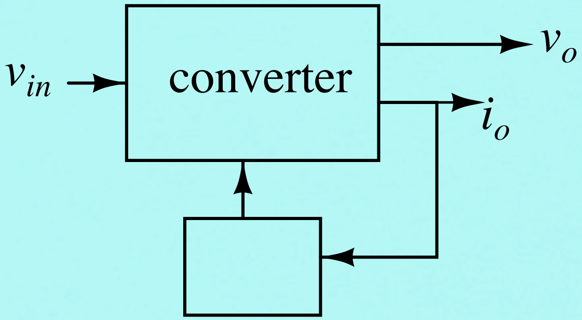
A general note on control

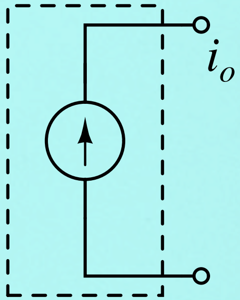
- Voltage mode control (voltage programming)
    - basically makes the converter a voltage source





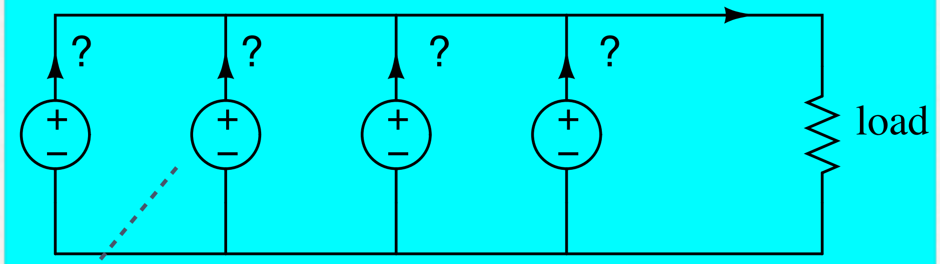
- Current mode control (current programming)
    - fundamentally controls current
    - basically makes the converter a current source





Parallel-connected converters

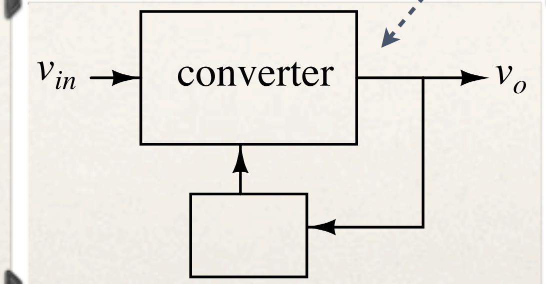
- **Parallel connected converters for high current output applications**
- Control challenge is: sharing of output currents
- PROBLEM: If each converter attempts to produce a regulated output voltage, we are trying put voltage sources in parallel ! This is a ***fundamental conflict!***



Perfectly regulated voltage converter is like an independent voltage source.

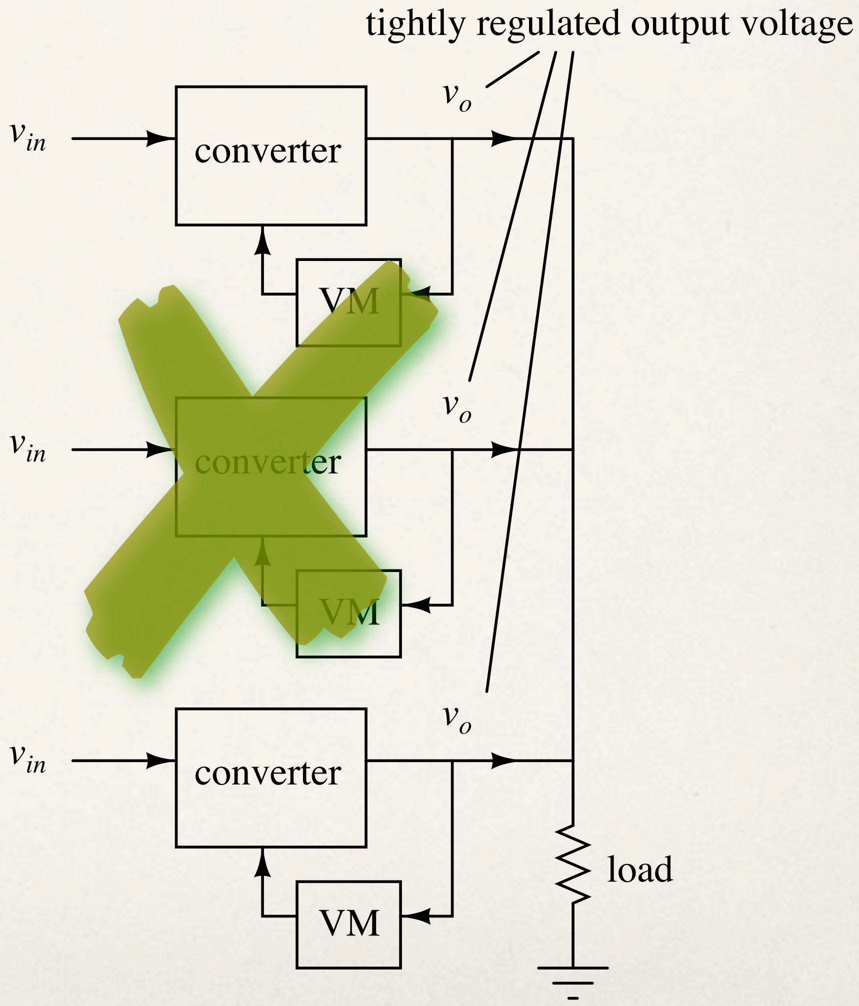
Connecting voltage sources in parallel violates KVL, and should not be allowed.

Even if the voltages have the same voltage magnitude, currents are theoretically not solvable.



What should be prohibited

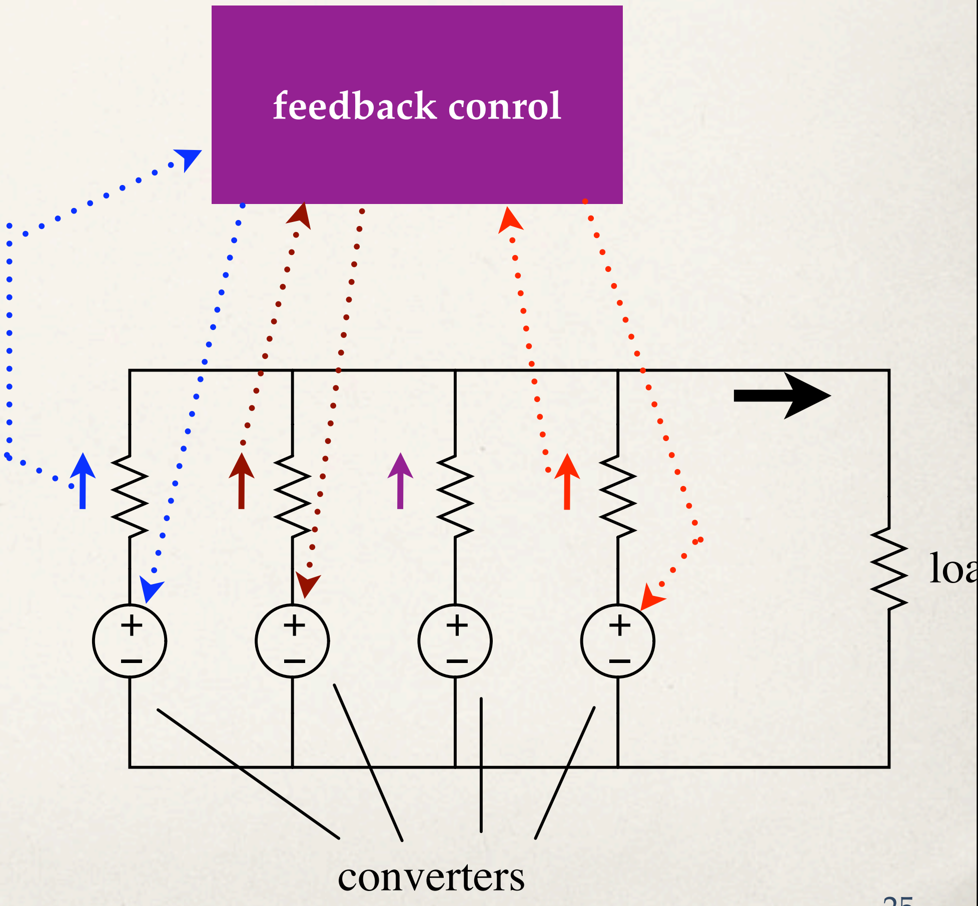
- Putting “more than one converters having regulated output voltages” in parallel is ***theoretically faulty and should be prohibited***!



Still tolerable in practice

- Conventional connection (used widely in practice called ***droop connection method***):
  - Each converter is output regulated.
  - Parallel connection of two or more converters to deliver large currents.
  - Current sharing control is applied mandatorily.

Current sharing is controlled and maintained in individual converters through the simple voltage feedback which automatically detects the voltage drops across the resistances and regulates the output voltage slightly. This is the simple DROOP METHOD, involving just connecting the "poorly" voltage-regulated converters.



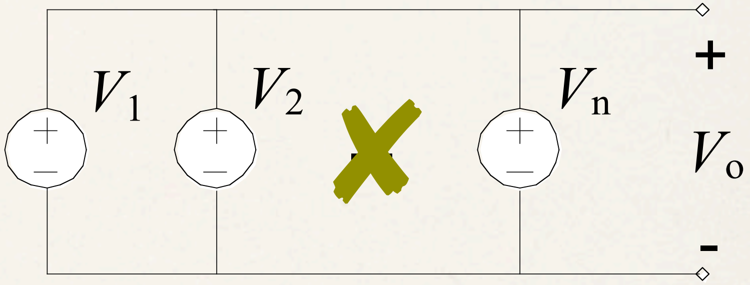
Limitations of connecting voltage regulators using droop method

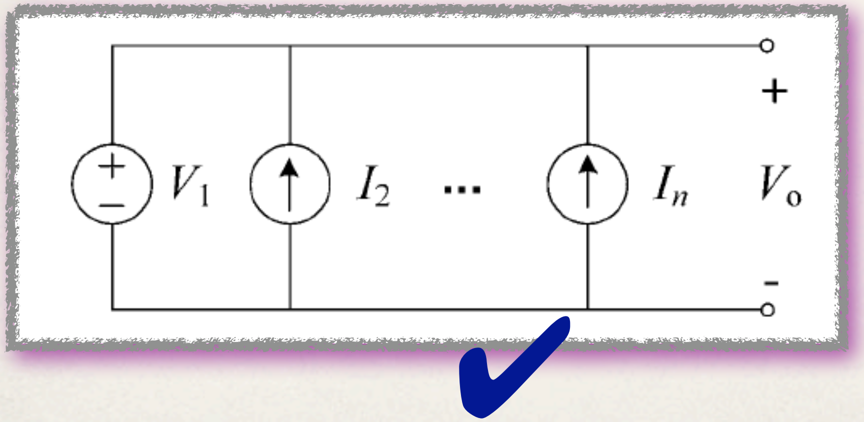
- First, it is theoretically bad (strictly "prohibited") to connect voltage sources in parallel.
- We must deliberately make the output regulation in each converter poor, so that it has substantial output resistance.
- Current sharing is possible through adjusting the output voltage levels of individual converters. The range is very limited because it is supposed to be voltage regulator (fixed voltage more or less).
- Obviously, the output voltage regulation cannot be very good for the load.

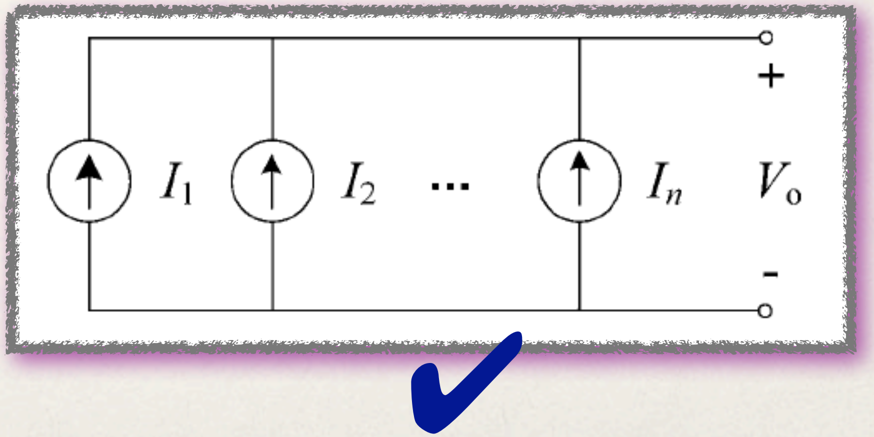
- ***But it is simple and enjoys modularity!***
    - ***theoretically nonsense at start, but practically sensible if appropriately applied.***

Connection re-examined

- How should we connect the converters if they are controlled as voltage/ current sources?
- Then, it would become straightforward to select the appropriate control strategies.

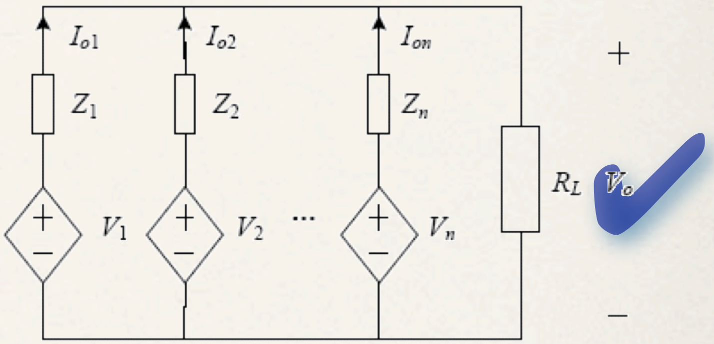




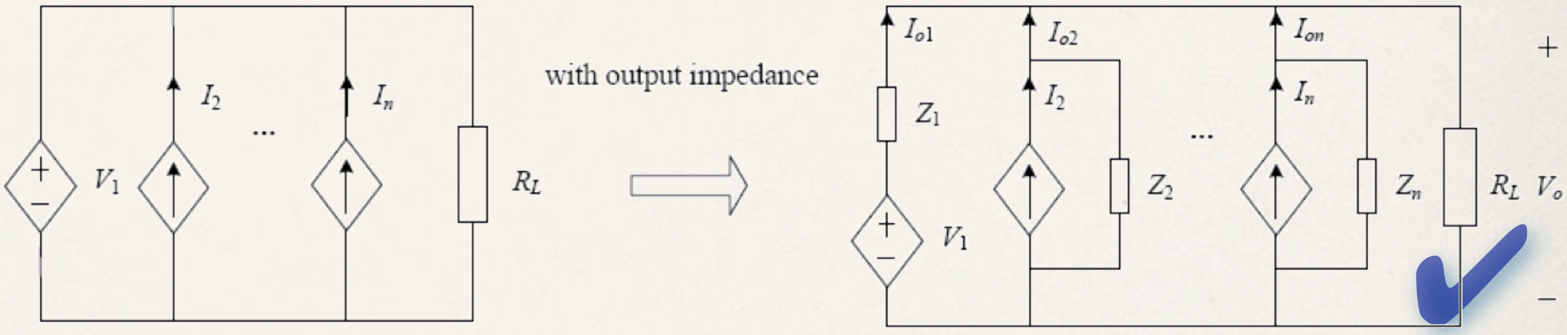


Possible configurations

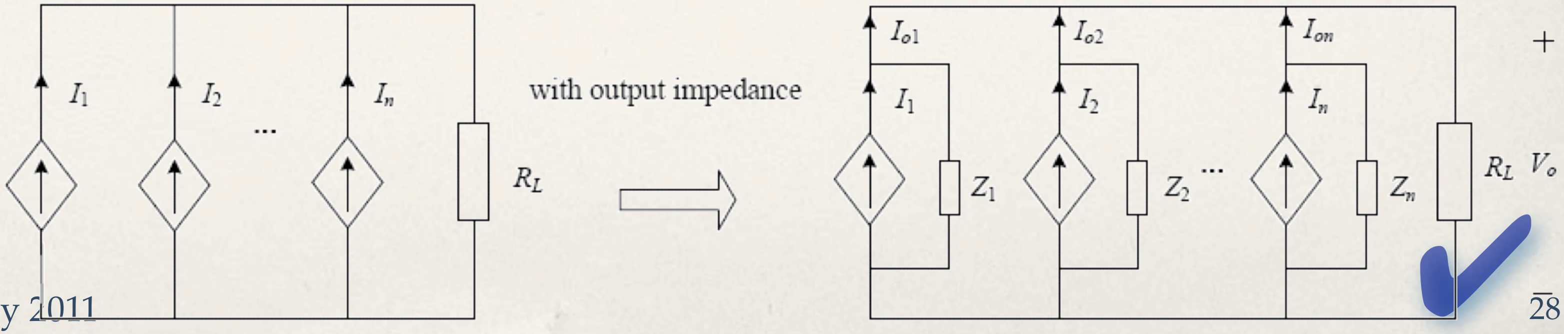
Type I



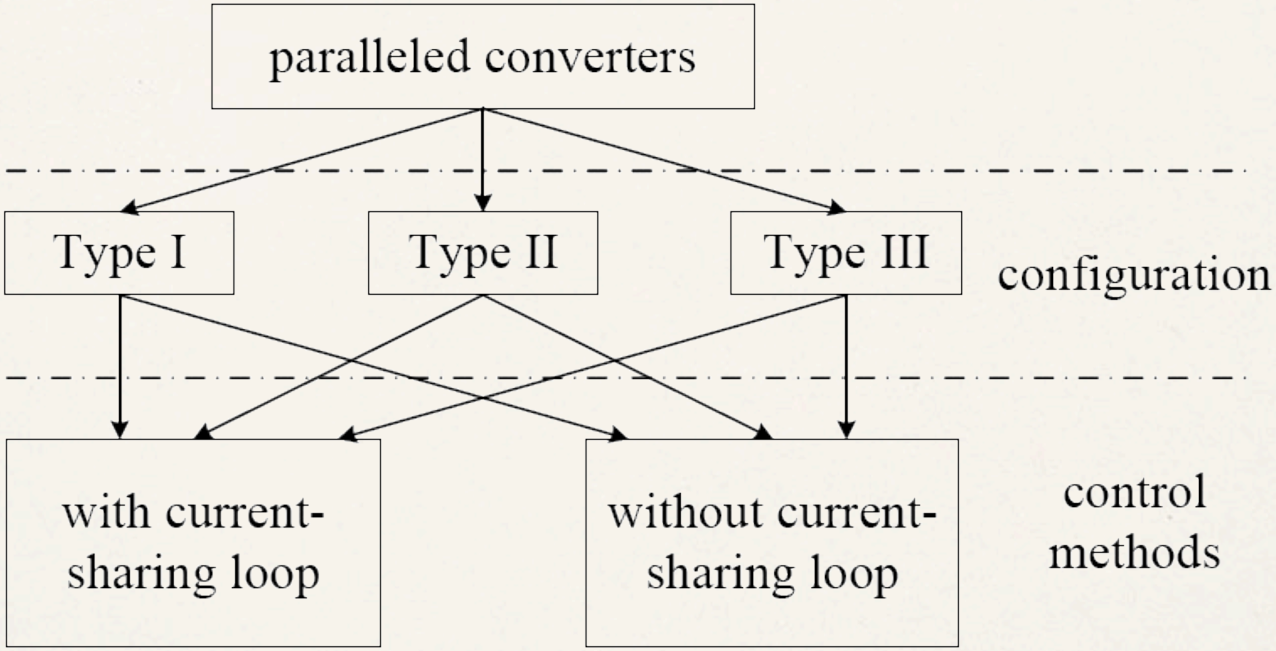
Type II



Type III



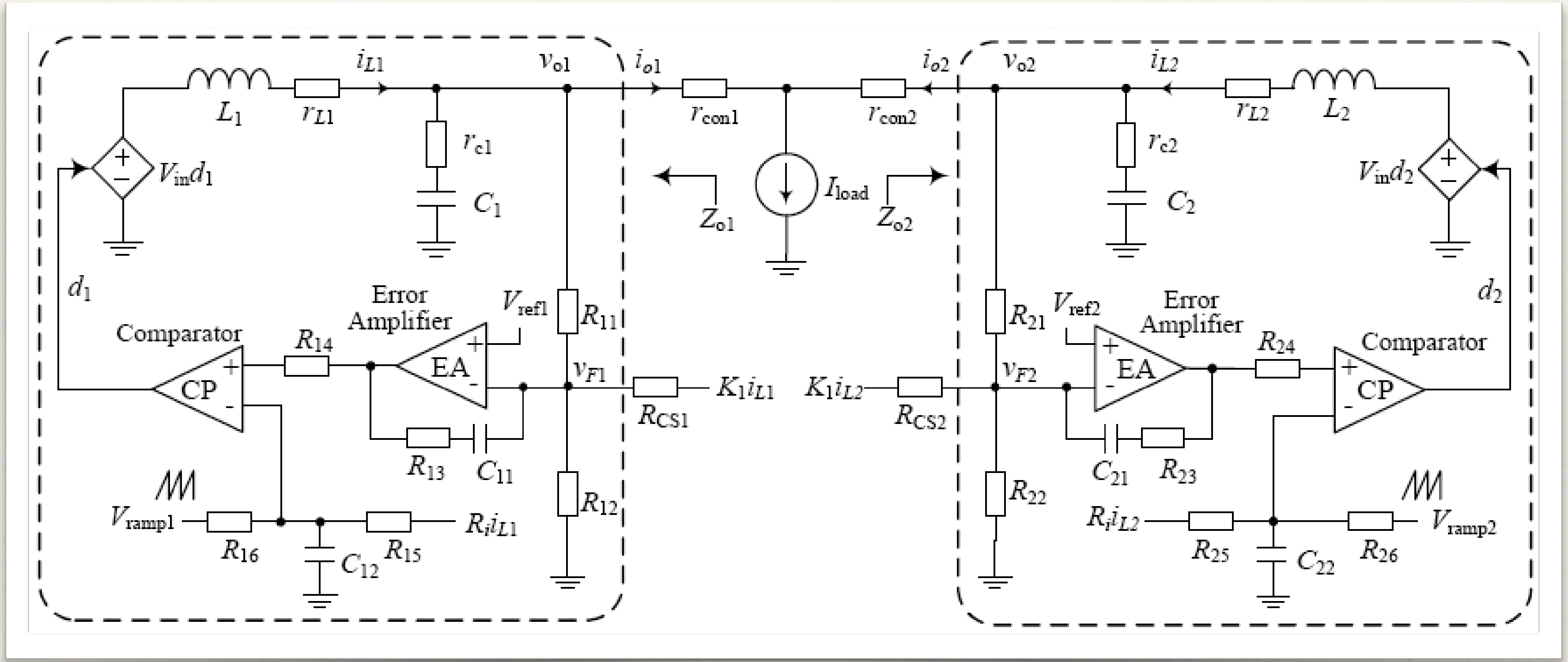
General classification



Definition: ***Current sharing loop*** is defined as one that takes output current information from one or more constituent converters to produce a current control signal which is used for controlling an individual converter.

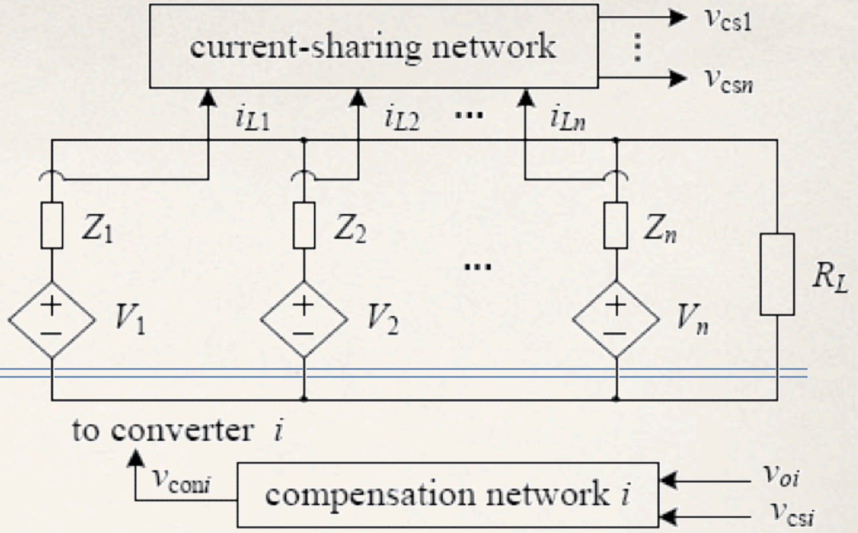
Type I

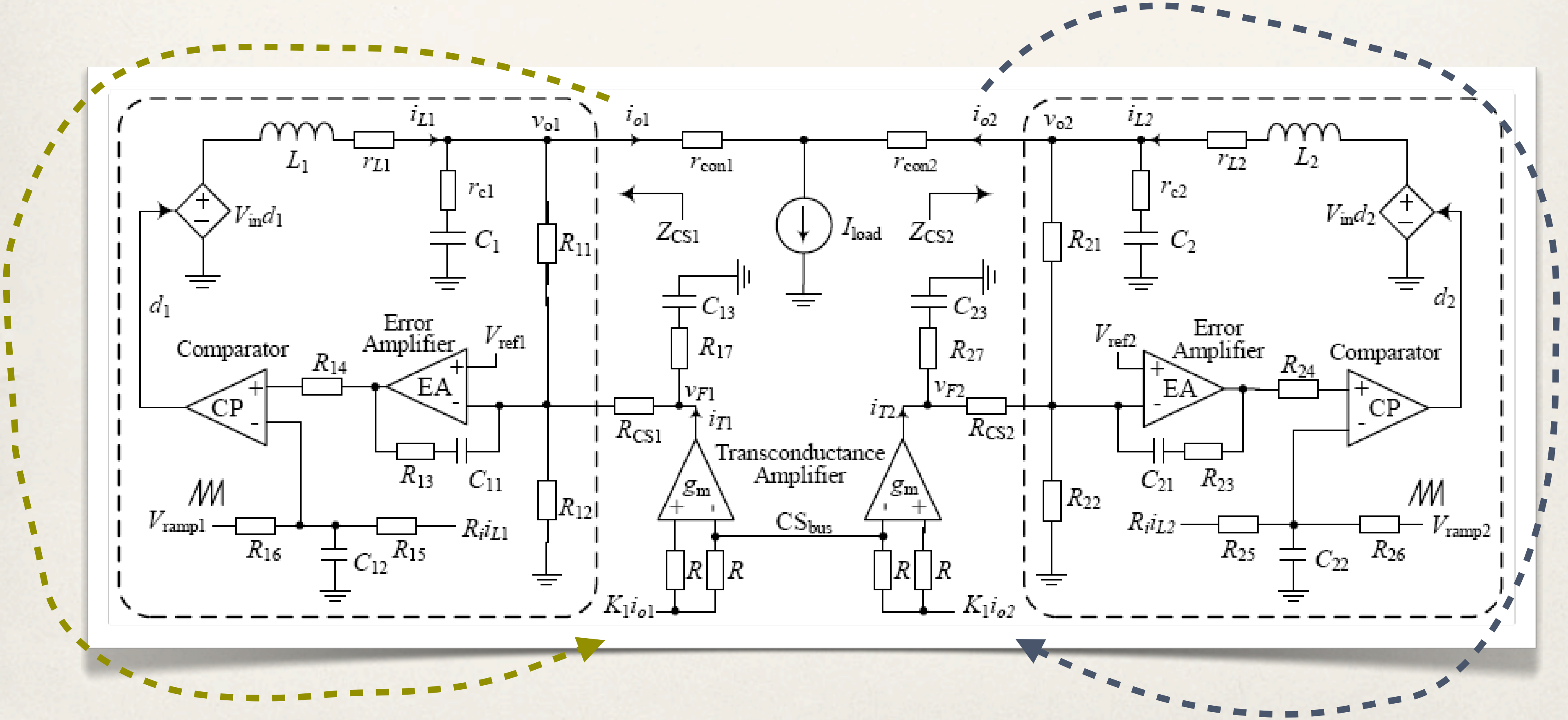
Control *without* current sharing loop, i.e., **droop method**



Type I

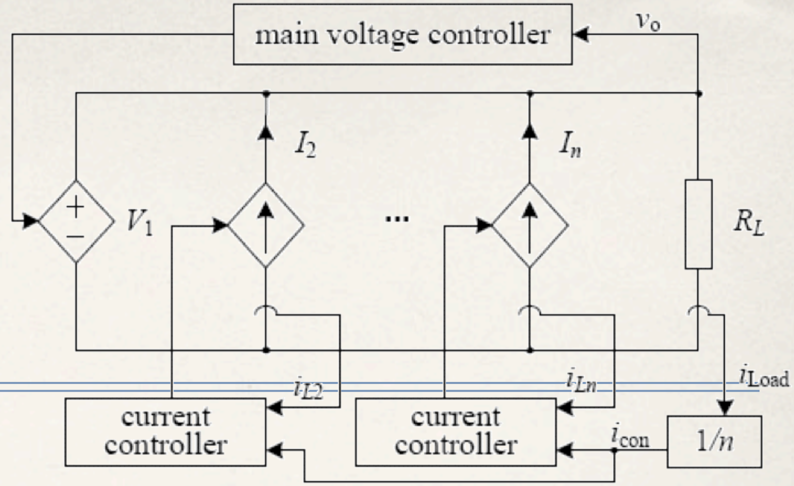
Control *with* current sharing loop

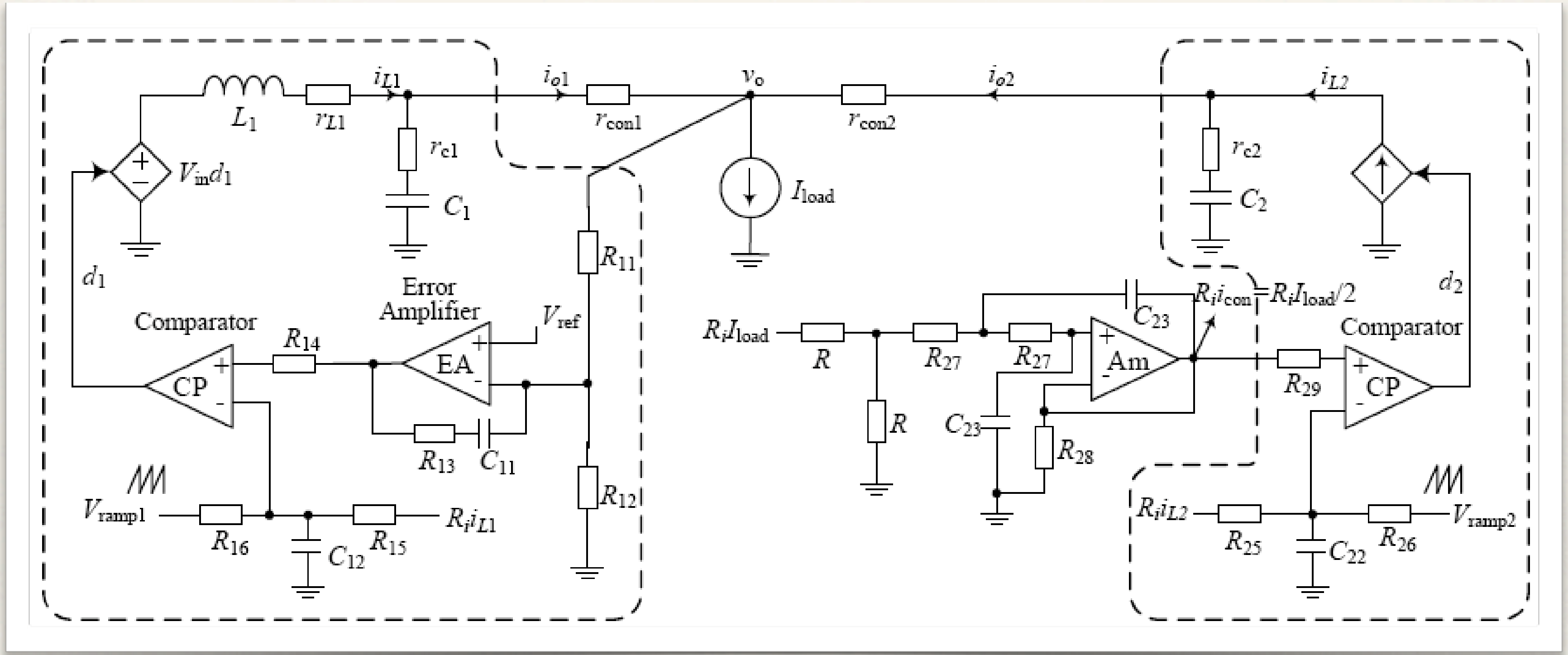




Type II

Control *without* current sharing loop

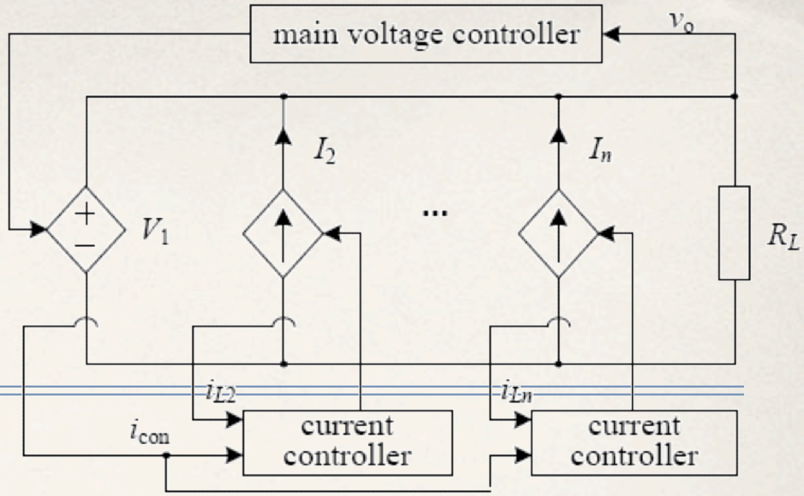


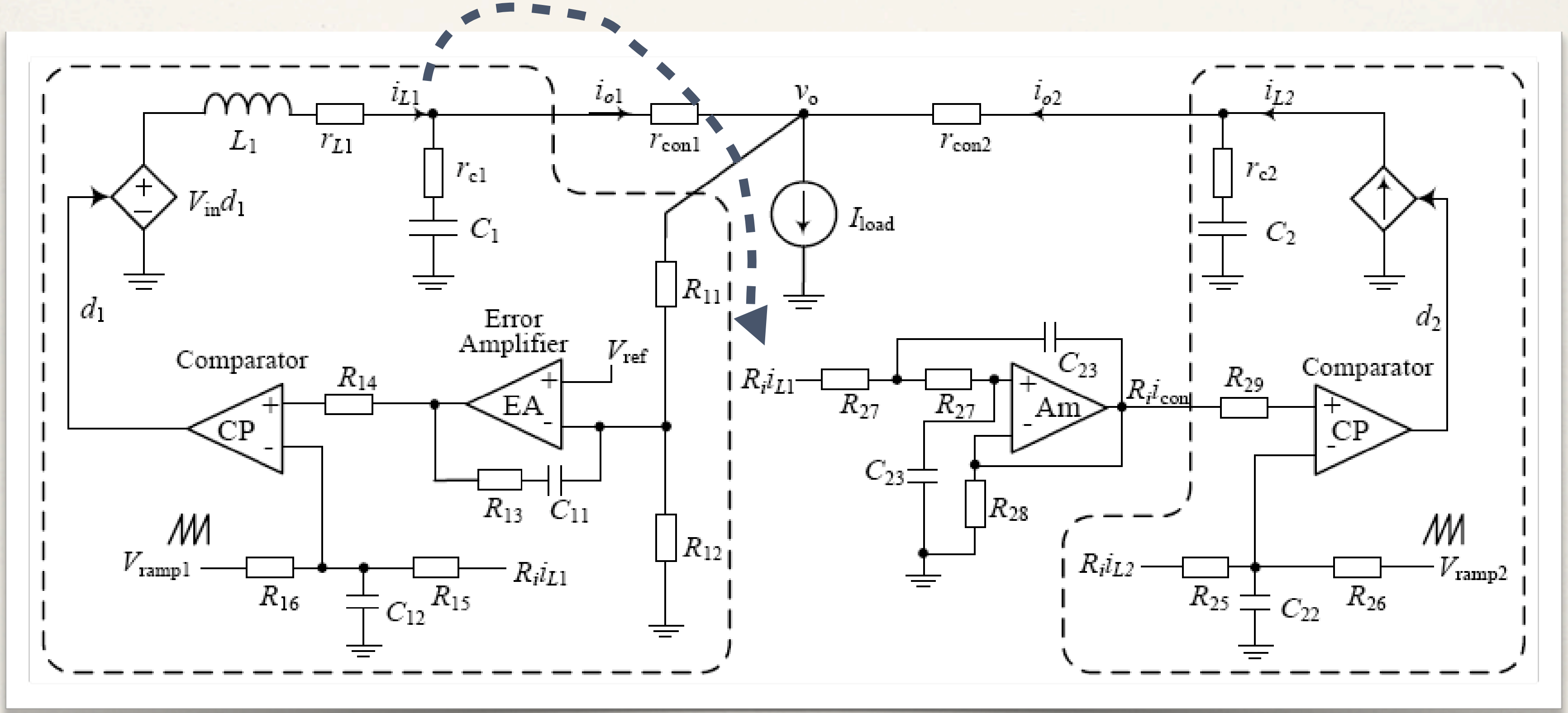


- For **Type II connection**, only one converter serves as a voltage source (more precisely a Thevenin source), and all others behave as current (Norton) sources.
- There is a main voltage controller to regulate the output voltage tightly.
- All current sources only need to follow a common current control signal to achieve current sharing.

Type II

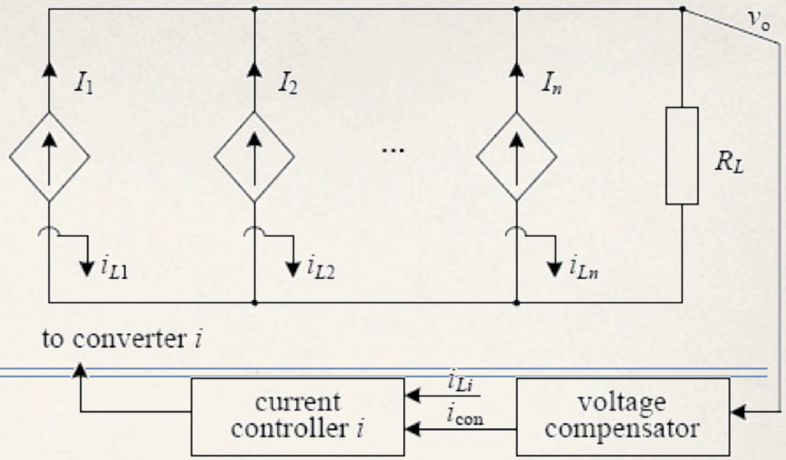
Control *with* current sharing loop

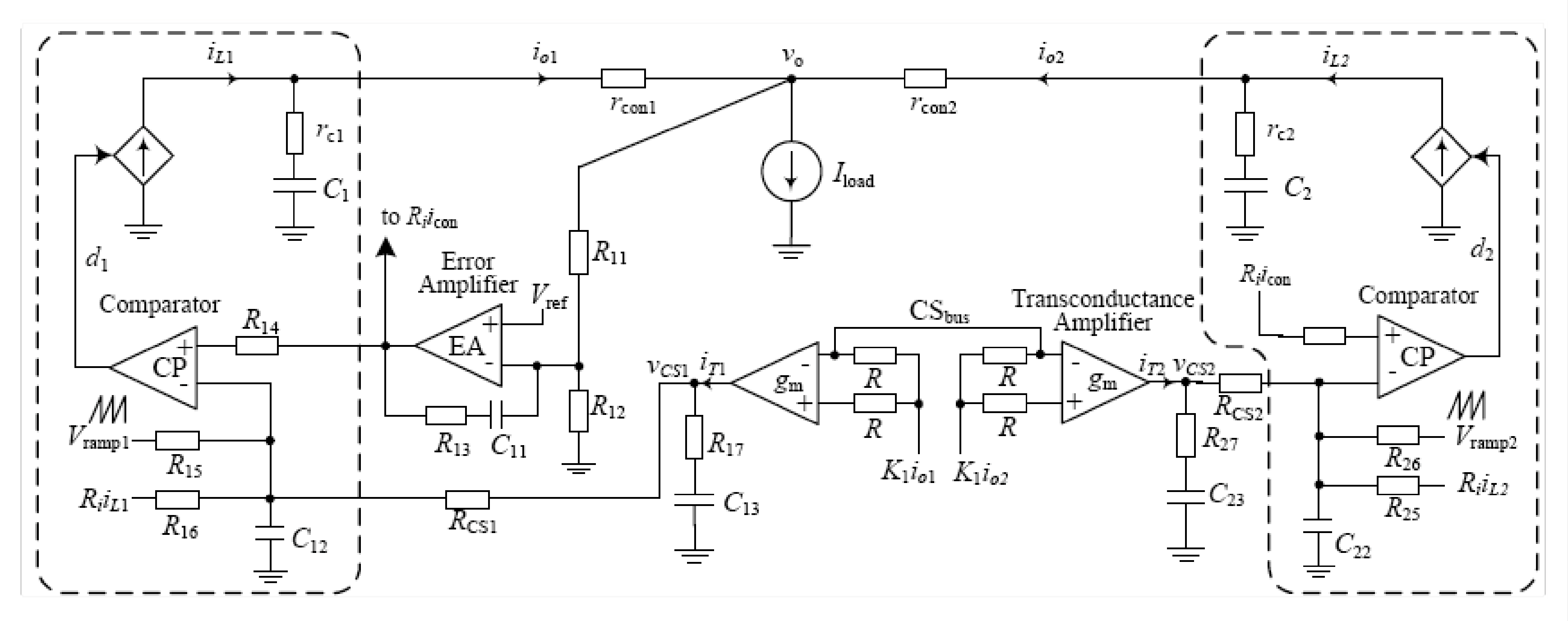




Type III

Control *without* current sharing loop

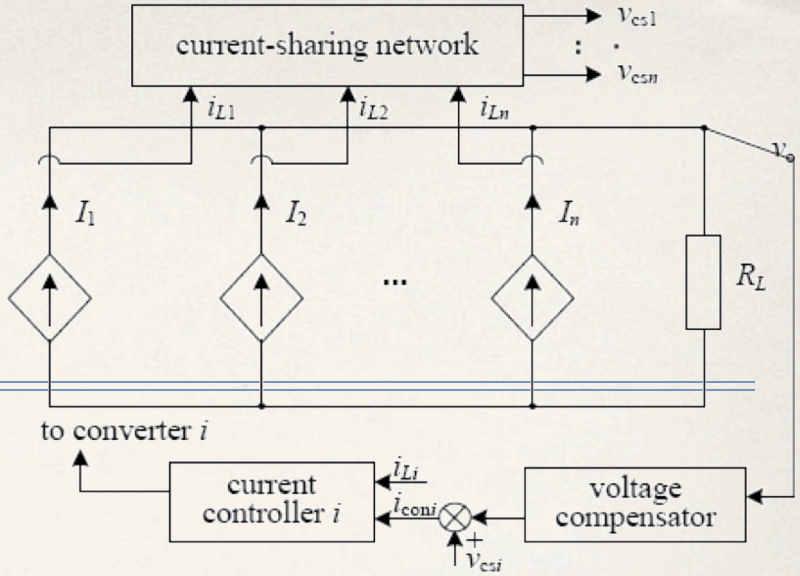


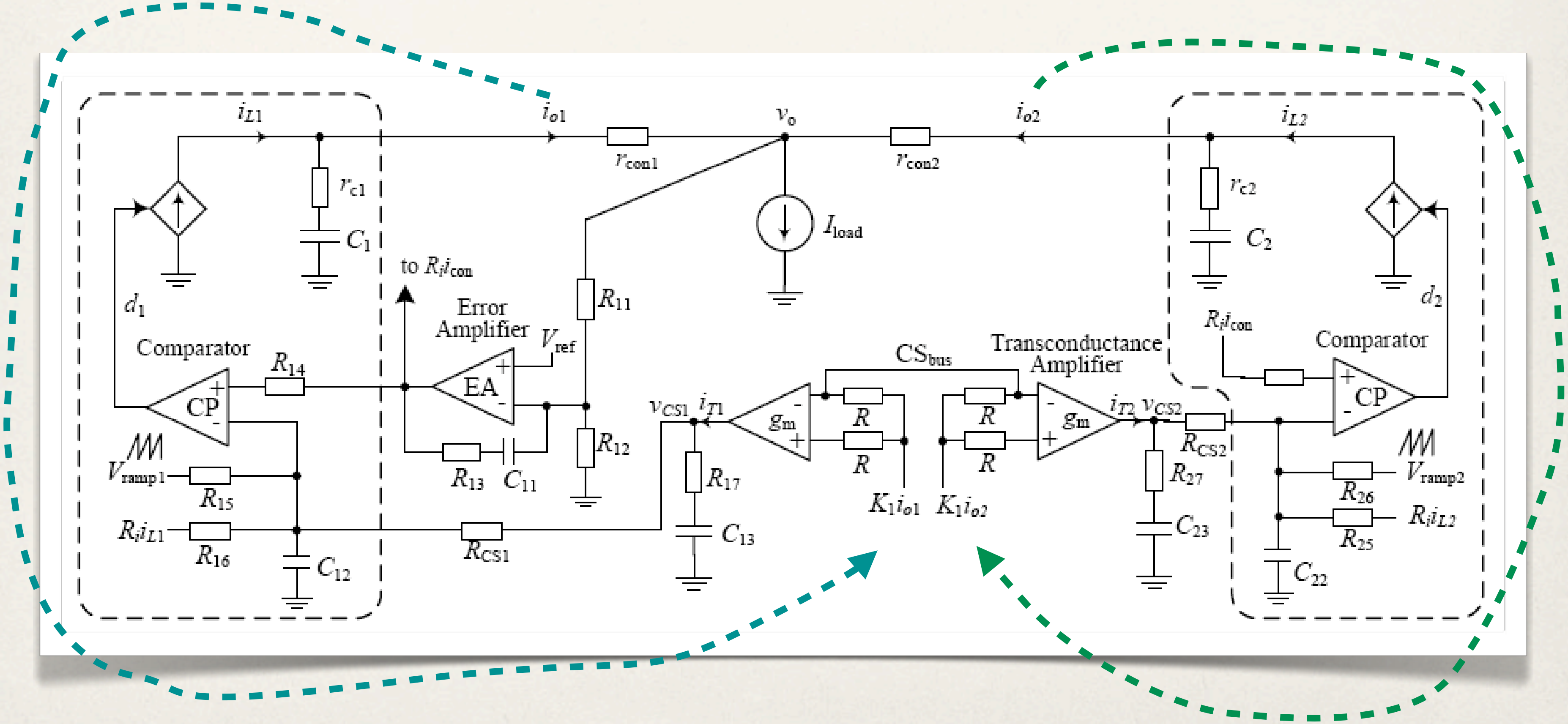


For **Type III connection**, all converters are current (Norton) sources.

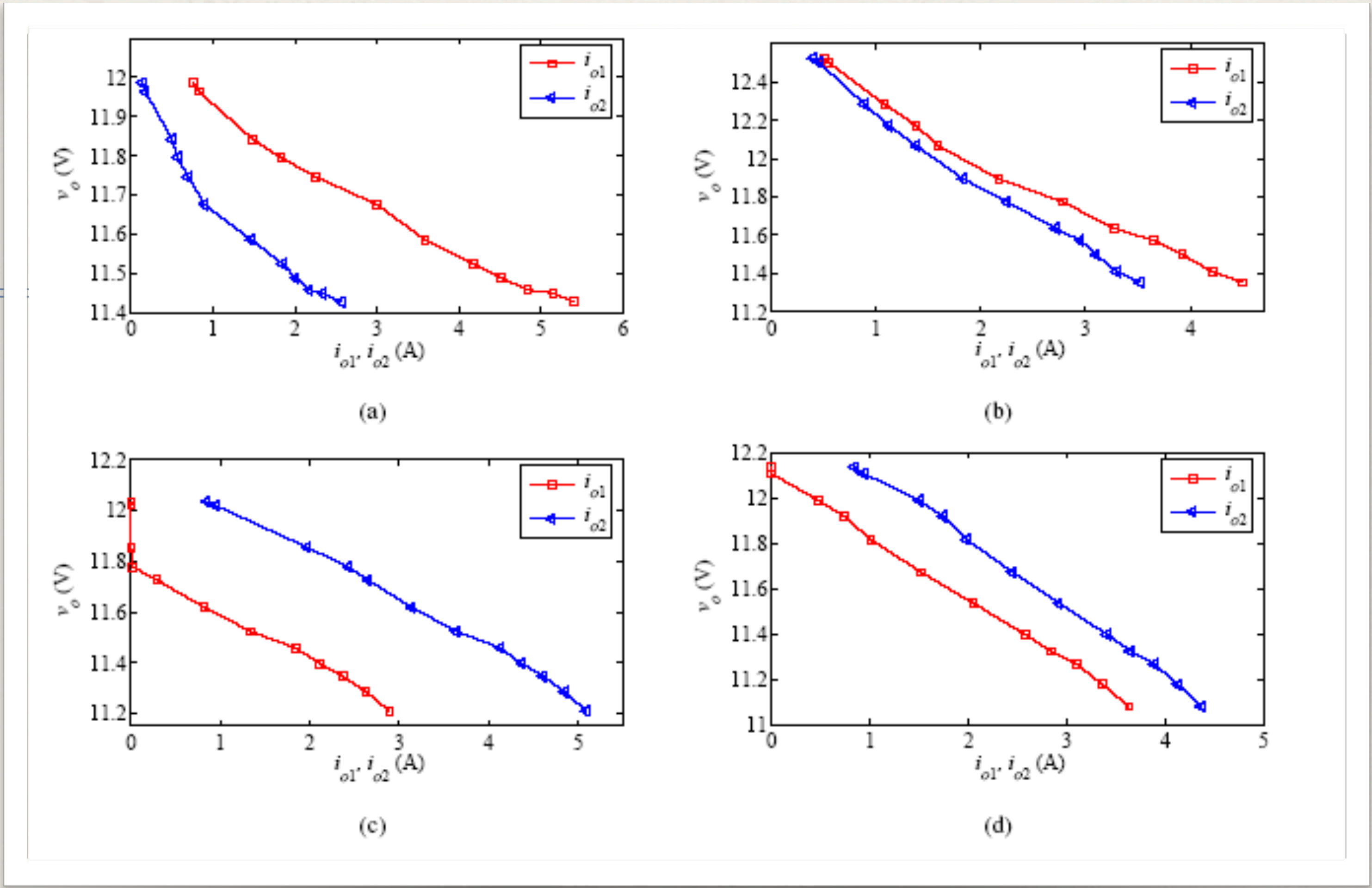
Type III

Control *with* current sharing loop



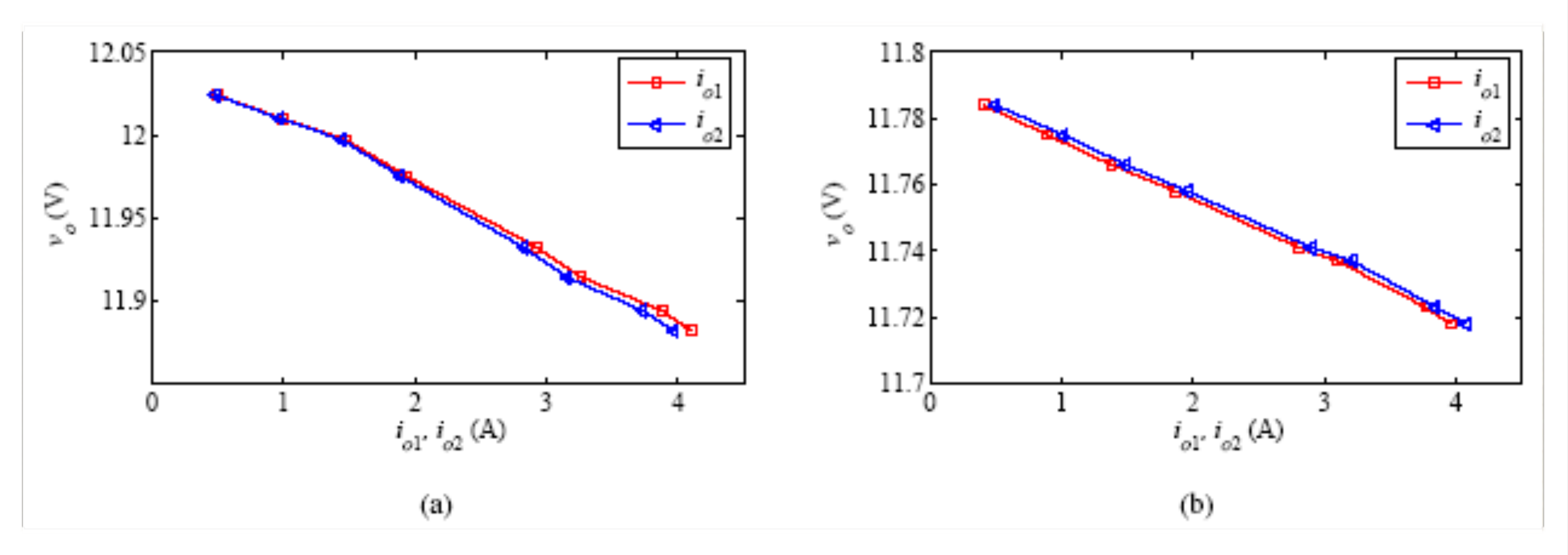


Results



- Output voltage versus output current for **Type I scheme without a current-sharing loop**. (a) $V_{\mathrm{ref1}} = V_{\mathrm{ref2}} = 2.5$ V, $r_{\mathrm{con1}} = 0.001\Omega$, $r_{\mathrm{con2}} = 0.05\Omega$, $R_{\mathrm{CS1}} = R_{\mathrm{CS2}} = 150$ kΩ; (b) $V_{\mathrm{ref1}} = V_{\mathrm{ref2}} = 2.5$ V, $r_{\mathrm{con1}} = 0.001\Omega$, $r_{\mathrm{con2}} = 0.05\Omega$, $R_{\mathrm{CS1}} = R_{\mathrm{CS2}} = 50$ kΩ; (c) $V_{\mathrm{ref1}} = 2.4$ V, $V_{\mathrm{ref2}} = 2.5$ V, $r_{\mathrm{con1}} = r_{\mathrm{con2}} = 0.025\Omega$, $R_{\mathrm{CS1}} = R_{\mathrm{CS2}} = 150$ kΩ; (d) $V_{\mathrm{ref1}} = 2.4$ V, $V_{\mathrm{ref2}} = 2.5$ V, $r_{\mathrm{con1}} = r_{\mathrm{con2}} = 0.025\Omega$, $R_{\mathrm{CS1}} = R_{\mathrm{CS2}} = 50$ kΩ.

Results

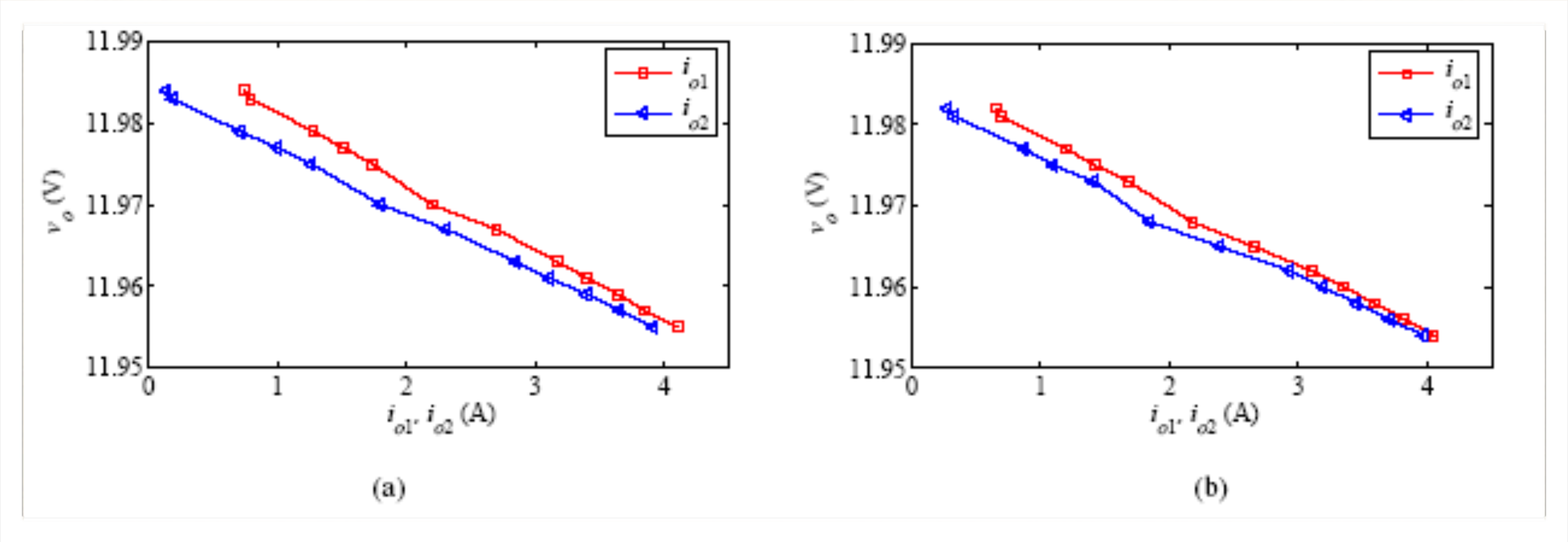


(a)

(b)

- Output voltage versus output current for **Type I scheme with a current-sharing loop**. (a) $V_{\text{ref1}} = V_{\text{ref2}} = 2.5$ V, $r_{\text{con1}} = 0.001\ \Omega$, $r_{\text{con2}} = 0.05\ \Omega$; (b) $V_{\text{ref1}} = 2.4$ V, $V_{\text{ref2}} = 2.5$ V, $r_{\text{con1}} = r_{\text{con2}} = 0.001\ \Omega$.

Results

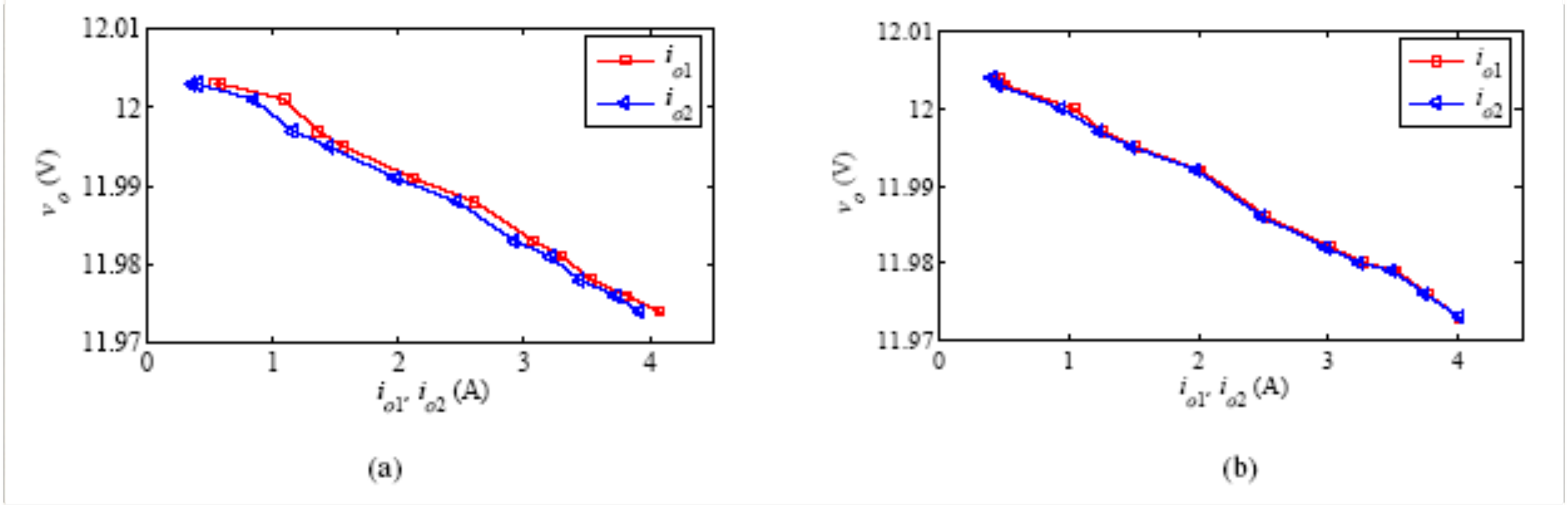


(a)

(b)

- Output voltage versus output current for **Type II scheme** at $V_{\text{ref}} = 2.5$ V, $r_{\text{con1}} = 0.001\ \Omega$, $r_{\text{con2}} = 0.05\ \Omega$, (a) without a current-sharing loop; (b) with a current-sharing loop.

Results



(a)

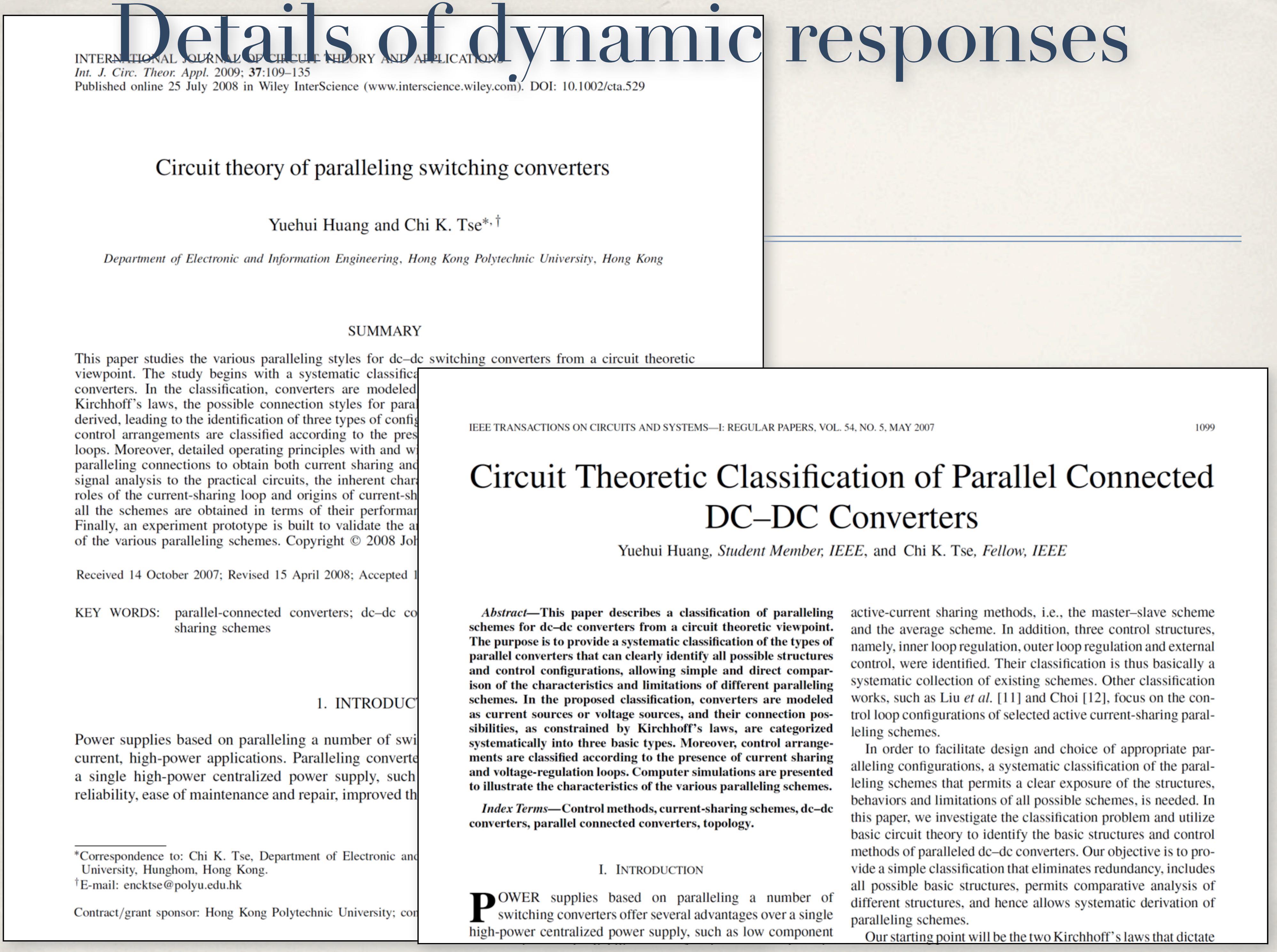
(b)

- Output voltage versus output current for **Type III scheme** at V_{ref} = 2.5 V, r_{con1} = 0.001 Ω, r_{con2} = 0.05 Ω, (a) without a current-sharing loop; (b) with a current-sharing loop.

General comparison

- **Type I** schemes are simple but suffer fundamentally from paralleling voltage sources. The adjustment range for current sharing is small since each constituent converter is designed primarily to regulate its output voltage.
- **Type II** schemes are theoretically more viable as there is only one voltage source paralleling with current sources. The dynamics of the voltage regulation thus depends on the control method being employed by the voltage regulating loop. Current-sharing performance is generally much better and the control implementation is simpler, compared to Type I schemes.
- **Type III** schemes are generally best in terms of current sharing as all converters are fundamentally current controlled. The voltage regulation is only executed at the load side (only one voltage loop to keep tight regulation). Both voltage regulation and current sharing are excellent.

Details of dynamic responses



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Circuit theory of paralleling switching converters

Yuehui Huang and Chi K. Tse*,†

Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong

SUMMARY

This paper studies the various paralleling styles for dc–dc switching converters from a circuit theoretic
viewpoint. The study begins with a systematic classifica
converters. In the classification, converters are modeled
Kirchhoff's laws, the possible connection styles for paral
derived, leading to the identification of three types of config
control arrangements are classified according to the pres
loops. Moreover, detailed operating principles with and w
paralleling connections to obtain both current sharing and
signal analysis to the practical circuits, the inherent chara
roles of the current-sharing loop and origins of current-sh
all the schemes are obtained in terms of their performan
Finally, an experiment prototype is built to validate the a
of the various paralleling schemes. Copyright © 2008 Joh

Received 14 October 2007; Revised 15 April 2008; Accepted 1

KEY WORDS: parallel-connected converters; dc–dc co
sharing schemes

1. INTRODUC

Power supplies based on paralleling a number of swi
current, high-power applications. Paralleling converte
a single high-power centralized power supply, such
reliability, ease of maintenance and repair, improved th

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*Correspondence to: Chi K. Tse, Department of Electronic and
University, Hunghom, Hong Kong.
†E-mail: encktse@polyu.edu.hk

Contract/grant sponsor: Hong Kong Polytechnic University; con

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Circuit Theoretic Classification of Parallel Connected DC–DC Converters

Yuehui Huang, *Student Member, IEEE*, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—This paper describes a classification of paralleling schemes for dc–dc converters from a circuit theoretic viewpoint. The purpose is to provide a systematic classification of the types of parallel converters that can clearly identify all possible structures and control configurations, allowing simple and direct comparison of the characteristics and limitations of different paralleling schemes. In the proposed classification, converters are modeled as current sources or voltage sources, and their connection possibilities, as constrained by Kirchhoff's laws, are categorized systematically into three basic types. Moreover, control arrangements are classified according to the presence of current sharing and voltage-regulation loops. Computer simulations are presented to illustrate the characteristics of the various paralleling schemes.**

***Index Terms*—Control methods, current-sharing schemes, dc–dc converters, parallel connected converters, topology.**

I. INTRODUCTION

POWER supplies based on paralleling a number of switching converters offer several advantages over a single high-power centralized power supply, such as low component

active-current sharing methods, i.e., the master–slave scheme and the average scheme. In addition, three control structures, namely, inner loop regulation, outer loop regulation and external control, were identified. Their classification is thus basically a systematic collection of existing schemes. Other classification works, such as Liu *et al.* [11] and Choi [12], focus on the control loop configurations of selected active current-sharing paralleling schemes.

In order to facilitate design and choice of appropriate paralleling configurations, a systematic classification of the paralleling schemes that permits a clear exposure of the structures, behaviors and limitations of all possible schemes, is needed. In this paper, we investigate the classification problem and utilize basic circuit theory to identify the basic structures and control methods of paralleled dc–dc converters. Our objective is to provide a simple classification that eliminates redundancy, includes all possible basic structures, permits comparative analysis of different structures, and hence allows systematic derivation of paralleling schemes.

Our starting point will be the two Kirchhoff's laws that dictate

Conclusion

- In this lecture, we emphasize how converters lose stability
  - the conditions under which converters lose stability
  - how the converter would behave after it loses stability
  - the resulting impact on the converter operation

- Application of control has to be considered in conjunction with the configuration of the converter and the application objectives.
  - Voltage mode control versus current mode control
  - Impact of connection configurations on choice of control methods in the case of interconnecting converter systems

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