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Hardware Architecture to Accelerate Regular Expression Matching for Network Intrusion Detection

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Venue: Room **B6605**, City University of Hong Kong
Reception starts at 4:15pm
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Abstract

At the core of a network intrusion detection system (NIDS) is a pattern matching engine. It matches packet payloads against a large set of pre-defined signatures (in the order of thousands) in real-time. The computation complexity of the pattern matching engine is exacerbated by the following three factors:

1. Increased data rate made possible by advances in optical communication technology.
2. Steadily increasing number of signatures.
3. Increasing proportion of complex signatures specified using regular expression.

In this seminar, I shall present a hardware architecture to accelerate the matching of regular expressions. The proposed method is based on extended non-deterministic finite automata. The hardware exploits the parallelism offered by content addressable memory (CAM) to achieve deterministic processing rate of one character per cycle. In addition, the space complexity of the proposed architecture is linearly proportional to the length of the regular expression.

About the Speaker

Dr. Derek Pao obtained the BSc(Eng) degree in Electrical Engineering from the University of Hong Kong, and the PhD degree in Computer Science from Concordia University, Montreal, Canada. He is currently an Associate Professor of Electronic Engineering, City University of Hong Kong. His research interests include hardware architecture for high-speed pattern matching, fast IP address lookup and packet classification algorithms, network security, and network protocols.

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