

Pulse Density Modulated Three-phase Single-stage AC-AC System for Series Resonant Load with Low Grid Current Harmonics

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Abstract—This paper proposes a direct three-phase single-stage AC-AC system based on pulse density modulation (PDM) for the series resonant load. Compared with the traditional multi-stage AC-DC-AC system, the bus capacitors among the DC stage can be eliminated, and good grid-side current quality is achieved. Unlike pulse width modulation, PDM has fewer switching times for switching devices, which can reduce switching power loss. In this paper, the high-quality grid-side current can be achieved without applying any additional power factor correction device. Furthermore, a detailed current harmonic analysis is implemented, explaining the harmonic distribution of the converter's input current. Finally, theoretical and experimental results of a single-stage AC-AC converter are presented to validate the proposed AC-AC system.

Index Terms—Direct AC-AC, three-phase single-stage converter, pulse density modulation, delta-sigma modulator.

I. INTRODUCTION

SERIES resonant load is widely equivalized in the fields of wireless power transfer, high-frequency heating [1][2], high-power telecommunication power supplies, and wireless lighting systems [3]. Their common feature is to convert low-frequency AC power [4] or DC power [5] into high-frequency AC power through power electronic conversion devices.

Compared with DC power, AC power is easier to obtain through the power grid in daily life. To get high-frequency AC power, the AC-DC-AC system is the most common structure. But it needs a DC bus capacitor, which takes up a large volume

and has a limited life. Much research has been implemented to achieve the AC-AC converter. In [6], a single-phase AC-AC converter was proposed, where the design of energy injection and free oscillation modes is applied. However, due to the inherent defect of the single-phase power supply, it has limited output capacity. Especially when the input AC voltage is crossing zero, the current flowing through the transmitting coil is very small. Consequently, the output power has large fluctuations inevitably. Based on the above method, a similar scheme for a three-phase power supply was proposed in [7][8]. However, the drive signals of MOSFETs had not been fully utilized and can be further improved. Take A-phase as an example, its switches only work when the absolute value of A-phase voltage is the maximum in the three phases. Then A-phase intermittently injected energy into the converter with a break time of 1/3 power frequency cycle, causing limited output power capacity and the issue of grid current harmonics. In [9], an AC-AC converter was proposed, which can achieve high output capacity because the supplying voltage is line voltage. Similar to [7], only the maximum line voltage at any moment was applied to the resonant load, supplying the grid with many low-order current harmonics, although the passive low-pass filters were used. In fact, the MOSFETs do not play a full role, and the complex topology can be replaced by an uncontrolled three-phase rectifier cascaded with a Class-D converter [10]. Similarly, in [11], only the maximum line voltage was used at any time, resulting in an issue of current harmonics to the grid.

To get a satisfying grid current quality, a three-phase single-stage converter with power factor correction and bus voltage control was proposed in [12]. However, in addition to the inductors and capacitors of the three-phase LC filter, three inductors of about 100 μH and two bulk DC capacitors are used in the converter, which is large in size and will increase the energy loss. For the traditional AC-DC-AC system, an additional power factor correction device and large DC capacitors are needed [13][14]. In [15]–[17], the authors achieved a satisfying grid current by controlling the conduction time of three phases during each resonant period. Unfortunately, hard switching and frequent switch actions cause serious electromagnetic interference (EMI). In addition, at any time except the dead zone time, the current of the converter should flow through at least four MOSFETs, so the conduction loss and switching loss are significant. Besides, there were also some solutions for the single-phase AC-AC

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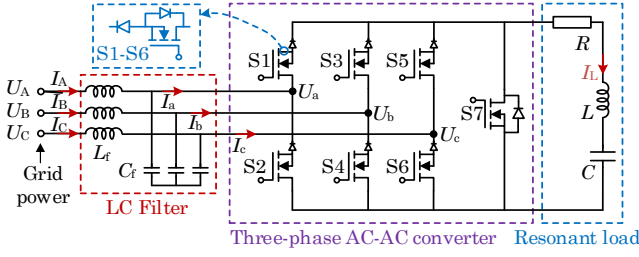


Fig. 1. Structure of pulse density modulated three-phase single-stage AC-AC system for the series resonant load.

converter [18]-[21], however, they all had the disadvantage of limited output capacity. Consequently, how to achieve a direct three-phase AC-AC converter with low grid current harmonic and high efficiency needs to be studied.

The good-quality grid-side current means that the current and its corresponding phase voltage should be synchronized as much as possible. Taking phase A as an example, phase A should provide more current to the converter when its voltage is high, and hardly provide current when its voltage crosses zero. To achieve this goal, the length of turn-on time of the A-phase bridge can be controlled to follow the A-phase voltage in each switching cycle, which is exactly the idea of [15]. Meanwhile, this method will inevitably lead to frequent switch actions, causing serious issues and additional switching loss. Apart from this method, we can also set a fixed switching period equaling the resonant period and then control the switching density of the A-phase bridge to realize a good-quality grid current. When the A-phase voltage is high, the density is large, while the density is approximately zero near the voltage zero crossing point, which is exactly the working principle of pulse density modulation (PDM).

Compared with pulse width modulation and pulse-frequency modulation, PDM ensures a wider range of soft switching, limited switching times, and availability of natural oscillation [10]. As a typical PDM method, the delta-sigma ($\Delta\Sigma$) modulator is being more and more widely used in power electronic converters. For the wireless power transfer, the authors a conducted single-phase inverter based on $\Delta\Sigma$ modulation [22], achieving high efficiency and zero voltage switching (ZVS). Besides, similar methods can also be seen in [23]. However, the analysis has been conducted only with a DC power supply. Due to the availability of AC power and the high efficiency of single-stage conversion, it is worthful to explore a three-phase PDM strategy to realize a high-quality grid current.

In this paper, a three-phase PDM method based on $\Delta\Sigma$ modulator is proposed for the direct AC-AC converter, where a high-quality grid-side current and fewer switching times can be accomplished. Compared with the existing literature, the contribution of this paper is: 1) newly applying the PDM method to a three-phase single-stage system with equivalent series resonant load and realizing low grid current harmonics and fewer switching times, 2) implementing detailed harmonic analysis to investigate the harmonic distribution of the input current of the converter and to determine the relationship between its total harmonic distortion (THD) and modulation ratio, which provides theoretical guidance for the design of LC

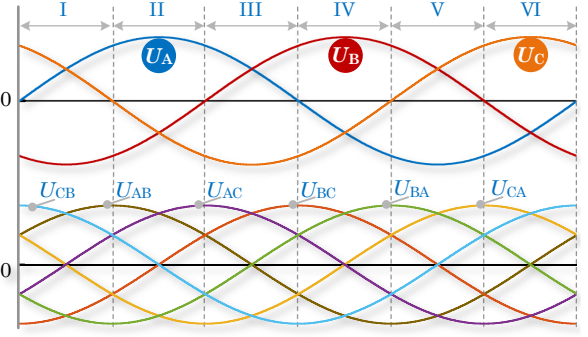


Fig. 2. Three-phase grid voltage and six corresponding sectors.

filter and the factors affecting the grid current quality, 3) achieving ZVS operation for half of the total switching times.

In Section II, the topology and the switch modes are presented to explain the principle of how the PDM achieves high-quality grid current. In Section III, harmonic analysis based on the proposed PDM method is conducted, and the detailed modulation implementation is presented. In Section IV, the experimental results are carried out to verify the proposed scheme. The conclusion is drawn in Section V.

II. TOPOLOGY AND SWITCHING PATTERN ANALYSIS

The direct three-phase AC-AC system structure is shown in Fig. 1. The converter is composed of six reverse blocking switches S1-S6 and one regular switch S7, the new circuit symbol about S1-S6 is shown in the left dashed blue dotted box, which is composed of a series connection of a MOSFET with its body diode and an additional power diode. The input of the converter is connected to the grid through an LC low-pass filter. The series resonant load is connected to the output of the converter, with the resonant capacitor and inductor represented by C and L , respectively. The ideal three-phase AC-AC system has small grid current harmonics, and the output current amplitude has slight fluctuation. According to (1), the ideal grid output power is a constant that does not change with time.

$$U_m \sin(\omega_g t) \times I_m \sin(\omega_g t) + U_m \sin(\omega_g t - 2\pi/3) \times I_m \sin(\omega_g t - 2\pi/3) + U_m \sin(\omega_g t + 2\pi/3) \times I_m \sin(\omega_g t + 2\pi/3) = 3U_m I_m / 2 \quad (1)$$

Ignoring the loss of the converter, the instantaneous power flowing into and out of the converter is equal. Based on (1), if the grid power has low fluctuation crossing the LC low-pass filter, then the output power of the converter should also be stable after filtering. Due to the energy storage of the inductor of the resonant load, the fluctuation of the load current amplitude can be considered very small when the quality factor of the resonant load is high. To simplify the analysis, this paper ignores the magnitude fluctuation of the load current I_L , and the difference between the input voltages of the converter (U_a, U_b, U_c) and grid voltages (U_A, U_B, U_C).

According to the phase position of the grid voltage, six sectors can be defined in Fig. 2. To achieve low grid current harmonics and considerable output power limit, the largest line voltage and the second largest line voltage will take turns injecting energy into the converter in every sector. Taking Sector I as an example, its switch modes are shown in Fig. 3. When S1 and S4 are ON, the current flow is shown in Fig. 3(a).

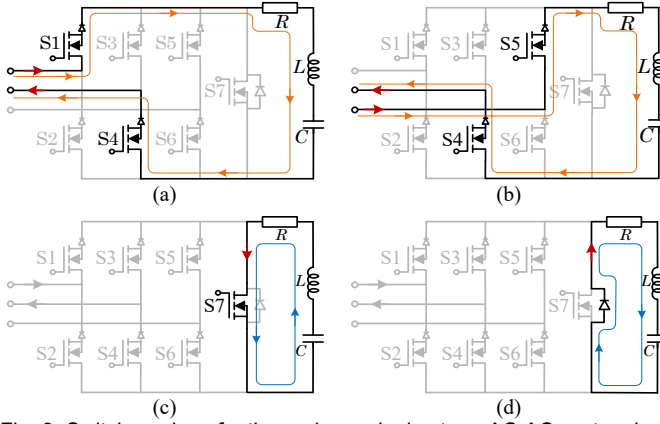


Fig. 3. Switch modes of a three-phase single stage AC-AC system in Sector I. (a) Switches S1 and S4 are ON. (b) Switches S5 and S4 are ON. (c) Switch S7 is ON. (d) All switches are OFF.

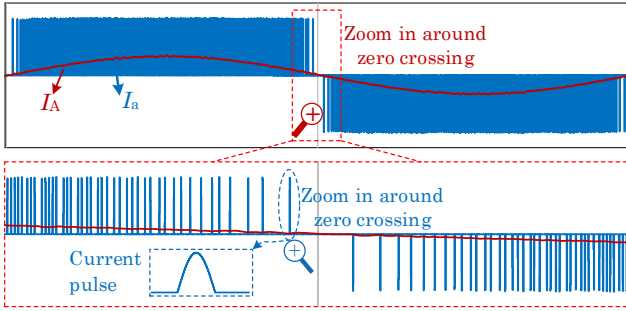


Fig. 4. When crossing LC low-pass filter, grid current I_A has a good harmonic quality if I_a is composed of many current pulses with sinusoidal density pattern.

After half of a resonant period, S1 and S4 are turned OFF, S7 is turned ON, and the current will freely oscillate along the path shown in Fig. 3(c). Then in this resonant period, phase A injects an approximately half-sine current pulse that flows out from the converter to phase B. According to the area equivalence principle and the above assumption of stable load current amplitude, if the number of current pulses flowing three phases per unit time changes sinusoidally, the grid currents (I_A , I_B , I_C) after the LC filter is approximately a sinusoidal wave. In Fig. 4, I_A is approximately sinusoidal when I_a is composed of many current pulses with a density that varies sinusoidally.

Consequently, the key to achieving low grid current harmonics is to control the number of three-phase current pulses crossing the LC filter per unit time changing along the corresponding phase voltage. In Fig. 2, U_{AB} and U_{CB} inject energy into the resonant circuit when the phase position of the grid voltage is in Sector I. For different sectors, the supply voltage and operating switches are summarized in Table I.

Fig. 5 presents the conceptual plot of the switch states. The density of the switch's pulse is proportional to the corresponding phase voltage. When U_A is positive, the density of S1 changes with the amplitude of U_A (work state). When U_A is negative, S1 always keeps OFF (idle state), and the density of S2 changes with the amplitude of U_A . And at any time, no more than two switches are turned ON. In the time interval Δt_1 , S1 and S4 are turned ON, so the positive current pulse will cross phase A and the negative current pulse will cross phase B, which corresponds to the switch mode in Fig. 3(a). At Δt_2 , a positive

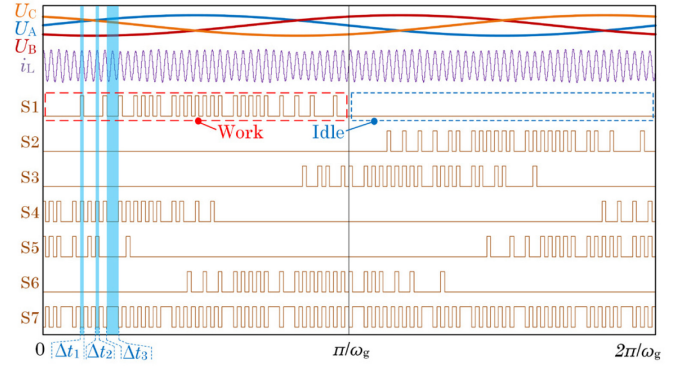


Fig. 5. A conceptual plot of three-phase input voltages, resonant current, and corresponding switch gate drive signals with PDM. The S7 gate drive signal is complementary to the S1-S6 gate drive signals.

TABLE I SUPPLY VOLTAGE AND OPERATING SWITCHES

Sector	Phase position	Supply voltage	Operating switches
I	$[0, \pi/3]$	U_{CB}, U_{AB}	S1, S4, S5, S7
II	$[\pi/3, 2\pi/3]$	U_{AB}, U_{AC}	S1, S4, S6, S7
III	$[2\pi/3, \pi]$	U_{AC}, U_{BC}	S1, S3, S6, S7
IV	$[\pi, 4\pi/3]$	U_{BC}, U_{BA}	S2, S3, S6, S7
V	$[4\pi/3, 5\pi/3]$	U_{BA}, U_{CA}	S2, S3, S5, S7
VI	$[5\pi/3, 2\pi]$	U_{CA}, U_{CB}	S2, S4, S5, S7

current pulse and a negative current pulse are produced on I_c and I_b respectively as shown in Fig. 3(b). Moreover, between the two energy injections, the load current oscillates freely between the L , C , and $S7$, which corresponds to the switching state in the time interval Δt_3 shown in Fig. 5, and its switch mode is presented in Fig. 3(c) and Fig. 3(d).

III. MODULATION METHOD AND HARMONIC ANALYSIS

A. Modulation Principle and Harmonic Analysis

To control the number of three-phase current pulses per unit time changes along its corresponding phase voltage. A PDM method based on the delta-sigma modulator is proposed. The delta-sigma modulator can be explained by the area equivalence principle [24]. In fact, at most, only two switches among S1-S6 are turned ON during one resonant period, which means the three-phase Δ - Σ modulation cannot work independently. A distribution method for avoiding simultaneous turn-ON of multiple switches in one resonant period should be introduced. To simplify the harmonic analysis, this interaction among the three phases can be ignored, and only the harmonic distribution of the A phase is presented.

Here, only I_a is analyzed, I_b and I_c are similar. Section II presents that if the density of G_1 (G_x is the drive signal of S_x) follows the positive half of U_A and the density of G_2 follows the negative half of U_A , I_a can get a series of current pulses with a density that varies sinusoidally. In Fig. 6, the sinusoidal modulation signal is synchronized with the A-phase voltage. It can be expressed by:

$$m = k \sin(\omega_g t) \quad (2)$$

where k is the modulation ratio in the range $[0,1]$, which is introduced to change pulse density and further regulate the output power.

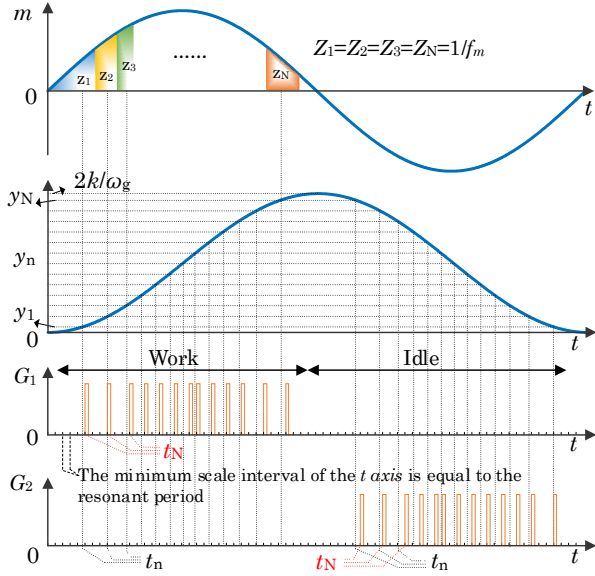


Fig. 6. Delta-sigma modulation presented by the area equivalence principle. Using this, switching time can be obtained by (7). Then the spectral distribution of I_a can be obtained by Fourier transform.

Take the positive half of the modulation signal as an example, it can be divided into N parts, and every part has an equal area ($Z_1=Z_2=Z_N$). If there is a corresponding drive signal in every part, then the switching density can follow a sinusoidal wave. When k is 1, the pulse density is maximum at the peak of the sinusoidal modulation signal, where one resonant period corresponds to one switching pulse at most. After k is introduced, $1/k$ resonant cycles correspond to a switching pulse. At the peak of the modulation signal, since the switching frequency is much higher than the power frequency, the area enclosed by the sinusoidal wave and the t -axis in $1/k$ resonant period can be considered as $1/f_m$, where f_m is the resonant frequency of the series resonant load. Therefore, the half-period modulation wave (whose area is $2k/\omega_g$) can be divided into N parts, N is $\text{floor}(2kf_m/\omega_g)$. Here, the turn-ON time t_N is set near the half of each part and can be obtained in Fig. 6, where y is the integration of modulation signal, expressed by:

$$y = \int_0^t k \sin(\omega_g t) dt \quad (3)$$

Sequence y_n can be expressed by:

$$y_n = [Z_1/2, Z_2+Z_1/2 \dots \sum_{n=2}^N Z_n + Z_1/2] \quad (4)$$

Since $Z_n=1/f_m$, y_n can also be expressed by:

$$y_n = [1/2f_m : 1/f_m : (2N-1)/2f_m] \quad (5)$$

The time sequence t_n corresponding to y_n is:

$$t_n = \arccos(1 - \omega_g y_n / k) / \omega_g \quad (6)$$

Since the switching time is the integer multiple of the half of the resonant period, the turn-ON time t_N can be expressed by:

$$t_N = \text{round}(t_n f_m) / f_m \quad (7)$$

Then the drive signal of switch S1 shown in Fig. 6 is:

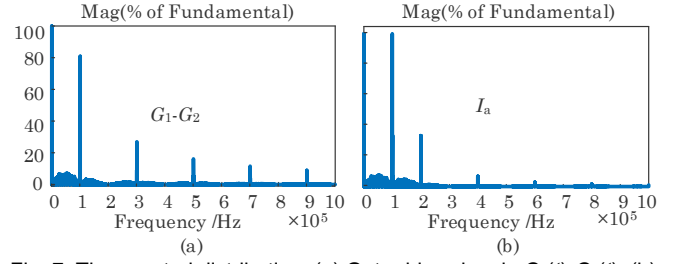


Fig. 7. The spectral distribution. (a) Gate drive signals $G_1(t)-G_2(t)$. (b) Phase A current $I_a(t)$ after grid LC filter.

$$G_1(t) =$$

$$\begin{cases} 1 & (\text{round}(t_n f_m)/f_m < t < \text{round}(t_n f_m)/f_m + 1/2f_m) \\ 0 & \text{other} \end{cases} \quad (8)$$

Similarly, the drive signal of S2 shown in Fig. 6 is:

$$G_2(t) =$$

$$\begin{cases} 1 & (\text{round}((T_g - t_n) f_m)/f_m < t < \text{round}((T_g - t_n) f_m)/f_m + 1/2f_m) \\ 0 & \text{other} \end{cases} \quad (9)$$

where T_g is the power frequency period. The amplitude of resonant load current is I_{Lm} , then I_a can be calculated by:

$$I_a(t) = I_{Lm} \sin(\omega_m t) (G_1(t) - G_2(t)) \quad (10)$$

where $\omega_m = 2\pi f_m$. Due to the round function in (8) and (9), it's difficult to express the spectral density function with the analytical method. Fig. 7(a) presents the spectral distribution ($f_m=100$ kHz, $k=0.9$, $f_g=50$ Hz) of $G_1(t)-G_2(t)$ using numerical simulation based on (5)-(10).

According to the frequency shift properties of the Fourier transform and the Euler equation:

$$\mathcal{F}[f(t) \cdot \sin(\omega_m t)] = \mathcal{F}[f(t) \cdot \frac{e^{j\omega_m t} + e^{-j\omega_m t}}{2}] = \frac{F(\omega + \omega_m) + F(\omega - \omega_m)}{2} \quad (11)$$

The frequency spectrum of I_a can be obtained and shown in Fig. 7(b), which can be regarded as the spectrum of $G_1(t)-G_2(t)$ being shifted first left by ω_m , next shifted right by ω_m , and then added together and divided by 2. According to the spectral distribution shown in Fig. 7, some general conclusions about I_a can be drawn:

- 1) In addition to the fundamental component of the power frequency and the switching frequency harmonics, there are also some even-order harmonics of the switching frequency.
- 2) When the frequency is between two adjacent multiple switching frequencies, the harmonic amplitude is low on both sides and high in the middle.

Aiming to analyze the quality of current I_a (which can be thought of as the output of I_a after low-pass filtering) affected by modulation ratio and operating frequency, I_a can be decomposed into an infinite sine series using the Fourier series.

$$I_a(t) = \frac{a_0}{2} + \sum_{m=1}^{\infty} (a_m \cos m\omega t + b_m \sin m\omega t) \quad (12)$$

$$a_m = \frac{1}{\pi} \int_{-\pi}^{\pi} I_a(t) \cos m\omega t d(\omega t) \quad (13)$$

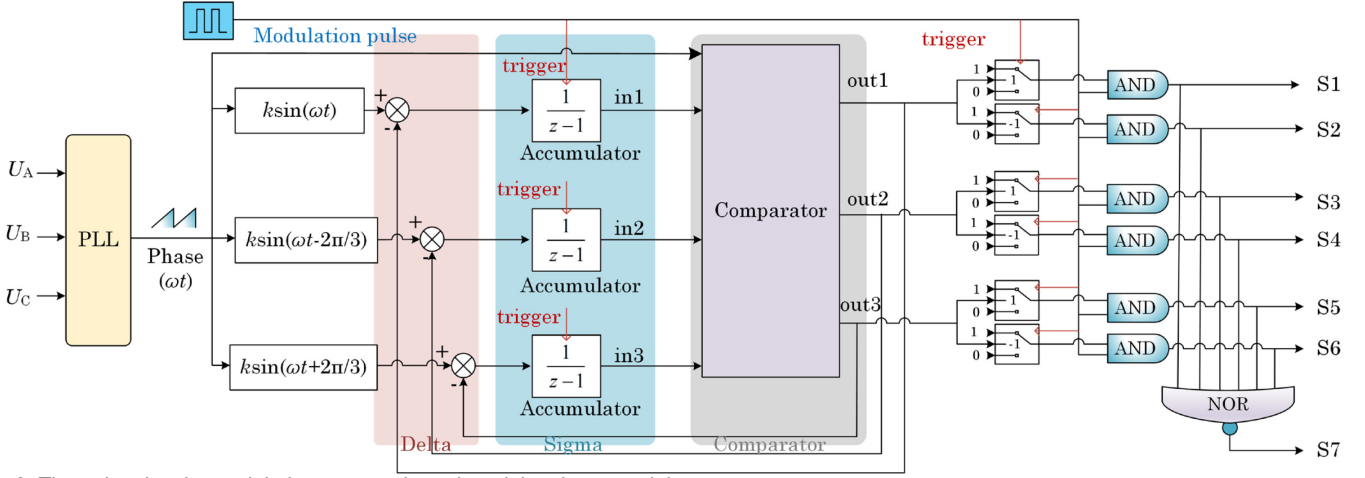


Fig. 8. The pulse density modulation strategy based on delta-sigma modulator.

$$b_m = \frac{1}{\pi} \int_{-\pi}^{\pi} I_a(t) \sin m\omega t d(\omega t) \quad (14)$$

According to Parseval's theorem [25]:

$$\frac{1}{T_g} \int_{t_0}^{t_0+T_g} I_a^2(t) dt = a_0^2 + \frac{1}{2} \sum_{m=1}^{\infty} (a_m^2 + b_m^2) \quad (15)$$

Then the THD of I_a can be expressed by:

$$THD = \sqrt{\frac{\frac{1}{T} \int_{t_0}^{t_0+T_g} I_a^2(t) dt - a_0^2 - \frac{1}{2} (a_1^2 + b_1^2)}{\frac{1}{2} (a_1^2 + b_1^2)}} \quad (16)$$

From Fig. 6, it can be found that the number of pulse currents during a power-frequency period is $4kf_m/\omega_g$. Then the left part of (15) can be obtained:

$$\frac{1}{T_g} \int_{t_0}^{t_0+T_g} I_a^2(t) dt = \frac{\omega_g}{2\pi} \times \frac{4kf_m}{\omega_g} \int_0^{\pi/\omega_m} (I_{Lm} \sin(\omega_m t))^2 dt = \frac{kI_{Lm}^2}{2\pi} \quad (17)$$

Meanwhile, the DC component of I_a can be ignored, so a_0 is 0. According to the analysis in Fig. 6, for I_a , the number of current pulses during time interval dt can be expressed by:

$$p(dt) = \frac{\sin \omega_g t dt}{2/\omega_g} \times \frac{2kf_m}{\omega_g} = kf_m \sin \omega_g t dt \quad (18)$$

Due to the high operating frequency, $\sin \omega_g t$ can be regarded as a constant during an operating period. Then:

$$\int_0^{\pi/\omega_m} \sin(\omega_m t) \sin(\omega_g t) dt = \sin(\omega_g t) \int_0^{\pi/\omega_m} \sin(\omega_m t) dt = \frac{2}{\omega_m} \sin(\omega_g t) \quad (19)$$

To simplify the analysis of the fundamental component, $I_a(t)$ can be considered as an odd function. Based on (13), it can be found that a_1 is 0. And b_1 is:

$$\begin{aligned} b_1 &= \frac{1}{\pi} \int_{-\pi}^{\pi} I_a(t) \sin \omega_g t d(\omega_g t) \\ &= \frac{2}{\pi} \omega_g \int_0^{\pi/\omega_g} I_a(t) \sin \omega_g t dt \\ &= \frac{2}{\pi} \omega_g I_{Lm} \int_0^{\pi/\omega_g} p(dt) \int_0^{\pi/\omega_m} \sin(\omega_m t) \sin(\omega_g t) dt \\ &= \frac{2}{\pi} \omega_g \frac{2}{\omega_m} I_{Lm} \int_0^{\pi/\omega_g} kf_m \sin(\omega_g t) \sin(\omega_g t) dt \\ &= \frac{kI_{Lm}}{\pi} \end{aligned} \quad (20)$$

Substitute (17) and (20) into (16), the THD of I_a is:

$$THD = \sqrt{\frac{kI_{Lm}^2}{2\pi} - \frac{k^2 I_{Lm}^2}{2\pi^2}} / \sqrt{\frac{k^2 I_{Lm}^2}{2\pi^2}} = \frac{\sqrt{k\pi - k^2}}{k} \quad (21)$$

According to (21), the THD of I_a is only related to the modulation ratio and has no relation with the switching frequency. As k decreases, THD will become higher. The harmonics of I_a are low on both sides and high in the middle between adjacent switching frequencies. Consequently, although the switching frequency does not affect the THD of I_a , it will cause the harmonic distribution to stretch along the frequency axis when it increases. Through the LC low-pass filter, higher harmonics are filtered out. Therefore, when the switching frequency increases, the harmonic distortion of the grid-side current I_A will decrease. On the contrary, the reduction of the resonant frequency will bring challenges to the design of the LC low-pass filter. A low switching frequency means a larger low-pass filter. In addition, since k does not affect the switching frequency, the harmonic distribution of I_a will not be stretched or shrank laterally. Therefore, with the decrease of k , the harmonic distortion of the grid-side current I_A will also become larger.

Considering that between adjacent switching frequencies, the harmonics of I_a are low on both sides and high in the middle, and the harmonic distribution is very wide, the cutoff frequency of the three-phase LC filter should be as low as possible. The lower the cutoff frequency, the THD of the grid side current will be better, but the required passive components will also be

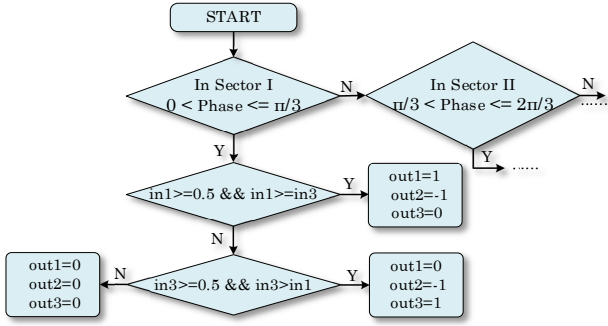


Fig. 9. Flow diagram of the comparator. Only the case of voltage phase in sector I is presented, the same operation for other sectors.

larger. Considering the trade-off, it is recommended that the cut-off frequency of the passive filter be designed to be lower than 1/20 of the resonant frequency.

B. Modulation Method

Based on the above analysis of delta-sigma modulation and the assumption of the constant output current amplitude, the low harmonic distortion characteristic of the grid-side current has been verified in principle. The proposed three-phase PDM strategy based on the $\Delta-\Sigma$ modulator is shown in Fig. 8. Firstly, the real-time phase of the three-phase grid voltage is calculated by a phase-locked loop (PLL). The $\Delta-\Sigma$ modulator consists of three parts, which are the delta module, the sigma module, and the comparator. Then the delta module makes a subtraction between the input sine modulation signal and the pulse output by the comparator. The output of the delta module is the input of the accumulator, and the accumulator is triggered to integrate at the rising edge of the modulation pulse. Considering that at any time, no more than two switches (S1-S6) are turned ON. Therefore, the three-phase $\Delta-\Sigma$ modulation cannot work independently. It is necessary to compare the outputs of the three-phase integrators to avoid the simultaneous action of multiple switches. Fig. 9 shows a simple distribution method by taking Sector I as an example. The three outputs of the delta-sigma modulator are converted into driving signals and distributed to seven switches through logic operations, which are also triggered by the rising edge of the modulation pulse.

Fig. 10 presents the generation of the modulation pulse. Theoretically, the modulation pulse is a square wave with a duty cycle of 50%. However, since the DIODEs in series with the MOSFETs prevent the reverse flow of current, the turn-ON moments of S1-S6 need to be around or after the zero-crossing time when load current I_L changes from negative to positive to avoid excessive reverse flow current, which can accumulate charge, and then cause overvoltage breakdown of the diode and S7. In addition, to realize the ZVS of the S7, S7 should be turned ON before the zero-crossing time when the load current I_L changes from positive to negative, so that the parasitic output capacitance of S7 can be discharged during the dead time, and then zero-voltage turn-ON can be realized.

As shown in Fig. 10, I_L is sampled, and a timer is used to control switching time. The period value of the timer is equal to the resonant period of the series load. The timer value should be cleared when the load current crosses zero from negative to positive. The preset reference value is set slightly less than half

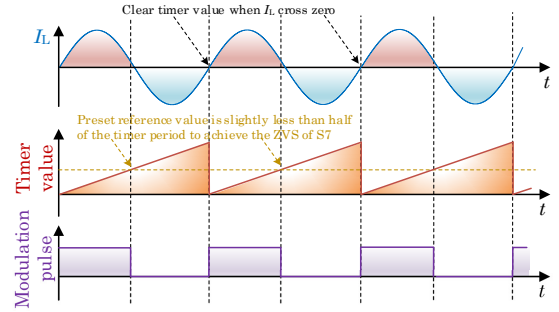


Fig. 10. The generation of modulation pulse. The rising edge of the modulation pulse is around or after the nearest zero crossing point of I_L . Its falling edge is before the nearest zero-cross point of I_L .

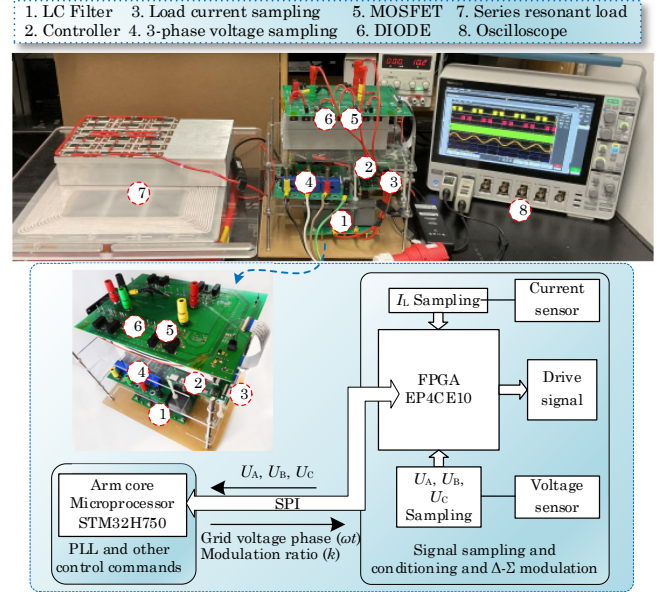


Fig. 11. Experimental prototype of the proposed PDM three-phase single stage AC-AC system with Arm core Microprocess and FPGA.

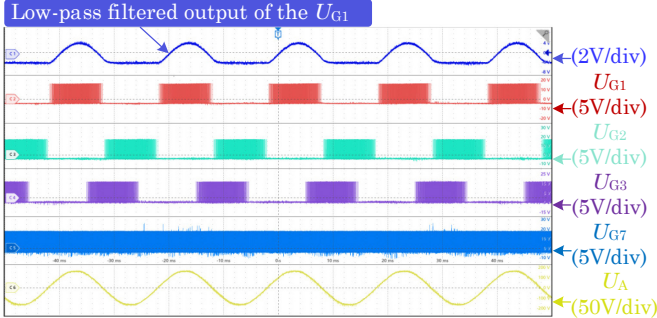
of the timer period to achieve the ZVS of S7. The modulation pulse is generated by comparing the timer value with the preset reference value.

C. Analysis of Switching Times

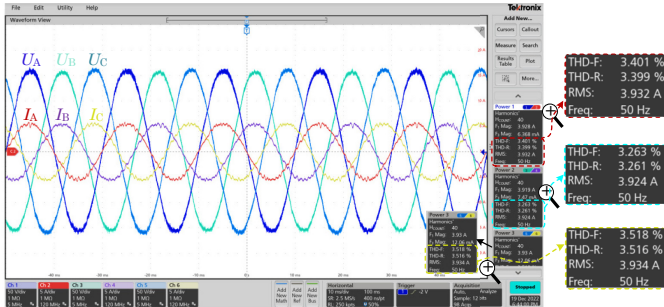
When the converter is working, S7 bears the line voltage when it is turned OFF. But for the switches of S1-S6, the line voltage will be applied to the two switches simultaneously when S7 is turned ON. In addition, in Sector I, whether S1 and S4 are turned ON, or S4 and S5 are turned ON, S4 always works (continuous operations for turn ON and OFF) but S1 and S5 work and are in an idle state (no switching operations) in turn. Hence, S4 can stay ON during this period. Similarly, in Sector II, S1 can also stay ON. It can be regarded that there is only one switching action when two switches among S1-S6 are turned ON simultaneously. In Fig. 6, N is $2kf_m/\omega_g$ ignoring the floor function. In a power-frequency period, S1 turns ON N times and turns OFF N times. It is the same with S2-S6. Due to the complementary properties of S7, S7 will turn ON $3N$ times and turn OFF $3N$ times. Only the turn-ON times of the converter are counted, the total switching times of the converter are only $12kf_m/\omega_g$ ($6N$) times.

TABLE II SYSTEM PARAMETERS

Parameter	Description	Typical Value
U_m	Three-phase voltage amplitude	$110\sqrt{2}$ V
f_r	Resonant frequency	100 kHz
R	Resistance of the resonant load	7.6 Ω
L	Inductance of the resonant load	190 μ H
R_{ACR}	AC resistance of the resonant inductor	0.6 Ω
C	Capacitance of the resonant load	13 nF
L_f	Inductance of the three-phase LC filter	2 mH
C_f	Capacitance of the three-phase LC filter	6 μ F

Fig.12. Measured waveforms of low-pass filtered output, the drive signals of MOSFETs (S1, S2, S3, and S7) ($k=1$), and phase A voltage.

THD-F: Phase-A, 3.401%; Phase-B, 3.263%; Phase-C: 3.518%

Fig.13. THD measurement of voltage and current waveforms at the grid side ($k=1.0$), where all measured THDs are less than 3.6%.

In [15][16][17], a modulation method based on vector composition was presented. Each switch is composed of two bidirectional MOSFETs, it can also be regarded that there is only one switching action when the two bidirectional MOSFETs are turned ON simultaneously. The output voltage of the converter changes six times in a resonant period. Considering that when the output voltage is switched from zero to line voltage, there will be two switching actions. And this process will occur twice in a resonant period. Consequently, the traditional matrix converter has 8 switching actions during each resonant period and $16\pi f_m/\omega_g$ switching times during a power-frequency period. According to the conclusion of ZVS and ZCS can reduce switching loss [26] and lower switching frequency (fewer switching times during fixed time) can reduce EMI level [27][28], the converter with the proposed three-phase PDM strategy in the paper has fewer switching times and lower switching losses and better EMI compared to the traditional three-phase matrix converter because of the fewer switching times and ZVS of S7 and ZCS (turn ON and turn OFF near the crossing zero point of I_L). In the appendix, the power loss of the converter is presented by mathematical equations.

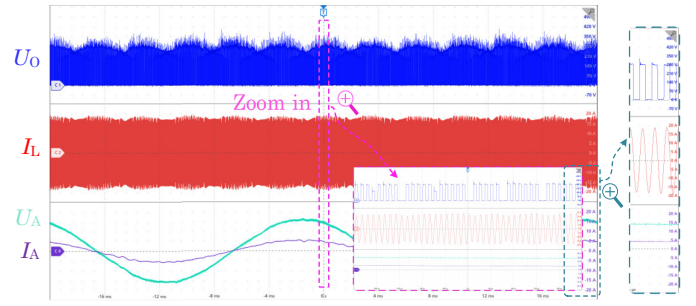
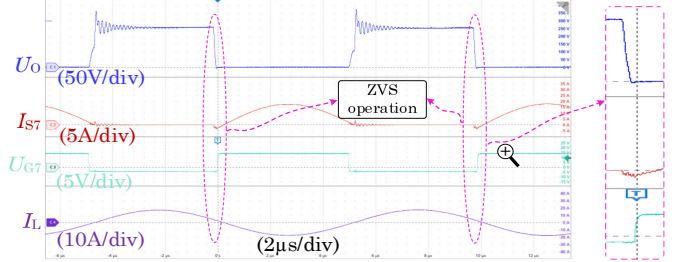
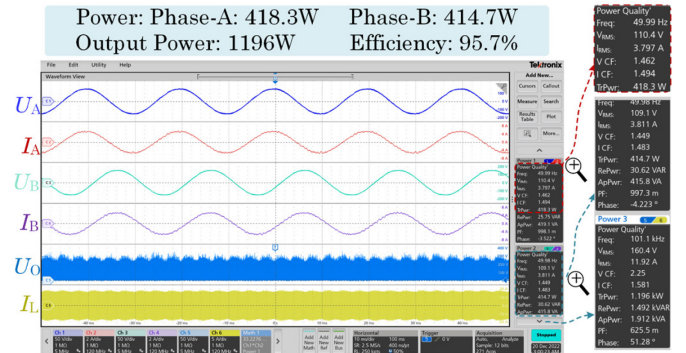
Fig.14. Voltage and current waveform of phase A and output voltage and resonant current waveforms of the converter ($k=1$).

Fig.15. ZVS operation of S7, which is essential to reduce switching loss and EMI as its switching times are half of the total switching times.

Fig.16. System efficiency measurement of the converter ($k=1$), where the efficiency can reach up to 95.7%.

IV. EXPERIMENTAL VERIFICATION

A. Experimental Setup

Experimental parameters are shown in Table II. Considering that most induction heating devices have a frequency range of 100 kHz to 200 kHz and wireless power transfer with an 80 kHz-90 kHz frequency. The resonant frequency is set at 100 kHz for verification. Since the large capacitance of the LC filter will generate considerable harmonic current under the effect of the three-phase grid voltage harmonics, considering the volume of capacitors and inductors comprehensively, the capacitance is chosen as 6 μ F then the inductance was selected as 2 mH based on the cutoff frequency. Fig. 11 presents the experimental prototype. The main controller is composed of STM32H750+EP4CE10. EP4CE10 FPGA implements Δ - Σ modulation, STM32H750 Arm core Microprocessor processes PLL, and other control commands. C3M0060065K and C4D30120H are respectively used as SiC MOSFETs and SiC DIODEs in the power circuit. S7 is connected in parallel by a MOSFET and diode. Experimental results are acquired by Tektronix

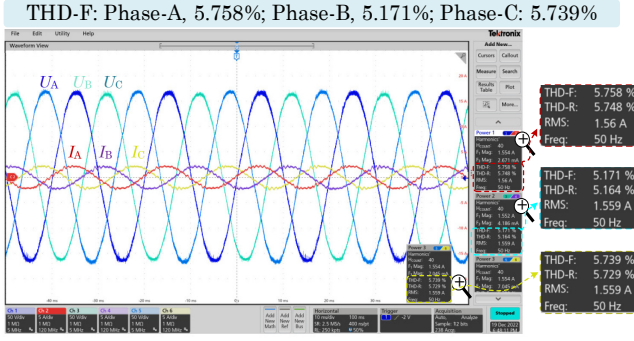


Fig.17. THD measurement of voltage and current waveforms at the grid side ($k=0.6$).

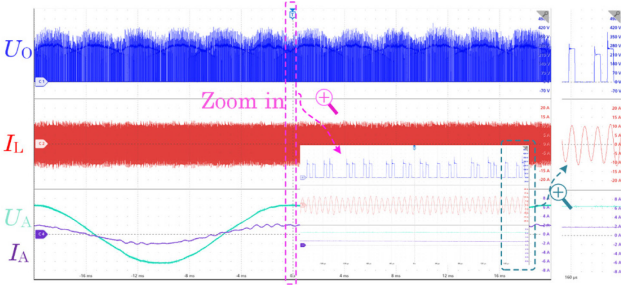


Fig.18. Voltage and current waveform of phase A and output voltage and resonant current waveforms of the converter ($k=0.6$).

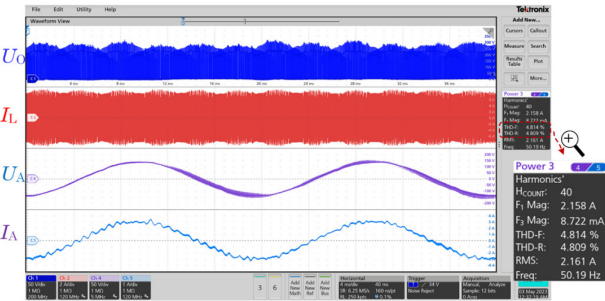


Fig.19. THD measurement of voltage and current waveforms at the grid side ($k=1$, $R=15\Omega$).

oscilloscope MSO46, differential probe THDP0200, and current probe TCP0030A.

B. Experimental Results

The drive signals ($k=1$) are shown in Fig. 12. The experimental waveform is consistent with the analysis in Fig. 5. U_{G1} , U_{G2} , U_{G3} , and U_{G7} represent the drive voltage of S1, S2, S3, and S7, respectively. Ignoring the steady-state error of the PLL, S1 works and S2 keeps idle when U_A is positive. U_{G3} lags behind U_{G1} by 120 degrees. Channel 1 presents the voltage waveform of U_{G1} after low-pass filtering, which shows that the pulse density of S1 changes sinusoidally when U_A is positive.

Fig. 13 presents the three-phase voltage and current at the grid side. It can be found that grid-side currents have good quality with low THDs of only 3.401%, 3.263%, and 3.518%, respectively. The grid current slightly leads the corresponding phase voltage due to the capacitance of the LC filter.

The output voltage U_O of the converter and the resonant current I_L are shown in Fig. 14. The middle area of the figure is enlarged, which corresponds to Sector II in Table I. The supply voltage is alternately switched between U_{AC} and U_{AB} . Meanwhile,

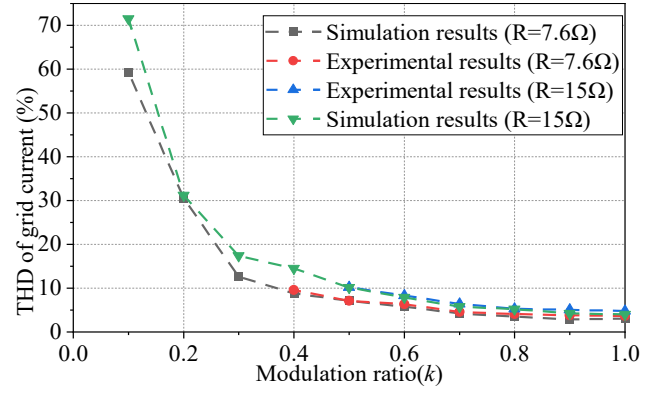


Fig.20. Influence of modulation ratio on grid current THD when modulation ratio k varies from 0 to 1.0 for different R .

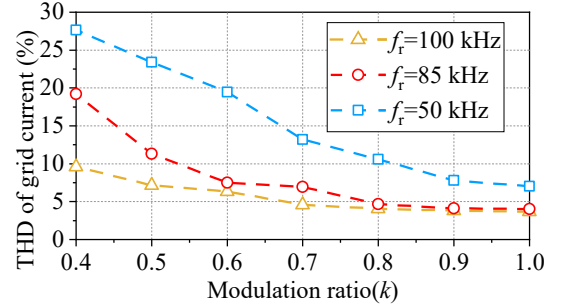


Fig.21. Grid current THD with different resonant frequency f_r .

the ZVS operation of S7 is presented in Fig. 15. Before the turn-ON signal of S7 arrives, the parasitic output capacitance of S7 discharges during the dead time, then the voltage U_O across the drain and source of S7 slowly decreases to zero, and then the ZVS operation is realized. Fig. 16 presents the efficiency of the converter (Efficiency is defined as the ratio of the output power of the converter to the input power, taking into account the losses of the LC filter). Due to the limitation of the number of oscilloscope channels, only the A-phase power, B-phase power, and output power are tested. Efficiency can be calculated as 95.7%. Based on the harmonic analysis of Section III, grid current quality will be degraded when the modulation ratio decreases. Grid current THD grows to 5.768%, 5.171%, and 5.739% as shown in Fig. 17 when k reduces to 0.6. Its output voltage and resonant current waveforms of the converter is shown in Fig. 18.

When the resistance of the series resonant load increases, the amplitude fluctuation of the output current of the converter will also become larger, which will affect the THD of the grid-side current to a certain extent. Fig.19 presents that the THD of the grid current will grow to 4.814% compared with 3.401% in Fig. 13 when the resistance increases to 15Ω . Fig. 20 shows the variation curve of THD with modulation ratio for different resistance. Since the grid-side current is too small when k is low, the oscilloscope cannot measure its THD, the simulation data of Simulink is also shown in Fig. 20. When the modulation ratio is very small, the grid-side current distortion is very serious and the reactive current generated by the LC filter will account for the main part of the grid current. Consequently, the pulse density modulation method based on the delta-sigma modulator is suitable for the situation when the modulation ratio k is large. Fortunately, neglecting the amplitude fluctuation of the load

TABLE III COMPARISON WITH OTHER STUDIES ABOUT AC-AC OR AC-DC-AC CONVERTER FOR SERIES RESONANT LOAD

	Conversion type	Power supply	DC side capacitors	Devices need	Resonant frequency	THD	Power	Efficiency	Soft switching
[5]	AC-DC-AC	Three phase	Yes	12 MOSFETs	85kHz	Not reported	25000W	91%	ZVS
[6]	AC-AC	Single phase	No	4 MOSFETs	30kHz	Not reported	12.5W	Not reported	No
[8]	AC-AC	Three phase	No	8 MOSFETs	50kHz	poor	300W	85%	No
[9]	AC-AC	Three phase	No	7 MOSFETs 6 diodes	85kHz	poor	267W	89.7%	ZCS
[12]	AC-DC-AC	Three phase	Yes	4 MOSFETs 6 diodes	85kHz	3.5%	3300W	95.4% (AC-AC part)	ZVS
[15][16]	AC-AC	Three phase	No	12 MOSFETs	85kHz	9%	2.5kW	90%	No
[19]	AC-AC	Single phase	No	8 MOSFETs	35kHz	19%	95W	92%	ZCS
[20]	AC-AC	Single phase	No	8 MOSFETs	20kHz	4.8%	1000W	89.6%	No
[21]	AC-AC	Single phase	No	8 MOSFETs	50kHz	4.5%	1200W	Not reported	ZVS
This paper	AC-AC	Three phase	No	7 MOSFETs 6 diodes	100kHz	3.4%	1200W	95.7% (AC-AC part)	Half ZVS ZCS

current, the output power is approximately proportional to k^2 [29]. Therefore, the grid-side current quality in most power situations is reasonably satisfying. Besides, for the wireless power transfer, keeping the converter on the transmit side works at a higher modulation ratio, the output power can also be regulated by only controlling the receiving side. When the resistance increases from 7.6Ω to 15Ω , the grid current quality will be affected to a small extent. The reason for this is that as the resistance increases, the converter output current's fluctuation also increases. Consequently, the assumption made in the article, which relies on a constant amplitude of the load current, will be impacted to a certain degree, thus affecting the grid-side current THD to some extent. However, the impact is not considerable, and the assumption of disregarding load current fluctuations remains reasonable.

Fig.21 presents the experimental results of the grid current THD when the resonant frequency of the series resonant load changes. The resonant frequency is changed by changing the value of the resonant capacitor C . When the resonant frequency increases, the grid-side current quality is improved. Especially when the resonant frequency is only 50kHz, it can be seen that there will still be some distortion in the grid-side current. Therefore, for lower-frequency applications, the method requires a larger passive filter to obtain a satisfactory grid-side current.

C. Comparison with Other Studies

Table III shows the comparison results between the proposed three-phase AC-AC converter and the conventional scheme. Compared with the two-stage AC-DC-AC converter [5][12], the main benefit is the elimination of the DC side capacitors, which is good for system lifetime and power density. Compared with the single-phase AC-AC converter [19][20][21], the difference is that the paper proposes a converter based on the three-phase power supply, which can have a larger output capacity. For the existing research on the three-phase converter, it is challenging to get a grid-side current with low harmonics

[8][9]. However, the proposed modulation method based on PDM can achieve a good grid current. Besides, the method of the paper has fewer switching times. Although the ZVS of all switches has not been realized, it has been improved a lot compared with the hard switching multiple times in one resonant cycle [15][16].

V. CONCLUSION

In this paper, a pulse density modulated three-phase single-stage AC-AC system for series resonant load was proposed. The PDM modulation principle and harmonic analysis have been explored in detail. Moreover, the design method, switching time, ZVS operation, and experimental validations have been presented. The following conclusions can be drawn.

- 1) Due to the energy storage of the LC resonant tank, the grid current with low harmonics can be obtained by controlling the sinusoidal change of switching density.
- 2) The grid side current has small harmonic distortion. With the decrease in the modulation ratio, the current quality will be degraded. It is recommended that the modulation ratio is not less than 0.5.
- 3) The system has fewer switching times. Only $12k_f/\omega_g$ times of turn-ON and $12k_f/\omega_g$ times of turn-off in a power frequency cycle.
- 4) The ZVS of S7 can be realized. The switching times of S7 are half of the total switching times of the converter.

Realizing the ZVS of all switching will be studied in the future, and in-depth exploration will be conducted from two aspects: optimizing the topology and refining the modulation method.

VI. APPENDIX

This section provides a loss analysis of the converter. Assume that the current flowing through the series resonant load is a sinusoidal current with amplitude I_{Lm} .

The loss of the converter is composed of conduction loss and switching loss of MOSFETs and diodes. In the proposed

scheme, the positive half-cycle output current flows through the two switches (among S1-S6) for 3N times in a power period. The power loss of MOSFETs (among S1-S6) can be calculated by:

$$\begin{aligned} P_{\text{cond_MOS(S1-S6)}} &= 6f_g N \int_0^{T_r/2} r_{\text{DS}} i_L^2(t) dt \\ &= 6f_g N \int_0^{T_r/2} r_{\text{DS}} I_{\text{Lm}}^2 \sin^2(\omega_m t) dt \\ &= 3\pi f_g N r_{\text{DS}} I_{\text{Lm}}^2 / \omega_m \end{aligned} \quad (22)$$

Similarly, the conduction loss of diodes (among S1-S6) can be expressed by:

$$\begin{aligned} P_{\text{cond_D}} &= 6Nf_g \int_0^{T_r/2} v_{\text{AK}}(t) i_c(t) dt \\ &= 6Nf_g \int_0^{T_r/2} (V_f + r_D I_{\text{Lm}} \sin(\omega_m t)) I_{\text{Lm}} \sin(\omega_m t) dt \\ &= 12Nf_g V_f I_{\text{Lm}} / \omega_m + 3Nf_g \pi r_D I_{\text{Lm}}^2 / \omega_m \end{aligned} \quad (23)$$

where r_{DS} is the on-state resistance of MOSFETs. v_{AK} , V_f , and r_D are the anode-cathode voltage, threshold voltage and on-state resistance of diodes.

Besides, the negative half-cycle output current flows through the parasitic diode of S7 3N times. And full cycle output current will flow through S7 up to f_r/f_g -3N times in a power period. Consequently, the conduction loss of S7 can be expressed by:

$$\begin{aligned} P_{\text{cond_S7}} &= 3Nf_g \int_0^{T_r/2} (V_f + r_D I_{\text{Lm}} \sin(\omega_m t)) I_{\text{Lm}} \sin(\omega_m t) dt \\ &\quad + (f_r - 3Nf_g) \int_0^{T_r} r_{\text{DS}} I_{\text{Lm}}^2 \sin^2(\omega_m t) dt \\ &= 6Nf_g V_f I_{\text{Lm}} / \omega_m + 1.5N\pi f_g r_D I_{\text{Lm}}^2 / \omega_m + (f_r - 3Nf_g) \pi r_{\text{DS}} I_{\text{Lm}}^2 / \omega_m \end{aligned} \quad (24)$$

The switching loss of S7 can be ignored because the ZVS operation, the switching loss of MOSFETs (S1-S6) can be expressed by:

$$P_{\text{SW_MOS}} = 3Nf_g \int_0^{\tau_{\text{sw}}} v_{\text{ds}}(t) i_d(t) dt \quad (25)$$

where τ_{sw} , v_{ds} and i_d are switching time, drain to source voltage and current crossing MOSFETs. Consequently, the total power loss of the proposed converter is given as follows:

$$P_{\text{LOSS}} = P_{\text{cond_MOS(S1-S6)}} + P_{\text{cond_D}} + P_{\text{cond_S7}} + P_{\text{SW_MOS}} \quad (26)$$

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