IEEE International Conference on Field-Programmable Technology

Technical Programme

Co-organizers:
The Department of Computer Science and Engineering, CUHK
The IEEE Hong Kong Section Computer Chapter

Conference sponsors:
The Croucher Foundation
The IEEE Hong Kong Section Electron Devices Society
Chung Chi College, CUHK

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Altera Corporation

Celoxica

Micom Tech Ltd.

Quicksilver Technology

SUGA Electronics Ltd.

Xilinx Inc.

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0845 – 0900	**Special Keynote: Paul Y.S. Cheung**	ELB LT3
0900 – 0945	**Keynote: Tsugio Makimoto, Sony Corp.**	ELB LT3
0940 – 1030	Session 1: Networking Applications	ELB LT3
1030 – 1100	Coffee and Poster Session 1	ELB 1/F
1030 – 1110	Session 2: Run-time Reconfiguration Technology	ELB LT3
1250 – 1415	Lunch at SCR (shuttle bus)	SCR
1415 – 1455	**Keynote: Patrick Lysaght, Xilinx Inc.**	ELB LT3
1455 – 1610	Session 3: Signal and Matrix Processing	ELB LT3
1610 – 1650	Tea and Poster Session 2	ELB 1/F
1650 – 1830	Session 4: FPGA-based Applications	ELB LT3
Tuesday 17 December 2002		
0900 – 0940	**Keynote: Michael Flynn, Stanford University**	ELB LT3
0940 – 1030	Session 5: Reconfigurable and Memory Architectures	ELB LT3
1030 – 1110	Coffee and Poster Session 3	ELB 1/F
1110 – 1250	Session 6: High-Level Design Tools	ELB LT3
1250 – 1300	Special Presentation: Masahiro Fujita	ELB LT3
1300 – 1415	Lunch at Chung Chi Staff Club	Staff Club
1415 – 1455	**Keynote: Paul Master, Quicksilver Technology**	ELB LT3
1455 – 1610	Session 7: Reconfigurable Circuits and Devices	ELB LT3
1610 – 71650	Tea and Poster Session 4	ELB 1/F
1650 – 1830	Session 8: Technology Mapping and Layout Tools	ELB LT3
1915	Shuttle bus leaves Esther Lee Building for Ferry Pier	ELB G/F
1945	OR Meet and embark at Hung Hom Ferry Pier	Ferry Pier
2000 – 2330	**Conference Dinner (Hong Kong Harbour Cruise)**	On the Cruise
Wednesday 18 December 2002		
0900 – 0945	**Keynote: Erik Cleage, Altera Corp.**	ELB LT3
0945 – 1030	Session 9: Debugging Methods	ELB LT3
1030 – 1110	Coffee and Poster Session	ELB 1/F
1110 – 1250	Session 10: Instruction Processors and Systems	ELB LT3
1250 – 1300	Closing Remarks	ELB LT3
1430 – 1730	Asia-Pacific Technology Forum	ELB LT3
Thursday 19 December 2002		
0930 – 1130	Tutorial Session 1: Xilinx	SB LT2
1300 – 1500	Tutorial Session 2: Celoxica	SB LT2
1600 – 1800	Tutorial Session 3: Altera	SB LT2

Legends: ELB - Esther Lee Building, SB - Sino Building, SCR – Staff Common Room

Monday 16 December 2002

0800-1830 - Registration

0830-0845 - Welcome

0845-0900
Special Keynote: Paul Y.S. Cheung, Policy Advisor, Innovation and Technology Commission, Hong Kong Government
Title: Technology Research and Development in Hong Kong: Hype or Reality

0900-0940
Keynote: Tsugio Makimoto, Sony Corporation
Title: The Hot Decade of Field Programmable Technologies

Session 1: Networking Applications

Session Chair: S.J.E. Wilton, University of British Columbia

0940-1005
Paper : Real-time Packet Editing Using Reconfigurable Hardware for Active Networking
Authors : T. Miyazaki, T. Murooka, N. Takahashi, M. Hashimoto

1005-1030
Paper : Implementation of an FPGA Based Accelerator for Virtual Private Networks
Authors : O.Y.H. Cheung and P.H.W. Leong

1030-1110 - Coffee and Poster Session 1

Session 2: Run-time Reconfiguration Technology

Session Chair: C.C. Cheung, Chinese University of Hong Kong

1110-1135
Paper : Compiling Run-Time Parametrisable Designs
Authors : A. Derbyshire and W. Luk

1135-1200
Paper : Adaptive FIR Filter Architectures for Run-Time Reconfigurable FPGAs
Authors : T. Rissa, R. Uusikartano and J. Niittylahti

1200-1225
Paper : A Methodology for Design of Run-time Reconfigurable Systems
Authors : G. Lee and G. Milne

1225-1250
Paper : Resource-Aware Run-time Elaboration of Behavioural FPGA Specifiations
Authors : U. Malik, K. So and O. Diessel

1250-1415 - Lunch

1415-1455
Keynote: Patrick Lysaght, Xilinx, Inc.
Title: FPGAs as Meta-platforms for Embedded Systems

Session 3: Signal and Matrix Processing

Session Chair: O. Diessel, University of New South Wales

1455-1520
Paper : High-Speed Programmable Sum-of-Power-of-Two (SOPOT) Finite-Duration Impulses Response (FIR) Filters
Authors : K.S. Yeung and S.C. Chan

1520-1545
Paper : FPGA-based System-level design framework based on the IRIS synthesis tool and System Generator
Authors : Y. Yi and R. Woods

1545-1610
Paper : Area and Time Efficient Implementation of Matrix Multiplication on FPGAs
Authors : J. Jang, S. Choi and V.K. Prasanna

1610-1650 - Tea and Poster Session 2

Session 4: FPGA-based Applications

Session Chair: T. Rissa, Nokia

1650-1715
Paper : A System Level Implementation of Rijndael on a Memory-slot based FPGA Card
Authors : D.K.Y. Tong, P.S. Lo, K.H. Lee and P.H.W. Leong

1715-1740
Paper : FPGA-Based Cloud Detection for Real-Time Onboard Remote Sensing
Authors : J.A. Williams, A.S. Dawood and S.J. Visser

1740-1805
Paper : An FPGA-Based Processor for Shogi Mating Problems
Authors : Y. Hori, M. Sonoyama and T. Maruyama

1805-1830
Paper : Population based Ant Colony Optimization on FPGA
Authors : M. Guntsch, B. Scheuermann and H. Schmeck

Tuesday 17 December 2002

0800-1830 - Registration

0900-0940
Keynote: Michael J. Flynn, Stanford University
Title: Programmed Solutions: The step beyond Programmed Logic

Session 5: Reconfigurable and Memory Architectures

Session Chair: O. Mencer, Bell Laboratories

0940-1005
Paper : Clustered Programmable-Reconfigurable Processors
Authors : D.B. Gottlieb, J.J. Cook, J.D. Walstrom, S. Ferrera, C. Wang and N.P. Carter

1005-1030
Paper : Implementing Logic in FPGA Embedded Memory Arrays: Heterogeneous Memory Architectures
Authors : S.J.E. Wilton

1030-1110 - Coffee and Poster Session 3

Session 6: High-Level Design Tools

Session Chair: A. Fong, City University of Hong Kong

1110-1135
Paper : Optimising and Adapting High-Level Hardware Designs
Authors : J.G.F. Coutinho and W. Luk

1135-1200
Paper : Floating-Point Bitwidth Analysis via Automatic Differentiation
Authors : A.A. Gaffar, O. Mencer, W. Luk, P.Y.K. Cheung and N. Shirazi

1200-1225
Paper : DRESC: A Retargetable Compiler for Coarse-Grained Reconfigurable Architectures
Authors : B. Mei, S. Vernalde, D. Verkest, H.D. Man and R. Lauwereins

1225-1250
Paper : A Prolog Based Hardware Description Environment
Authors : K. Benkrid, S. Belkacemi and D. Crookes

1250-1300
Special Session: Masahiro Fujita, The University of Tokyo
Title: Presentation on FPT'03 (Tokyo)

1300-1415 – Lunch
Shuttle bus leaves for SCR lunch from Esther Lee Building
The bus will run twice and ferry guests back after lunch.

1415-1455
Keynote: Paul Master, Quicksilver Technology
Title: The Next Big Leap in Reconfigurable Systems

Session 7: Reconfigurable Circuits and Devices

Session Chair: H. Lau, University of Hong Kong

1455-1520
Paper : Gigahertz SiGe BiCMOS FPGAs with new architectures and novel power management schemes
Authors : K. Zhou, Channakeshav, J. Guo, S. Liu, R.P. Kraft, C. You and J.F. McDonald

1520-1545
Paper : Evolutionary Analog Circuit Design on a Programmable Analog Multiplexer Array
Authors : C.C. Santini, J.F.M. Amaral, M.A.C. Pacheco, and M.M. Vellasco

1545-1610
Paper : An Optically Differential Reconfigurable Gate Array and its Power Consumption Estimation
Authors : M. Watanabe and F. Kobayashi

1610-1650 - Tea and Poster Session 4

Session 8: Technology Mapping and Layout Tools

Session Chair: T. Kok, HK University of Science & Technology

1650-1715
Paper : A Technology Mapping Algorithm for CPLD Architectures
Authors : S. Chen, T.T. Hwang and C.L. Liu

1715-1740
Paper : Power-Aware Technology Mapping for LUT-Based FPGAs
Authors : J.H. Anderson and F.N. Najm

1740-1805
Paper : Synthesizing Datapath Circuits for FPGAs with Emphasis on Area Minimization
Authors : A. Ye, J. Rose and D. Lewis

1805-1830
Paper : The Effect of Cluster Packing and Node Duplication Control in Delay Driven Clustering
Authors : M.E. Dehkordi and S.D. Brown

2000-2330 - Conference Dinner (Hong Kong Harbour Cruise)
1715 - Shuttle bus leaves Esther Lee Building for Ferry Pier
1745 – OR Meet and embark at Hung Hom Ferry Pier

Wednesday 18 December 2002

0800-1250 - Registration

0900-0940
Keynote: Erik Cleage, Altera Corporation
Title: The Economics of FPGAs, ASSPs & ASICs

Session 9: Debugging Methods

Session Chair: Y.L. Wu, Chinese University of Hong Kong

0940-1005
Paper : Debug Methodology for Arithmetic Circuits on FPGAs
Authors : M. Kubo and M. Fujita

1005-1030
Paper : Debug Methods for Hybrid CPU/FPGA Systems
Authors : E. Roesler and B. Nelson

1030-1110 - Coffee and Poster Session

Session 10: Instruction Processors and Systems

Session Chair: S.C. Chan, University of Hong Kong

1110-1135
Paper : Scalable Acceleration of Inductive Logic Programs
Authors : A. Fidjeland, W. Luk and S. Muggleton

1135-1200
Paper : A Fine-Grained Reconfigurable Logic Array Based on Double Gate Transistors
Authors : P. Beckett

1200-1225
Paper : A Co-simulation Study of Adaptive EPIC Computing
Authors : V.S. Gheorghita, W. Wong, T. Mitra and S. Talla

1225-1250
Paper : System on Programmable Chip for Real-Time Control Implementations
Authors : D.L.S. Pradel, S.R. Jones and R.M. Goodall

1250-1300 - Closing Remarks

Thanks for joining the FPT'02 conference!
We look forward to seeing you in FPT'03 in Japan.

POSTER SESSION 1

Paper : A Reconfigurable Vision System for Real-time Applications
Authors : C.T. Huitzil, S.E.M. Rueda and M.A. Estrada

Paper : Loseless Data Compression Programmable Hardware for High-speed Data Networks
Authors : J.L. Nunez and S. Jones

Paper : A Multiplier-less FPGA Core for Image Algebra Neighbourhood Operations
Authors : K. Benkrid

Paper : Multi-hop Routing of Multi-terminal Nets for Evaluation of Hybrid Multi-FPGA Boards
Authors : S.C. Jain, A. Kumar and S. Kumar

Paper : Serial-Parallel Tradeoff Analysis Of All-Pairs Shortest Path Algorithms In Reconfigurable Computing
Authors : S.T. Mak and K.P. Lam

Paper : On-board Satellite Image Compression Using Reconfigurable FPGAs
Authors : A.S. Dawood, J.A. Williams and S.J. Visser

Paper : Efficient Single-Chip Implementation of SHA-384 & SHA-512
Authors : M. McLoone and J.V. McCanny

Paper : An Optimal PCM Codec Soft IP Genereator and Its Application
Authors : G. Wu, L. Chen, Y. Jeang and G. Jong

Paper : Efficient 4-input LUTs FPGA Implementation of Combinatorial Multiplier over Canonical Base GF(16)
Authors : V. Tomashau

Paper : FPGA Based Real-time Adaptive Filtering for Space Applications
Authors : S.J. Visser, A.S. Dawood and J.A. Williams

POSTER SESSION 2

Paper : Diagnosis of Open Defects in FPGA Interconnect
Authors : M.B. Tahoori

Paper : Testing for Resistive Open Defects in FPGA
Authors : M.B. Tahoori

Paper : A Novel Parallel Three Phase Genetic Approach To Routing For Field Programmmable Gate Arrays
Authors : A. Muthukaruppan, S. Suresh and V. Kamakoti

Paper : Reconfigurable Implementation of Radiosity Distribution Computation
Authors : J.Y.H. Ko and K.W. Ng

Paper : Specification Of Concurrent Reconfigurable Hardware Using Hardware Join Java
Authors : J. Hopf, G.S. Itzstein and D. Kearney

Paper : Fusion For Uninhabited Airborne Vehicles
Authors : M. D. Jasiunas, D. A. Kearney, J. Hopf and G. B. Wigley

Paper : Compiling Policy Descriptions into Reconfigurable Firewall Processors
Authors : T.K. Lee, S. Yusuf, W. Luk, M. Sloman, E. Lupu and N. Dulay

Paper : Design and Implementation of a Novel Architecture for Symmetric FIR filters with Boundary Handling on Xilinx VIRTEX FPGAs
Authors : A. Benkrid, K. Benkrid and D. Crookes

Paper : Enabling Technologies for Reconfigurable System-on-Chip
Authors : N.W. Bergmann

Paper : FPGA Implementation of MFNN for Image Registration
Authors : M.S. Puranik and D.C. Gharpure

POSTER SESSION 3

Paper : An Efficient Architecture for an Improved Watershed Algorithm and its FPGA Implementation
Authors : C. Rambabu, I. Chakrabarti and A. Mahanta

Paper : The Hardware Implementation of a Genetic Algorithm Model with FPGA
Authors : T. Lei, M. Zhu and J. Wang

Paper : Dynamic reconfiguration for the common key encryption using FPGA
Authors : T. Yamaguchi, T. Hashiyama and S. Okuma

Paper : Field Modifiable Architecture with FPGAs and its Design Methodology
Authors : S. Komatsu, Y. Kojima, H. Saito, K. Seto and M. Fujita

Paper : The Feasibility study of designing a FPGA Multiplier-core on Finite Field
Authors : C.H. Hsu, T.K. Truong, M.H. Jing, W.C. Wu and H.C. Wu

Paper : The Diversity Study of AES on FPGA Application
Authors : M.H. Jing, C.H. Hsu, Y.H. Chen, T.K. Truong and Y.T. Chang

Paper : Speedup Analysis of Simulation-Emulation Co-Operation
Authors : S.G. Miremadi, S.B. Sarmadi, G. Asadi

Paper : Performing Speech Recognition on Multiple Parallel Files Using Continuous Hidden Markov Models on an FPGA
Authors : S.J. Melnikoff, S.F. Quigley and M.J. Russell

Paper : Evolution-enabled reconfigurable computing using field programmable analog devices
Authors : A. Stoica, X. Guo, R.S. Zebulum, M.I. Ferguson and D. Keymeulen

Paper : FPGA-based Free-Form Deformation
Authors : J. Jiang, W. Luk and D. Rueckert

Paper : Incremental Programming for Reconfigurable Engines
Authors : D. Lee, T. K. Lee, W. Luk and P. Y. K. Cheung

POSTER SESSION 4

Paper : Delivering Error Detection Capabilities into a Field Programmable Device: The HORUS Processor Case Study
Authors : F. Rodriguez, J. C. Campelo and J. J. Serrano

Paper : Energy Efficiency of FPGAs and Programmable Processors for Matrix Multiplication
Authors : R. Scrofano, S. Choi and V. K. Prasanna

Paper : Reconfigurable Hardware Control Software Using Anonymous Libraries
Authors : C. Hinkelbein, A. Kugel, R. Manner and M. Muller

Paper : Logic Synthesis of Multi-output Functions for PAL-based CPLDs
Authors : K. Dariusz

Paper : A Method of Implementing Bit-Serial LDI Ladder Filters in FPGAs Using JBits
Authors : A. Carreira, T.W. Fox and L.E. Turner

Paper : PD-XML: Extensible Markup Language for Processor Description
Authors : S.P. Seng, K.V. Palem, R.M. Rabbah, W.F. Wong, W. Luk and P.Y.K. Cheung

Paper : Sensitivity of FPGA Power Evaluation
Authors : K.K.W. Poon and S.J.E. Wilton

Paper : Pattern Recognition in the HADES – Spectrometer: An Application of FPGA Technology in Nuclear and Particle Physics
Authors : I. Frohlich, A. Gabriel, D. Kirschner, J. Lehnert, E. Lins, M. Petri, T. Perez-Cavalcanti, J. Ritman, D. Schafer, A. Toia, M. Traxler and W. Kuehn

Paper : FPGA Education and Research Activities in Taiwan
Authors : Y.T. Chang, Y.T. Chou, W.C. Tsai and C.Y. Lee

Paper : Alternatives in FPGA-based SAD Implementations
Authors : S. Wong, B. Stougie and S. Cotofana

Paper : Strassen's Matrix Multiplication for Customisable Processors
Authors : H. Ip, J. Low, P.Y.K. Cheung, G. Constantinides, W. Luk, S.P. Seng and P. Metzgen

Asia-Pacific Technology Forum & Exhibition

Asia-Pacific Technology Forum

Time: 2:30-5:30pm, Dec 18, 2002 (registration begins at 2pm)
Place: LT3, Esther Lee Building, CUHK

(5 minutes walk from the KCR University Station)

Theme: Field-Programmable Technology in Industry: Opportunities and Experiences

- Applications: embedded systems, video/image processing, compression/encryption
- Short talks by university and industrial experts, followed by discussions
- Demonstrations and exhibition

Forum schedule

TIME	SESSION	SPEAKER	AFFILIATION
1430	F0	W. Luk	Imperial College
Introduction			
1435	F1	L. Leung	Altera Corporation
1450	F2	P.Y.K. Cheung	Imperial College
1505	F3	D. Levi	Xilinx Inc.
1520	F4	P.H.W. Leong	Chinese University of Hong Kong
1535	F5	P. Master	Quicksilver Technology
1550	F6	S. Wilton	University of British Columbia
1605	F7	R. Gook	Celoxica
1620	F8	B. Nelson	Brigham Young University
1635	F9	O. Mencer	Bell Laboratories
1650	F10	T. Rissa	Nokia
1705	F11	W. Luk	Imperial College
Summary			

Technical Tutorials on FPT

Time: 9:30am-6pm, December 19, 2002 (registration begins at 9am)
Place: LT2, Sino Building, CUHK

(8 minutes walk from the KCR University Station)

Session 1: Xilinx Inc. (0930 – 1130)
Title: Tools for Run-Time Reconfiguration and Design Experiences of a State-of-the-Art Reconfigurable Crossbar Switch for Telecommunications
Speaker: *Delon Levi*

Abstract:
Unlike ASICS and custom manufactured devices, FPGAs are based on SRAM technology which enable user-defined circuits to be modified. This capability enables design updates and bug fixes without remanufacturing new silicon. Run-time reconfiguration takes this concept a step further by stipulating circuit modification as a required behavior. Only static circuits, however, are produced by mainstream FPGA tools, which until recently have been heavily influenced by ASIC tools. In this tutorial we will examine a new set of tools that are modeled on software development flows. Run-time generation of hardware IP, routing, and configuration bitstreams will be explored. Tools for verifying changing circuits will also be examined. Several design examples will be discussed, like reconfigurable cryptography algorithms, reconfigurable CAMs, and evolvable hardware.

In the last half we will study in detail a state-of-the-art commercial design of a reconfigurable 1Kx1K crossbar switch. Partial configuration of the routing fabric at run-time increases switch capacity by 16X. Constant clock latency through all paths is maintained through partial configuration. Each path operates at 155.5 MHz, for a total aggregate bandwidth of 155.5 GBits/s accross all outputs. The design is implemented in 60% of a XC2V6000 FPGA. Finally, the partial configuration controller is itself a circuit that is designed for maximum reconfiguration speed.

Session 2: Celoxica (1300 – 1500)
Title: Introduction to software-compiled system design for Field Programmable System on Chip (FPSoC)
Speaker: *Lucien Murray-Pitts*

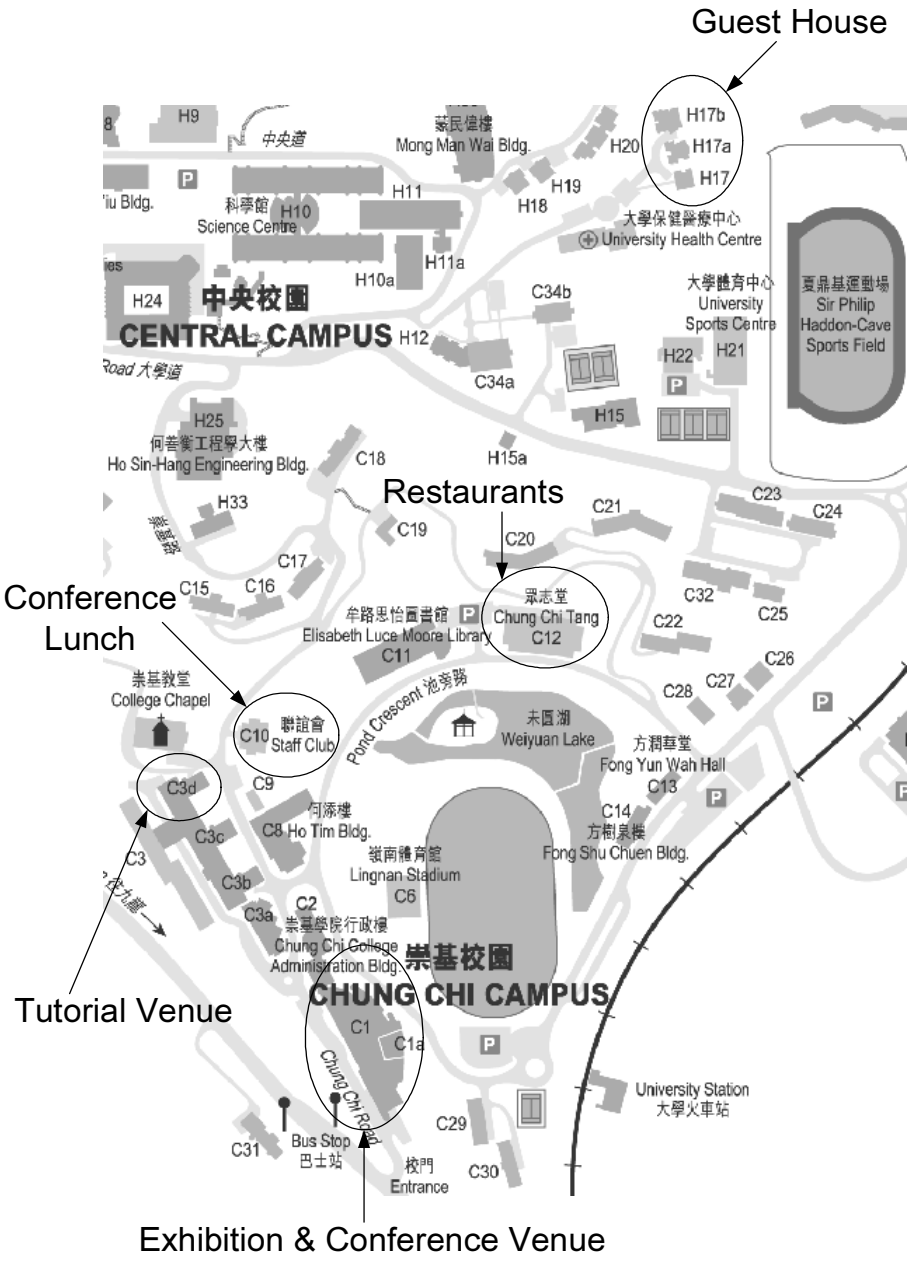
Abstract:
1. Brief introduction to Celoxica
2. Overview of 'software-compiled system design' our design methodology that drives (from the system level specification) partitioning, co-verification and co-simulation through to direct implementation in FPSoC.
3. Brief overview of the Handel-C language (language semantics, constructs and extensions)
4. Brief overview of the DK design suite (functionality and specification, capabilities for language and tool interoperability e.g. HDLs & Co-Simulation)
5. Introduction to the DSM (Data Stream Manager) codesign API
6. Designing hardware
   - Creating hardware using Handel-C (basic language semantics, constructs and design techniques)
7. Codesign example: JPEG2000
   - Porting C source code to Handel-C
   - Setting up DSM calls between software and hardware
   - Optimization techniques for efficient hardware implementation
   - Implementing your design using the PAL (Platform Abstraction Layer) API
   - Integrating DK design suite with Wind River's Tornado and VxWorks
     i. MQ coder (performance optimization)
     ii. Discrete Wavelet Transform (area optimization)

Session 3: Altera (1600 – 1800)
Title: Altera SOPC Solution
Speakers: *Paul Chan and Brian Ching*

Abstract:
Altera system-on-a-programmable-chip (SOPC) solutions combine products, software, and intellectual property (IP) to serve professional needs in a variety of applications. Designers can improve their system-level designs and differentiate their products to make them the most competitive and distinctive in the market.

This tutorial session gives an overview of Altera SOPC solutions to enable designers to learn and understand the inherent advantages of using a programmable solution, such as:
- Programmable = time-to-market, flexibility, and low risk
- Design reuse using IP cores
- System design techniques (e.g. block based design and timing closure)
- Provide solutions to SOPC designs and concepts as well as state-of-the-art technology
- Examine the options available to today's systems designers and look at the rapid progress made in SOPC designs
- Designing with the latest development and verification tools
- Demonstrate real systems being built with Altera SOPC solutions

Conference Map

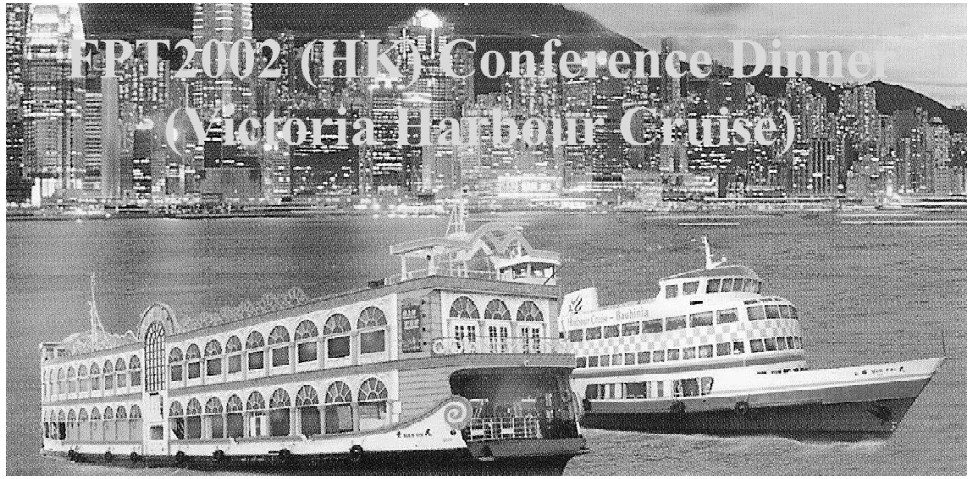


Conference Dinner Information

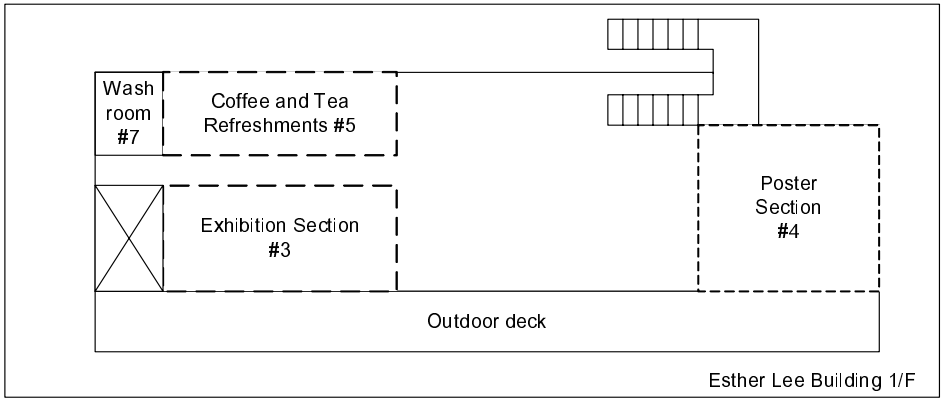
Hung Hom Pier gathering location

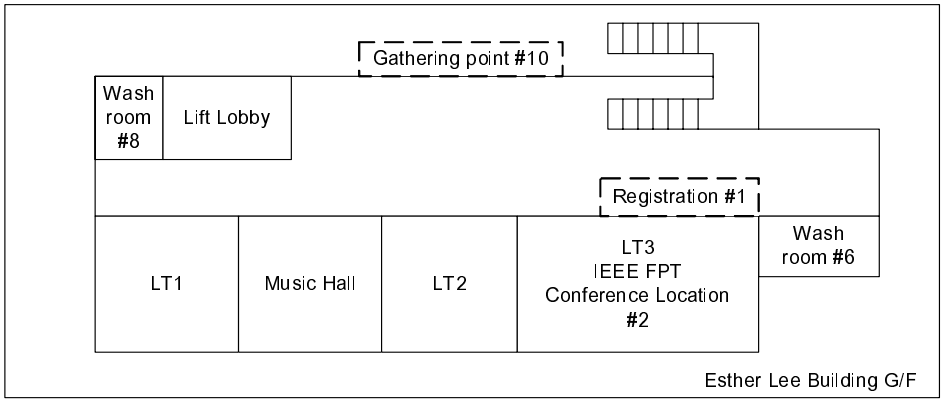
Meet and embark at Hung Hom Ferry Pier labeled ⊕

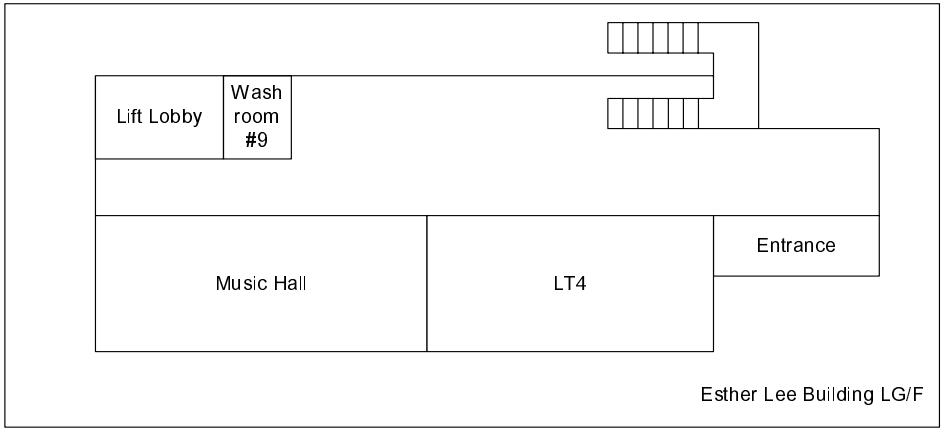
Conference dinner ticket



Esther Lee Building Floorplan

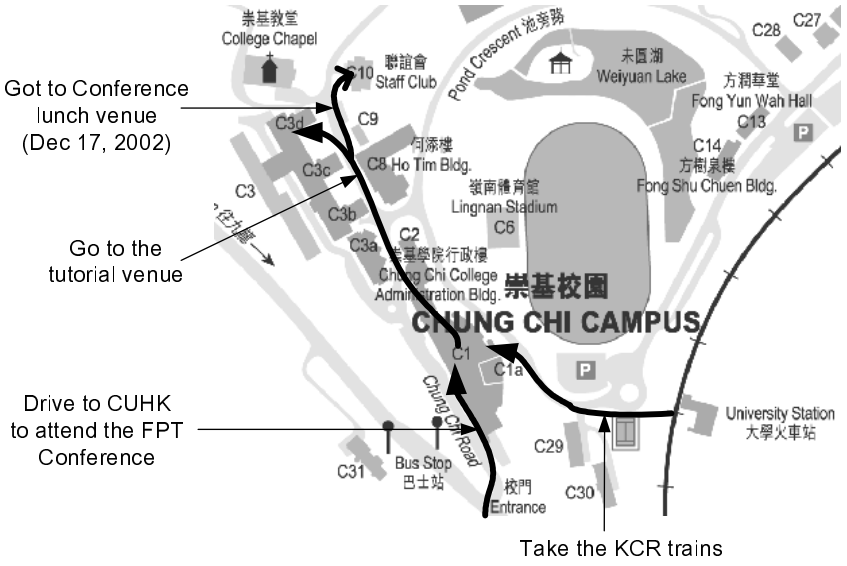






Helpful Hints

- **Color coding of the badges**
  - Blue – Speakers, Red – Student helpers
- **How to get to Esther Lee Building (ELB) from the Station?**
  - Exit the station (see photograph P1, page 18-21) and then follow the path on the left side (P2)
  - Walk along this path until you reach a stair (P4)
  - Go up and you can see the entrance of ELB on LG/F (P5).
- **How to get to LT3 in Esther Lee Building (ELB)?**
  - LT3 is located in the G/F of ELB
  - It is the theater located in #2 of the floorplan.
- **Where to get coffee?**
  - The refreshments are located in the 1/F of ELB
  - Please refer to #5 of the Floorplan.
- **Where to find the washrooms?**
  - They are located on 1/F: #7, G/F: #6, #8, LG/F: #9.
- **Where to gather and go to the Conference Dinner?**
  - Bus will leave from #10 on Tuesday evening 19:15.
- **Where to find machines with Internet access?**
  - They are located in ELB room 205 on 2/F.
- **How to go to Sino Building (P22) and attend the tutorials (P23)?**



CUHK Campus

University Station (P1)

Walk along this path (P2)

Esther Lee Building (P3)

Go upstairs (P4)

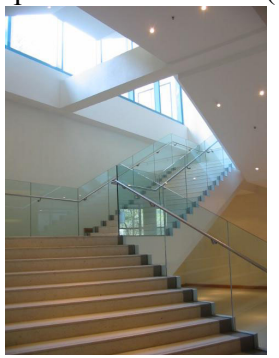
ELB main entrance (P5)

Esther Lee Building ELB (P6)

Exhibition & Conference Venue

ELB LG/F (P7)

Go upstairs to ELB G/F (P8)



ELB G/F (P9)

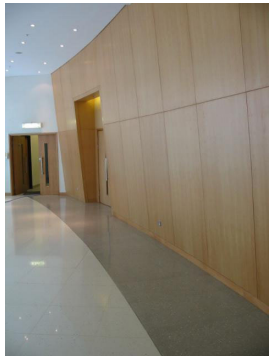
ELB LT3 (P10)
Main conference/Tech. Forum

ELB LT3 - Inside 1 (P11)

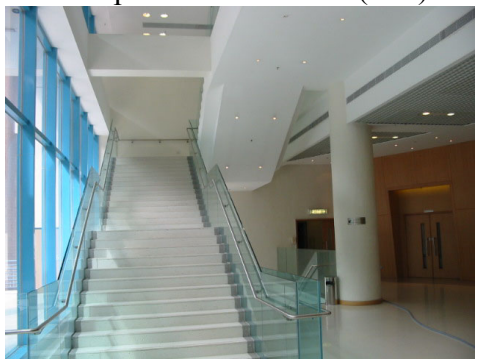
ELB LT3 - Inside 2 (P12)

Registration, Exhibition & Poster Venues

Registration venue ELB G/F (P13)



Go upstairs to ELB 1/F (P14)



Exhibition venue ELB 1/F (P15)

Poster venue ELB 1/F (P16)

Outdoor deck ELB 1/F (P17)

Shuttle bus gathering point
Conference dinner ELB G/F (P18)

Tutorial Venue

Leave Esther Lee Building (P19)

Go to the one nearest chapel (P20)

Chapel (P21)

Sino Building SB (P22)

SB LT2 – Tutorial (P23)

C10 – Chung Chi Staff Club (P24)

We hope you enjoy the conference venue and the Chinese University of Hong Kong campus.