The 2009 International Conference on Field-Programmable Technology (FPT'09)

http://www.icfpt.org

Sydney, Australia
9-11 December 2009

FPT is the premier conference in the Asian region on field-programmable technologies including reconfigurable computing devices and systems containing such components. Field-programmable devices promise the flexibility of software with the performance of hardware. The development and application of field-programmable technology have become important topics of research and development. Field-programmable components are widely applied, such as in high-performance computing systems, embedded and low-power control instruments, mobile communications, rapid prototyping and product emulation.

Submissions are solicited on new research results and detailed tutorial expositions related to field-programmable technologies, including but not limited to:

- **Tools and Design techniques for field-programmable technology** including placement, routing, synthesis, verification, debugging, run-time support, technology mapping, partitioning, parallelization, timing optimization, design and run-time environments, languages and modelling techniques, provably-correct development, intellectual property core based design, domain-specific development, hardware/software co-design.
- **Architectures for field-programmable technology** including field programmable gate arrays, complex programmable logic devices, coarse-grained reconfigurable arrays, field programmable interconnect, field programmable analogue arrays, field programmable arithmetic arrays, memory architectures, interface technologies, low-power techniques, adaptive devices, reconfigurable computing systems, high-performance reconfigurable systems, evolvable hardware and adaptive computing, fault tolerance and avoidance.
- **Device technology for field-programmable logic** including programmable memories such as non-volatile, dynamic and static memory cells and arrays, interconnect devices, circuits and switches, and emerging VLSI device technologies.
- **Applications of field-programmable technology** including biomedical and scientific computation accelerators, network processors, real-time systems, rapid prototyping, hardware emulation, digital signal processing, interactive multimedia, machine vision, computer graphics, cryptography, robotics, manufacturing systems, embedded applications, evolvable and biologically-inspired hardware.

Note that simply implementing an application using an FPGA is not sufficient to count as a research contribution. Applications-based papers should emphasise novel design techniques or clearly articulated and measured system performance benefits.

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Submissions

The program committee solicits papers describing original research or high quality tutorial expositions in field-programmable technology including, but not limited to, the areas of interest indicated above. High quality posters are also solicited. Current postgraduate research students are invited to submit a short paper detailing their proposed research to be presented in a poster-based PhD forum.

In addition to the above, the organizers solicit contributions to the following:

- Special Session on Self-Adaptive Reconfigurable Architectures for Ambient Intelligence
- Demonstration of Tools, Techniques and Applications

Further details of these special sessions are available on the conference website.

Papers must be prepared in PDF format using the template files provided and submitted electronically via the conference website. Full papers should not exceed 8 pages in length, while posters should not exceed 4 pages in length. PhD forum papers are limited to 2 pages.

FPT uses a blind reviewing system. Manuscripts must not identify authors or their affiliations. Self-references should be blanked out. Papers that identify authors will NOT be considered.

Proposals for half and full day tutorials in the areas of interest are also sought. Tutorials are likely to be scheduled for 7 or 8 December, preceding the conference.

Design Competition

Implement the fastest FPGA-based Sudoku solver for puzzles of arbitrary size – please refer to the conference website for details.

Important Dates

Submission of regular papers and tutorial proposals due:	8 June 2009
Demonstration session submissions due:	3 August 2009
Notification of acceptance:	10 August 2009
Design competition entries due:	9 October 2009

Organizing Committee

General Chair:	Oliver Diessel (UNSW, Australia) odiessel@cse.unsw.edu.au
Program Co-Chairs:	Neil Bergmann (UQ, Australia) n.bergmann@itee.uq.edu.au
	Lesley Shannon (SFU, Canada) lshannon@ensc.sfu.ca
Tutorials and Workshops Chair:	Doug Maskell (NTU, Singapore) ASDouglas@ntu.edu.sg
Special Session Chair:	Jean-Philippe Diguet (CNRS / Université Européenne de Bretagne, France) jean-philippe.diguet@univ-ubs.fr
Demo Session Chair:	Suhaib Fahmy (TCD, Ireland) suhaib.fahmy@tcd.ie
Design Competition Co-Chairs:	Hayden So (HKU, Hong Kong) hso@eee.hku.hk
	Satnam Singh (Microsoft, UK) satnams@microsoft.com
	Jorgen Peddersen (UNSW, Australia)jorgenp@cse.unsw.edu.au

Sponsorship

Enquiries regarding financial sponsorship should be directed to the General Chair.