The 2009 International Conference on Field-Programmable Technology (FPT'09)

The University of New South Wales, Sydney, Australia

9 - 11 December 2009

ADVANCE PROGRAM

Date	Day	Start Time	EndTime	Title	Authors
9/12/09	**Wed**	**0800**	**0900**	**REGISTRATION**	
	Wed	**0900**	**0910**	**Welcome**	
	Wed	**0910**	**1000**	**Keynote Session 1.1**	**Chair: Oliver Diessel**
	Wed	0910	1000	Packets Everywhere: The Great Opportunity for Field Programmable Technology	Gordon Brebner, Xilinx
	Wed	**1000**	**1100**	**Morning Tea, Poster Session 1.2, see details below**	
	Wed	**1100**	**1240**	**Oral Session 1.3 - Applications**	**Chair: Paul Beckett**
	Wed	1100	1125	Design of a Vehicle-to-Vehicle Communication System on Reconfigurable Hardware	Oliver Sander, Benjamin Glas, Christoph Roth, Jürgen Becker and Klaus D. Müller-Glaser
	Wed	1125	1150	Implementation of a Foveal Vision Mapping	Donald Bailey and Christos Bouganis
	Wed	1150	1215	An Architecture of Optimised SIFT Feature Detection for an FPGA Implementation of an Image Matcher	Lifan Yao, Hao Feng, Yiqun Zhu, Zhiguo Jiang, Danpei Zhao and Wenquan Feng
	Wed	1215	1240	Exploiting Memory Customization in FPGA for 3D Stencil Computations	Muhammad Shafiq, Miquel Pericas, Raul de la Cruz, Mauricio Araya, Nacho Navarro and Eduard Ayguade
	Wed	**1240**	**1400**	**Lunch**	
	Wed	**1400**	**1540**	**Oral Session 1.4 - Alternative FPGA Architectures**	**Chair: Hideharu Amano**
	Wed	1400	1425	Towards a Balanced Ternary FPGA	Paul Beckett
	Wed	1425	1450	Concurrently Optimizing FPGA Architecture Parameters and Transistor Sizing: Implications for FPGA Design	Alastair M. Smith, George A. Constantinides, Steven J. E. Wilton and Peter Y. K. Cheung
	Wed	1450	1515	Simulation of a QCA-Based CLB and a Multi-CLB Application	Chia-Ching Tung, Ruchi B. Rungta and Eric R. Peskin
	Wed	1515	1540	A Flexible DSP Block to Enhance FPGA Arithmetic Performance	Hadi Parandeh-Afshar, Alessandro Cevrero, Panagiotis Athanasopoulos, Philip Brisk, Yusuf Leblebici and Paolo Ienne
	Wed	**1540**	**1610**	**Afternoon Tea**	

	Wed	**1610**	**1750**	**Oral Session 1.5 - Low-level Architecture and Process Technology**	**Chair: Khaled Benkrid**
	Wed	1610	1635	VMATCH: Using Logical Variation to Counteract Physical Variation in Bottom-Up, Nanoscale Systems	Benjamin Gojman and André DeHon
	Wed	1635	1700	PGR: Period and Glitch Reduction Via Clock Skew Scheduling, Delay Padding and GlitchLess	Xiao Dong and Guy G.F. Lemieux
	Wed	1700	1725	A Detailed Delay Path Model for FPGAs	Eddie Hung, Steven J. E. Wilton, Haile Yu, Thomas C. P. Chau and Philip H.W. Leong
	Wed	1725	1750	Leakage Power Reduction for Coarse-Grained Dynamically Reconfigurable Processor Arrays Using Dual Vt Cells	Keiichiro Hirai, Masaru Kato, Yoshiki Saito and Hideharu Amano
	Wed	**1800**	**2100**	**Welcome Function & Demo Session 1.6 - details below**	
10/12/09	**Thurs**	**0800**	**0830**	**REGISTRATION**	
	Thurs	**0830**	**0845**	**Welcome, Announcements**	
	Thurs	**0845**	**1000**	**Keynote Session 2.1**	**Chair: Philip Leong**
	Thurs	0845	0935	From Dynamic Reconfiguration to Self-Reconfiguration: Invasive Algorithms and Architectures	Jürgen Teich, University of Erlangen-Nuremberg
	Thurs	0935	1000	ASIF: Application Specific Inflexible FPGA	Husain Parvez, Zied Marrakchi and Habib Mehrez
	Thurs	**1000**	**1100**	**Morning Tea, Poster Session 2.2, see details below**	
	Thurs	**1100**	**1240**	**Oral Session 2.3 - FPGA-Based Computing**	**Chair: Leseley Shannon**
	Thurs	1100	1125	The Challenges of Using an Embedded MPI for Hardware-Based Processing Nodes	Daniel L. Ly, Manuel Saldana and Paul Chow
	Thurs	1125	1150	Transforming Write Collisions in Block RAMs into Security Applications	Tim Gueneysu and Christof Paar
	Thurs	1150	1215	FPGA Implementation of an Invasive Computing Architecture	Abdulazim Amouri, Farhadur Arifin, Frank Hannig and Jürgen Teich
	Thurs	1215	1240	FFPU: Fractured Floating Point Unit for FPGA Soft Processors	Neil Hockert and Katherine Compton
	Thurs	1240	1250	FPT2010 Announcement	
	Thurs	**1250**	**1400**	**Lunch**	
	Thurs	**1400**	**1540**	**Oral Session 2.4 - Synthesis and Simulation**	**Chair: Makato Ikeda**
	Thurs	1400	1425	Rapid Synthesis and Simulation of Computational Circuits in an MPPA	David Grant, Graeme Smecher, Guy G.F. Lemieux and Rosemary Francis
	Thurs	1425	1450	Self-Hosted Placement for Massively Parallel Processor Arrays	Graeme Smecher, Steve Wilton and Guy G.F. Lemieux
	Thurs	1450	1515	Congestion-Driven Regional Re-Clustering for Low-Cost FPGAs	Darius Chiu, Guy G.F Lemieux and Steve Wilton
	Thurs	1515	1540	An Adaptive Sequential Monte Carlo Framework with Runtime HW/SW Repartitioning	Markus Happe, Enno Lübbers and Marco Platzner
	Thurs	**1540**	**1610**	**Afternoon Tea**	

	Thurs	**1610**	**1700**	**Oral Session 2.5 - Applications**	**Chair: Mark Shand**
	Thurs	1610	1635	Differential Power Analysis Resistance of Camellia and Countermeasure Strategy on FPGAs	Yingxi Lu, Maire O'Neill and John McCanny
	Thurs	1635	1700	Parallelizing Sparse Matrix Solve for SPICE Circuit Simulation Using FPGAs	Nachiket Kapre and André DeHon
	Thurs	**1715**		**BUS TO DINNER**	
	Thurs	**1800**	**2100**	**CONFERENCE DINNER**	
11/12/09	**Fri**	**0800**	**0830**	**REGISTRATION**	
	Fri	**0830**	**0845**	**Welcome, Announcements**	
	Fri	**0845**	**1000**	**Keynote Session 3.1**	**Chair: Peter Cheung**
	Fri	0845	0935	ASKAP Beamformer	John Bunton, CSIRO
	Fri	0935	1000	Announcement of Design Competition Winner & Talk by Sponsor	Altium
	Fri	**1000**	**1100**	**Morning Tea, Poster Session 3.2, see details below**	
	Fri	**1100**	**1240**	**Oral Session 3.3 - High-level Synthesis**	**Chair: André DeHon**
	Fri	1100	1125	K-Loops: Loop Skewing for Reconfigurable Architectures	Ozana Silvia Dragomir and Koen Bertels
	Fri	1125	1150	Profile Driven Data-Dependency Analysis for Improved High Level Language Hardware Synthesis	Peter Crosthwaite, John Williams and Peter Sutton
	Fri	1150	1215	Automatic Optimisation of MapReduce Designs by Geometric Programming	Qiang Liu, Tim Todman, Wayne Luk and George A. Constantinides
	Fri	1215	1240	Scheduling and 2D Placement Heuristics for Partially Reconfigurable Systems	Francesco Redaelli, Marco Domenico Santambrogio, Vincenzo Rana and Seda Ogrenci Memik
	Fri	**1240**	**1400**	**Lunch**	
	Fri	**1400**	**1605**	**Oral Session 3.4 - Applications**	**Chair: Guy Lemieux**
	Fri	1400	1425	FPGA vs MPPA for Positron Emission Tomography Pulse Processing	Michael Haselman, Nathan Johnson-Williams, Chad Jerde, Maria Kim, Scott Hauck, Thomas K. Lewellen and Robert Miyaoka
	Fri	1425	1450	Efficient Implementation of Fast Redundant Number Adders for Long Word-Lengths in FPGAs	William Kamp, Andrew Bainbridge-Smith and Michael Hayes
	Fri	1450	1515	A Parallel Spiking Neural Network Simulator	Kit Cheung, Simon R. Schultz and Philip H.W.
	Fri	1515	1540	FPGA vs. GPU for Sparse Matrix Vector Multiply	Yan Zhang, Yasser H. Shalabi, Rishabh Jain, Krishna K. Nagar and Jason D. Bakos
	Fri	1540	1605	American Option Pricing on Reconfigurable Hardware Using Least-Squares Monte Carlo Method	Xiang Tian and Khaled Benkrid
	Fri	**1605**	**1610**	**CLOSE**	

				POSTER, DEMO, PhD Session papers	
9/12/09	**Wed**	**1000**	**1100**	**Wednesday Morning Poster Session 1.2**	
				A High Performance FPGA-Based Core for Phylogenetic Analysis with Maximum Parsimony Method	Server Kasap and Khaled Benkrid
				Area, Delay, Power, and Cost Trends for Metal-Programmable Structured ASICs (MPSAs)	Usman Ahmed, Guy G.F. Lemieux and Steven J.E. Wilton
				An Architecture for Exploiting Coarse-Grain Parallelism on FPGAs	Davor Capalija and Tarek S. Abdelrahman
				Automatic Instrumentation of Profilers for FPGA-Based Design Space Exploration	Seiya Shibata, Yuki Ando, Shinya Honda, Hiroyuki Tomiyama and Hiroaki Takada
				A Novel Fast Online Placement Algorithm on 2D Partially Reconfigurable Devices	Thomas Marconi, Yi Lu, Koen Bertels and Georgi Gaydadjiev
				Exploring the Evolution of NoC-Based Spiking Neural Networks on FPGAs	Fearghal Morgan, Seamus Cawley, Brian Mc Ginley, Sandeep Pande, Liam J. Mc Daid, B. Glackin, J. Maher, and Jim Harkin
				Methodology for Designing Statically Scheduled Application-Specific SDRAM Controllers Using Constrained Local Search	Samuel Bayliss and George A. Constantinides
				An ASIC Implementation of Phase Correlation Based on Run-Time Reconfiguration Technique	Naoto Miyamoto, Katsuhiko Hanzawa and Tadahiro Ohmi
				Throughput Optimization by Pipeline Alignment of a Self Synchronous FPGA	Benjamin Devlin, Toru Nakura, Makoto Ikeda and Kunihiro Asada
				Real-Time Detection of Rotated Patterns Using FPGA	Yoshifumi Tanida and Tsutomu Maruyama
				Targeted Configurable Caches	John Shield, Peter Sutton and John Williams
				An Energy and Power Consumption Analysis of FPGA Routing Architectures	Peter Jamieson, Wayne Luk, Steve J.E. Wilton and George A. Constantinides
				Novel Hardening Techniques Against Differential Power Analysis for Multiplication in GF(2^n)	Felix Madlener, Marc Stöttinger and Sorin A. Huss
				A Module-Based Partial Reconfiguration Design for Solving Sparse Linear Systems Over GF(2)	Dimitrios Meintanis and Ioannis Papaefstathiou
				High Speed Merged-Datapath Design for Run-Time Reconfigurable Systems	Mahmood Fazlali, Ali Zakerolhosseini, Asadollah Shahbahrami and Georgi Gaydadjiev
				Using FPGA Resources for Direct Generation of Multivariate Gaussian Random Numbers	David B. Thomas and Wayne Luk
				Efficient Hardware Generation for Dynamic Programming Problems	Zubair Nawaz, Todor Stefanov and Koen Bertels
				SPY vs SLY: Run-Time Thread-Scheduler Aware Reconfigurable Hardware Allocators	Kyle Rupnow and Katherine Compton
9/12/09	**Wed**	**1800**	**2000**	**Wednesday Evening Demo Session 1.6**	
				ICAP-I: A Reusable Interface for the Internal Reconfiguration of Xilinx FPGAs	Victor Lai and Oliver Diessel
				Dynamic Reconfiguration in a PSoC Device	Alex Doboli, Patrick Kane and Dave Van Ess

				Low Power Image Processing Using MuCCRA-3: A Dynamically Reconfigurable Processor Array	Masayuki Kimura, Yoshiki Saito, Toru Sano, Masaru Kato, Vasutan Tunbunheng, Yoshihiro Yasuda and Hideharu Amano
				Using a Reconfigurable Compute Cluster for the Acceleration of Neural Networks	Christopher Pohl, Jens Hagemeyer, Johannes Romoth, Mario Porrmann and Ulrich Rückert
				FPGA-in-the-Loop-Simulations for Dynamically Reconfigurable Applications	Carlos Paiz, Christopher Pohl, Rafael Radkowski, Jens Hagemeyer, Mario Porrmann and Ulrich Rueckert
				FloRA: Coarse-Grained Reconfigurable Architecture with Floating-Point Operation Capability	Dongwook Lee, Manhwee Jo, Kyuseung Han and Kiyoung Choi
				Demonstration of Hardware-Accelerated Formal Verification	Hiroaki Yoshida, Satoshi Morishita and Masahiro Fujita
				Demonstration of the Fault Recognition and Recovery of FPGA Circuits by Means of Cytokine-Formal Immune Networks	Norma Montealegre
10/12/09	**Thurs**	**1000**	**1100**	**Thursday Morning Poster Session 2.2**	
				Performance Comparison of GPU and FPGA Architectures for the SVM Training Problem	Markos Papadonikolakis, Christos-Savvas Bouganis and George Constantinides
				A Distributed Operating System Supporting Strong Mobility of Reconfigurable Computing Applications in a Swarm of Unpiloted Airborne Vehicles	Mark Jasiunas, Avishek Chakraborty and David Kearney
				Optimization of Modular Multiplication on FPGA Using Don't Care Conditions	Bijan Alizadeh and Masahiro Fujita
				Round-based Priority Arbitration for Predictable and Reconfigurable Network-on-Chip	Chun-Hsien Lu, Kuo-Cheng Chiang and Pao-Ann Hsiung
				Reducing Dynamic Power Consumption in FPGAs Using Precomputation	Chi Chiu Tsang and Hayden K.-H. So
				Automated Application Acceleration Using Software to Hardware Transformation	Qiwei Jin, David B. Thomas and Wayne Luk
				A Study on Interconnection Networks of the Dynamically Reconfigurable Processor Array MuCCRA	Masaru Kato, Toru Sano, Yoshihiro Yasuda, Yoshiki Saito and Hideharu Amano
				Routing Optimization for Hybrid FPGAs	Chi Wai Yu, Wayne Luk, Steven J.E. Wilton and Philip H.W. Leong
				Benchmark Results for Asynchronous High-Speed FPGAs Focusing on High Performance Digital Signal Processing	Lars Rockstroh, Wenbin Li, Juergen Hillebrand, Marek Wroblewski and Sven Simon
				Option Pricing with Multi-Dimensional Quadrature Architectures	Anson H.T. Tse, David B. Thomas and Wayne Luk
				DRAFT: Flexible Interconnection Network for Dynamically Reconfigurable Architectures	Ludovic Devaux, Sana Ben Sassi, Sebastien Pillement, Daniel Chillet and Didier Demigny
				Reconfigurable Acceleration of Neural Models with Gap Junctions	Mark Wildie, Wayne Luk, Simon Schultz, Philip H.W. Leong and Andreas Fidjeland
				Modelling Degradation in FPGA Lookup Tables	Edward Stott, Pete Sedcole and Peter Cheung

				FPGA Implementation of Mixed Integer Quadratic Programming Solver for Mobile Robot Control	Yusuke Shimai, Junichi Tani, Hiroki Noguchi, Hiroshi Kawaguchi and Masahiko Yoshimoto
				A Flexible FPGA-Based MIMO Geometric Fading Channel Simulator for Rapid Prototyping	Saeed Fouladi Fard, Amirhossein Alimohammad, Bruce Cockburn and Christian Schlegel
				Automated Dynamic Reconfiguration for High-Performance Regular Expression Searching	Ken Eguro
				rSesame — A Generic System-Level Runtime Simulation Framework for Reconfigurable Architectures	Kamana Sigdel, Mark Thompson, Carlo Galuzzi, Andy D. Pimentel and Koen Bertels
11/12/09	**Friday**	**1000**	**1100**	**Friday Morning Poster Session 3.2**	
				Flexible Framework for Commodity FPGA Cluster Computing	Jeremy Espenshade, Marcin Lukowiak, Muhammad Shaaban and Gregor von Laszewski
				Efficient Reconfigurable Architectures for 3D Medical Image Compression	Afandi Ahmad and Abbes Amira
				Automatic System Architecture Synthesis for FPGA-Based Reconfigurable Computers	Colin Yu Lin, Ngai Wong and Hayden Kwok-Hay So
				Operating System Management of Reconfigurable Hardware Computing Systems	Kyle Rupnow
				The Effect of Node Size, Heterogeneity, and Network Size on FPGA based NoCs	Jason Lee and Lesley Shannon
				Reconfigurable Sparse/Dense Matrix-Vector Multiplier	Georgi Kuzmanov and Mottaquiallah Taouil
				QoS-Aware Dynamic Power Management for Coarse-Grained Reconfigurable Architecture	Ganghee Lee, Manhwee Jo, Yongjin Ahn, Kiyoung Choi and Nikil Dutt
				A Floating-Point Accumulator for FPGA-Based High Performance Computing Applications	Song Sun and Joseph Zambreno
				A High-Performance Double Precision Accumulator	Krishna K. Nagar and Jason D. Bakos
				3-Tier Reconfiguration Model for FPGAs Using Hardwired Network on Chip	Muhammad Aqeel Wahlah and Kees Goossens
				HW/SW Co-Design of Identity-Based Encryption Using a Custom Instruction Set	Leonardo Amaral, Guido Araujo and Julio López
				Run Time Mapping of Adaptive Applications onto Homogeneous NoC-Based Reconfigurable Architectures	Stefan Wildermann, Tobias Ziermann and Jürgen Teich
				FPGA Implementation of a 64-Bit BID-Based Decimal Floating-Point Adder/Subtractor	Amin Farmahini-Farahani, Charles Tsen and Katherine Compton
				Configurable CMOS H-Tree Logic Module	Shun-Wen Cheng
				An FPGA-Based Sudoku Solver Based on Simulated Annealing Methods	Pavlos Malakonakis, Miltiadis Smerdis, Euripides Sotiriades and Apostolos Dollas
				The TU Delft Sudoku Solver on FPGA	Kees van der Bok, Mottaqiallah Taouil, Panagoitis Afratis and Ioannis Sourdis
				An Initial Specific Processor for Sudoku Solving	Carlos González, Javier Olivito and Javier Resano