Workshop – Altera:

清華大學

Course Name: Design and Implementation of Digital TV Box using Altera DE2 FPGA Board

Date/Time:

[Session A]: 9am – 5pm. December 6, 2010 (Chinese Version)

[Session B]: 9am – 5pm. December 7, 2010 (English & Chinese Version)

NOTE: Both Session A & B have same content except Session B has an real-time English Lecturer (bilingual course)

Place: Tsinghua University Altera Joint Lab (West Building District 4 – 209)

Lecturer: Dr. Stephen Brown, Sean Peng, Rosaline Lin, Allen Houng

Course Outline:

This course will explain how to design and implement a real Digital TV Box using Altera DE2 FPGA Board. This course requires intensive hand-on skills on Verilog and Quartus II System.

(1) Introduce High-Performance Digital TV Box System (9am-12pm)

- Advanced Logic Design and Verilog Language
- TV Decoder Introduction
- ITU656 YUV 4:2:2 Decoder and Implementation.
- De-interlace Controller Design and Implementation

- Image / Video Scalar Design
- VGA Controller Design and Implementation
- Image Processor for Machine Vision

(2) Lab Exercise and Implementation (1pm-5pm)

- DE2 Board Hand-on Exercise
- Digital TV Box Design and Implementation
- VGA Controller Design and Implementation
- Color Space Convertor Design and Implementation

Online Registration:

Chinese Version: http://chinese.terasic.com.cn

English Version: http://english.terasic.com.cn

Please contact Ms. Sunny Yen for immediate service.

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